National Semiconductor

FGC Series Advanced 2-Micron CMOS Gate Array Family

Description

The FGC Series is an advanced, high performance CMOS gate array family designed for LSI implementation of existing discrete logic systems and new designs requiring high density and low power. With up to 8000 gates and high I/O to gate ratios, the FGC family offers single gate array solutions to a wide variety of digital logic applications. Table 1 summarizes the important characteristics of this gate array family.

Designed with true 2-micron design rules, the FGC Series is fabricated on an advanced, dual metal, oxide isolated, fully implanted CMOS process. Effective channel lengths of 1.3 microns coupled with reduced junction area capacitance allows system clock speeds up to 50 MHz. Internal gate propagation delays range from 1.1 ns typically to 1.9 ns worst case industrial and 2.0 ns for military operation.[1] Operating from a single 5 V power supply, these arrays exhibit extremely low power dissipation, typically 20 μW/gate/MHz.

FGC Series Features

- **500, 1200, 2400, 4000, 6000 and 8000 Gates**
- **True 2-micron Silicon Gate CMOS Technology**
- **High Performance—Typical Internal Delays 1.1 ns**
- **8 mA Output Drive Current Standard**
- **Low Power Dissipation—Typically 20 μW/gate/MHz**
- **Selectable CMOS or TTL I/O**
- **No Internal Cells Required for I/O Buffer**
- **Single 5 V Power Supply**
- **On-Chip Testability Features (Except FGC0500)**
- **Wide Choice of Package Pin Counts and Styles**
- **Complete Integrated CAD Support**
- **Second Source—VLSI Technology, Inc.**

[1] 2-input NAND. Fanout = 2, typical interconnect metal
Additional conditions include:
Industrial: V_{DD} = 4.5 V, T_J = 85°C, worst case process parameters
Military: V_{DD} = 4.5 V, T_J = 125°C, worst case process parameters

Array Organization

The general layout of the FGC6000 can be seen in Figure 7-1. Electrical components are organized into structural features called cells. Macro circuits, which are the basic building block of logic design, are comprised of one or more cells.

All FGC Series arrays use the same basic internal cell and I/O cell structure. Thus the same macros can be used throughout the FGC family.

The bussing structure for the FGC Series isolates the I/O cells from the internal array. Both the V_{DD} and Vss bus surround the array in second metal (dual-layer metal process) and are brought into the internal array area via a power rail structure. Each cell is connected to the power rail through the substrate which reduces the resistance and internal latch-up susceptibility.

Figure 7-1: FGC6000 Die

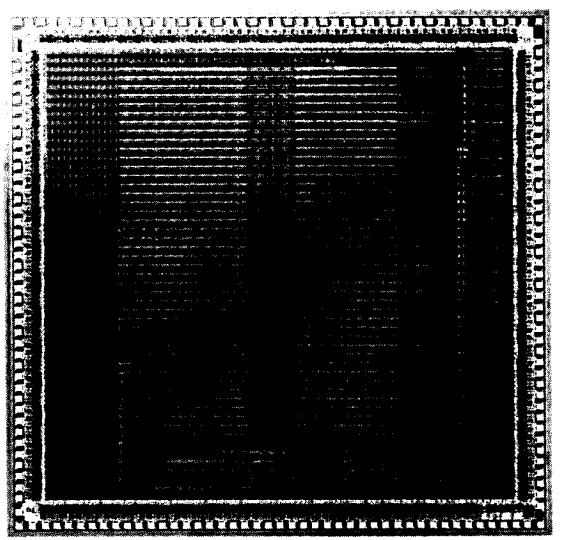

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Table 7-1: FGC Gate Array Family

	FGC0500	FGC1200	FGC2400	FGC4000	FGC6000	FGC8000
Total Cells	360	792	1728	2640	4000	5358
Equivalent Gates[2]	540	1188	2592	3960	6000	8037
Input Only	0	27	39	47	55	63
Inputs/Outputs	40	46	70	86	106	118
Total I/O	40	73	109	133	161	181
Power Pins	4	8	8	8	8	16
Testability Pins	0	3	3	3	3	3
Total Pins	44	84	120	144	172	200

[2] An equivalent gate is defined as one 2-input NAND.

Internal Cell Description

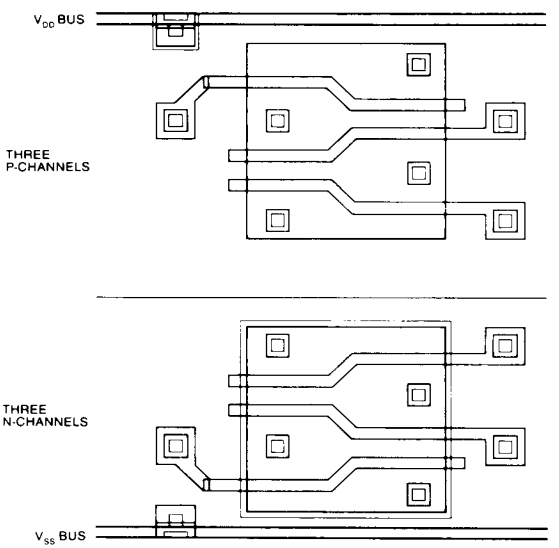
The basic internal cell of the FGC Series is shown in Figure 7-2. The cell consists of six transistors; three p-channel and three n-channel. The cell employs a bent gate pattern to optimize performance and minimize die size. Logic functions implemented with a single cell include two inverters, an inverter and a transmission gate, a two-input NAND or NOR and an inverter, and a three-input NAND or NOR.

Internal cells are preconnected to form macros, the basic logic element from which a design is implemented. The FGC Series shares a common macro library, which consists of most 7400 series logic functions. Additionally, macros to support enhanced testability design methodologies, such as scan test, are also available. Table 4 summarizes AC performance of commonly used macros.

Internal Cell Features

- 6-transistor cell (3 p-channel, 3 n-channel)
  - Greater routing efficiency over 4-transistor cell designs
- Single cell logic functions
  - Two single inverters
  - Inverter and transmission gate
  - 2-input NAND or NOR and inverter
  - 3-input NAND or NOR
- Bent gate pattern
  - Reduces junction capacitance
  - 15% area reduction over standard design

Figure 7-2: FGC Series Internal Cell



I/O Buffers

All I/O buffers contain built-in flexibility to allow both standard totem pole or 3-state output options without utilizing any internal cells. Additionally, each input can be individually programmed for either CMOS or TTL interface. This feature is available as a macro option, and is easily specified in the initial stages of logic design. Typical performance of input and output buffers is shown in Tables 5 and 6. The buffers have been designed to source or sink 8 mA (10 mA for FGC0500) across the industrial temperature range and 6 mA (8 mA for FGC0500) across the military range.

There are two cell types, input only and input/output, which are interspersed around the array (see Figure 7-3). Advantages of this configuration includes increased I/Os for a given gate count, reduced signal lengths and improved routability.

Input Protection

Input protection is incorporated into all I/O macros. As illustrated in Figure 7-4, dual V_{DD} and V_{SS} guard rings effectively reduce parasitic betas by providing recombination paths for minority carriers. This guard ring approach protects against up to 1200 V of static discharge.

Figure 7-4: Input Protection

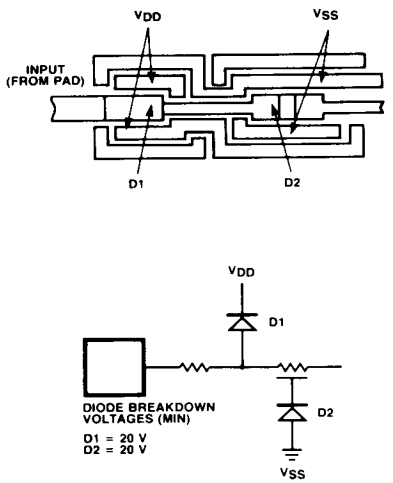


Figure 7-3: I/O Buffer Layout

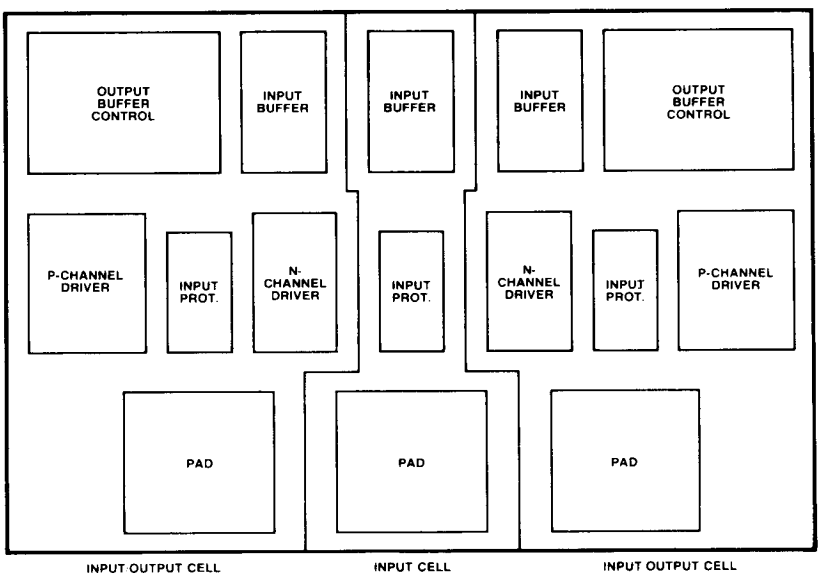


Table 7-2: Absolute Maximum Ratings Chart

Symbol	Parameter	Range	Unit
V_{DD}	Supply Voltage	−0.5 to +6	V
V_I	Input Voltage	−0.5 to V_{DD} +0.5	V
I_I	DC Input Current	±20	mA
T_{STG}	Storage Temperature Ceramic Package Plastic Package	 −65 to +150 −40 to +125	°C
T_A	Ambient Temperature Under Bias[3] Military Commercial/Industrial	 −55 to +125 −40 to +85	°C
T_L	Lead Temperature (Soldering, 10 seconds)	300	°C

[3] Junction temperature not to exceed ambient temperature by more than 20°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7-3: DC Characteristics (V_{DD} = 5.0 V ± 10%, T_A = −55°C to +125°C, unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Conditions
V_{IH}	Input HIGH Voltage[4] CMOS Input TTL Input (Industrial) TTL Input (Military)	 3.15 2.0 2.25	 V_{DD} V_{DD} V_{DD}	V	Guaranteed Input HIGH Voltage T_A = 125°C, V_{DD} = 4.5 V T_A = 0°C, V_{DD} = 5.25 V T_A = −55°C, V_{DD} = 5.5 V
V_{IL}	Input LOW Voltage[4] CMOS Input TTL Input	 -0.5 -0.5	 1.35 0.8	V	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage	V_{DD} − 0.05		V	I_{OH} = −1 μA, T_A = 125°C, V_{DD} = 4.5 V
	OB01F(FGC0500)	3.7		V	I_{OH} = −10 mA, T_A = 85°C, V_{DD} = 4.5 V I_{OH} = −8 mA, T_A = 125°C, V_{DD} = 4.5 V
	Other Output Buffers	3.7		V	I_{OH} = −8 mA, T_A = 85°C, V_{DD} = 4.5 V I_{OH} = −6 mA, T_A = 125°C, V_{DD} = 4.5 V
V_{OL}	Output LOW Voltage		0.1	V	I_{OL} = 1 μA, T_A = 125°C, V_{DD} = 4.5 V
	OB01F(FGC0500)		0.4	V	I_{OL} = 10 mA, T_A = 85°C, V_{DD} = 4.5 V I_{OL} = 8 mA, T_A = 125°C, V_{DD} = 4.5 V
	Other Output Buffers		0.4	V	I_{OL} = 8 mA, T_A = 85°C, V_{DD} = 4.5 V I_{OL} = 6 mA, T_A = 125°C, V_{DD} = 4.5 V

Table 7-3: DC Characteristics, continued
(V_{DD} = 5.0 V ± 10%, T_A = −55°C to +125°C, unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Conditions
I_{IN}	Input Leakage Current	−10	10	μA	V_{IN} = V_{DD} or GND (Without Pullup Resistor)
I_{OZ}	3-State Output Leakage Current	−10	10	μA	V_{OUT} = V_{DD} or GND
C_{IN}	Input Capacitance		5	pF	Excluding Package
C_{OUT}	Output Capacitance		5	pF	Excluding Package
$C_{I/O}$	Transceiver Capacitance		5	pF	Excluding Package

[4] V_{IH} and V_{IL} are steady state specifications and are specified with respect to the device ground pin. All functional tests are performed using additional margins to account for AC noise.

AC Characteristics for Selected Macros

Table 7-4: Internal Cell

Macro	Cells	Description	Symbol	Typical Propagation Delay (ns) Fanout = 2	Worst Case Propagation Delay (ns) Commercial/Industrial[5] Fanout 2	Commercial/Industrial[5] Fanout 4	Military[6] Fanout 2	Military[6] Fanout 4
INV11	1	2 1x Inverters	t_{PLH} t_{PHL}	1.1 0.4	2.1 0.9	3.3 1.3	2.2 0.9	3.5 1.5
NA02	1	2-Input NAND	t_{PLH} t_{PHL}	1.4 0.8	2.5 1.8	3.8 2.7	2.8 1.9	4.1 2.9
NA04	2	4-Input NAND	t_{PLH} t_{PHL}	1.7 1.9	3.3 4.0	4.6 5.7	3.7 4.4	5.1 6.3
NOR02	1	2-Input NOR	t_{PLH} t_{PHL}	1.9 0.6	4.1 1.2	6.4 1.7	4.5 1.4	7.0 1.9
NOR04	2	4-Input NOR	t_{PLH} t_{PHL}	4.3 0.7	9.7 1.4	14.2 2.0	10.8 1.5	15.7 2.1
DFP01	4	D Flip-Flop (Clock→Q)	t_{PLH} t_{PHL}	2.6 2.1	5.4 4.2	6.5 4.8	5.9 4.7	7.2 5.3
DFP04	6	D Flip-Flop with Set, Reset (Clock →Q)	t_{PLH} t_{PHL}	3.1 3.2	6.4 6.4	7.6 6.9	7.0 7.1	8.2 7.8

[5] V_{DD} = 4.5 V, T_J = 85°C, Worst Case Process, Worst Case Wirelength.
[6] V_{DD} = 4.5 V, T_J = 125°C, Worst Case Process, Worst Case Wirelength.

Table 7-5: Input Buffer

Macro	Description	Symbol	Typical Propagation Delay (ns) Fanout=2	Worst Case Propagation Delay (ns) Commercial/Industrial[5,7] Fanout 2	Commercial/Industrial[5,7] Fanout 4	Military[6,7] Fanout 2	Military[6,7] Fanout 4
IOC011F	CMOS with Pullup, FGC0500	t_{PLH} t_{PHL}	1.9 2.2	3.5 3.9	4.0 4.5	3.6 4.2	4.3 4.9
IOT011F	TTL with Pullup, FGC0500	t_{PLH} t_{PHL}	1.5 2.1	4.1 6.3	4.9 7.1	4.4 7.1	5.2 8.0
IOC011	CMOS with Pullup	t_{PLH} t_{PHL}	1.9 2.0	2.4 3.6	3.0 4.0	2.7 3.8	3.3 4.3
IOT011	TTL with Pullup	t_{PLH} t_{PHL}	2.6 2.9	3.6 4.3	4.1 5.1	3.9 5.0	4.5 5.8

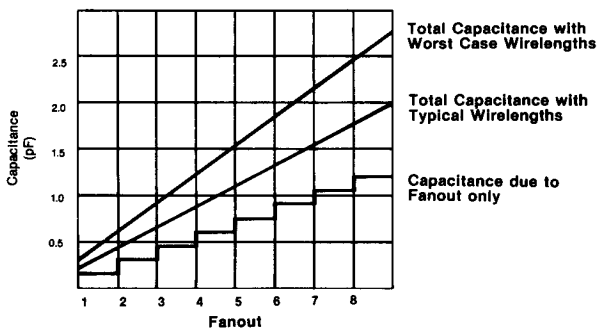
[7] CMOS Input t_r, t_f = 5 ns, FAST™ Input t_r, t_f = 2.5 ns.

Table 7-6: Output Buffer

Macro	Description	Symbol	Typical Propagation Delay (ns) Capacitive Load=15 pF	Worst Case Propagation Delay (ns) Commercial/Industrial[5] Capacitive Load (pF) 15	50	100	Military[6] Capacitive Load (pF) 15	50	100
OB01F	High Drive, FGC0500	t_{PLH} t_{PHL}	2.0 2.6	3.6 4.6	6.0 6.7	9.5 9.7	3.7 5.0	6.1 7.1	9.6 10.1
OB03F OB04F	3-State, FGC0500 Standard, FGC0500	t_{PLH} t_{PHL}	2.5 2.8	5.0 5.2	8.1 8.0	12.6 12.0	5.4 5.6	8.9 8.4	13.9 12.4
OB03 OB04	3-State Standard	t_{PLH} t_{PHL}	3.3 4.2	6.0 6.5	9.1 9.3	13.6 13.3	6.6 7.1	10.1 9.9	15.1 13.9

[5] V_{DD} = 4.5 V, T_j = 85°C, Worst Case Process, Worst Case Wirelength.
[6] V_{DD} = 4.5 V, T_j = 125°C, Worst Case Process, Worst Case Wirelength.

Figure 7-5: Capacitance Estimate for FGC Series Internal Macros



The figure illustrates variations of capacitance due to fanout and wirelength of an estimated average of internal cell macros. Typical wirelengths are based on an assumption of 15 mils length per connection, 30% first-layer and 70% second-layer metal routing. Worst case wirelengths assume 30 mils length per connection with 50% first-layer and 50% second-layer metallization.

Testability Features

Incorporated into the FGC Series (excluding the FGC0500) is a range of features to enhance design testability and simplify device testing. Three dedicated pads are located on each gate array, which may be bonded out to access three types of tests: output buffer parametric tests, DC functional tests, and an AC monitor test. A summary of each test is included in Table 7 and described more fully below.

The output parametric tests allow DC data to be measured on all outputs by controlling the three input pins, TEST, TOE (Test Output Enable), and TDAT (Test Data). This feature avoids the need for a lengthy test program to force outputs into the correct state for parametric testing.

System initialization can be greatly simplified by the JAM RESET feature. All flip-flops in a design can be simultaneously reset to zero, thereby avoiding long vector sequences to initialize a device into a known state. Alternately, scan testing is also supported, which among other features, allows the array to be initialized by serially writing data into each flip-flop.

An on-chip ring oscillator is provided as an indicator of AC performance of each device. The frequency is monitored by Fairchild at the wafer level as part of the outgoing test procedure. This signal may also be bonded out at the expense of an I/O pad and used as an incoming customer acceptance criterion.

Packaging

Fairchild offers the following packages and pin counts for the FGC Series: Plastic and Ceramic DIPs: 24, 40; Plastic and Ceramic Pin Grid Arrays: 68, 84, 100, 120, 132, 144, 180; Plastic and Ceramic J-Bend Chip Carriers: 44, 68, 84.

Table 7-7: FGC Series Testability Features

Type	Inputs			Output	Tests Performed	Description
	$\overline{TEST}$	$\overline{TOE}$	TDAT	ACOUT		
Output Buffer Parametric Tests	1	1	1	Disabled		Normal operation
	0	0	TDAT	Disabled	V_{OH}, V_{OL}, I_{OH}, I_{OL}	Test Data signal, TDAT, appears on all outputs
	0	1	0	Enabled	3-State Leakage	All outputs in 3-state mode
	0	1	1	Disabled	Standby Current	Measurement of static power dissipation
DC Functional Tests	1	1	0	Disabled	Jam Reset[a]	Resets all flip-flops to a LOW state
	1	0	Scan Data	Disabled	Scan Test[a]	Allows data to be serially scanned into all flip-flops
AC Monitor	0	1	0	Enabled	Ring Oscillator Frequency	Enables on-chip ring oscillator to monitor AC performance

[a] These tests are examples of Design for Testability techniques that the test pins can perform when additional internal cell logic is used.

CAD Support

Fairchild supports various options for design implementation, working either through FAIRCAD,™ Fairchild's in-house, computer-aided design system, or through one of several commercially available computer-aided engineering workstations. Using any of the hardware options, the designer may elect to perform any or all of the design steps or delegate responsibility to a Fairchild applications engineer.

Faircad Design Implementation

FAIRCAD, Fairchild's computer-aided design system, provides a user-friendly, technology-independent environment for building FGC Series gate arrays. FAIRCAD's fully integrated CAD tools allow the designer to perform all design functions from schematic entry, circuit analysis and fault grading to layout and automatic test vector generation. FAIRCAD can easily be learned and used by those with no prior CAD experience. Complete training is provided in a one-week class that takes the user through an entire design example.

FAIRCAD's high-level command menu and on-line help provides additional support by guiding the user step-by-step through the design cycle. Controlled program execution assures proper file management and adherence to design rules. In addition, summaries generated automatically after executing each program may be printed at any time for review. FAIRCAD supports off-hour batch submission—an effective method of increasing productivity while reducing CPU charges by running computer-intensive programs during non-prime-time hours.

In addition to design tools for implementing each of the steps illustrated below in Figure 7-6, FAIRCAD offers a number of system utilities including electronic mail, system/job status querying, color or B/W plot generation, as well as total CPU cost accounting.

FAIRCAD can be accessed at FAIRTECH Design Centers in Northern and Southern California; Dallas, Texas; Boston, Massachusetts; Minneapolis, Minnesota; Maitland, Florida and in international design centers in Reading, England and Tokyo, Japan. Additionally, a variety of compatible alphanumeric and graphic CRTs at customer sites can be linked to FAIRCAD through dial-up or leased lines. Further information on FAIRCAD's capabilities can be found in the Fairchild Gate Array CAD Support brochure, with comprehensive documentation available in the FAIRCAD User's Manual.

Workstation Implementation

Fairchild supports gate array design on Daisy Systems, Mentor Graphics and, in the future, Valid Logic and CAE computer-aided engineering workstations. Designers using workstations are provided with diskettes containing the macro library with all symbols and simulation models, and software for design verification, logic simulation, timing calculations and netlist generation.

Placement and routing is performed at a FAIRTECH Design Center after the netlist is transferred to FAIRCAD. Final netlengths are transferred back to the workstation for timing verification.

Figure 7-6: FAIRCAD Design Flow

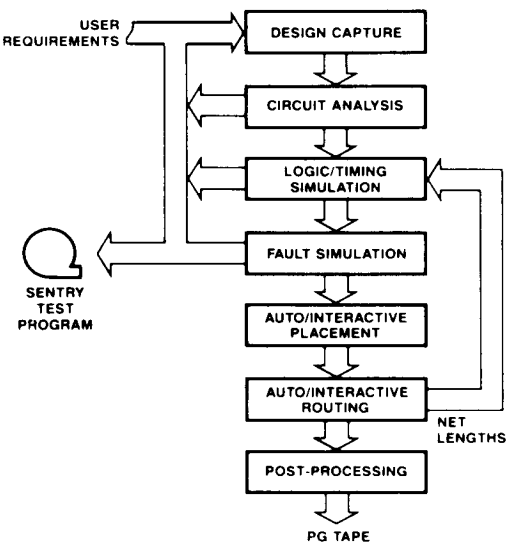
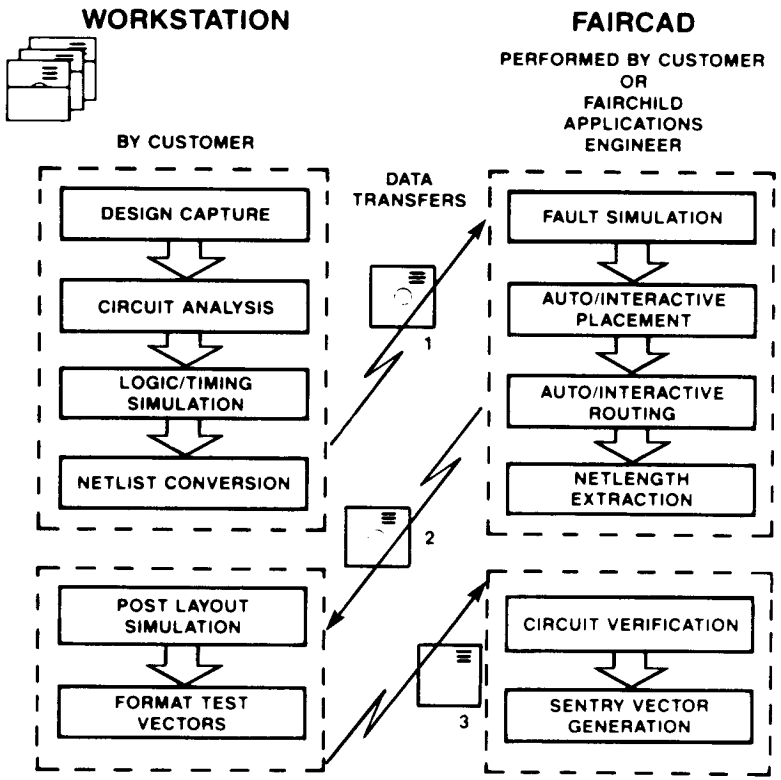


Figure 7-7: Typical Engineering Workstation Design Flow



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