Features

128Kx32 bit CMOS Static
Random Access Memory

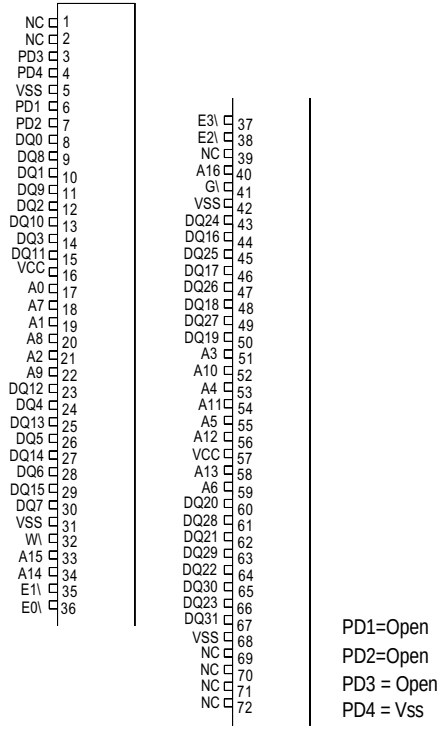
- Access Times
  - BiCMOS: 10 and12ns
  - CMOS: 15, 20, 25ns
- Individual Byte Selects
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Package

- JEDEC Standard Pinouts
- 72 Pad SIMM, No. 405
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram



PD1=Open
PD2=Open
PD3 = Open
PD4 = Vss

128Kx32 Static RAM CMOS, High Speed Module

The EDI8G32130C is a high speed 4 megabit Static RAM module organized as 128K words by 32 bits. This module is constructed from four 128Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables ($\overline{E}$Ø-$\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of enables.

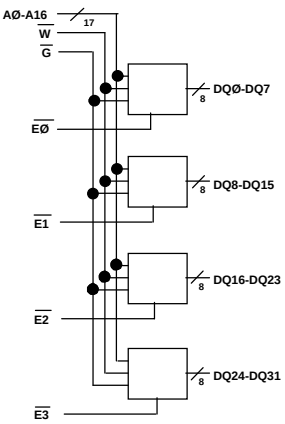
The EDI8G32130C is offered in a 72 Pad SIMM package, which enables four megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Four pins, PD1 to PD4, are used to identify module memory density in applications where alternate modules can be interchanged.

Pin Names

$\overline{A}$Ø-$\overline{A16}$	Address Inputs
$\overline{E}$Ø-E3	Chip Enables
$\overline{W}$	Write Enable
G	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Storage Temperature	-55°C to +125°C
Power Dissipation	4 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle		680	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL or VIN $\geq$ VIH		120	mA
Full Standby Power Supply Current CMOS	ICC3	$\overline{E} \geq$ VCC-0.2V VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V		40	mA
Input Leakage Current	ILI	VIN = 0V to VCC		±20	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		±20	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2/ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Output Deselect	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	45	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	45	pF

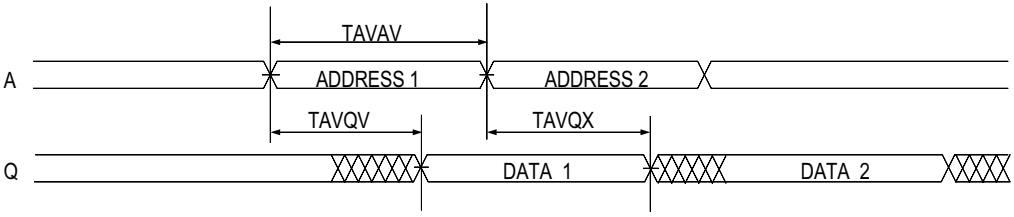
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

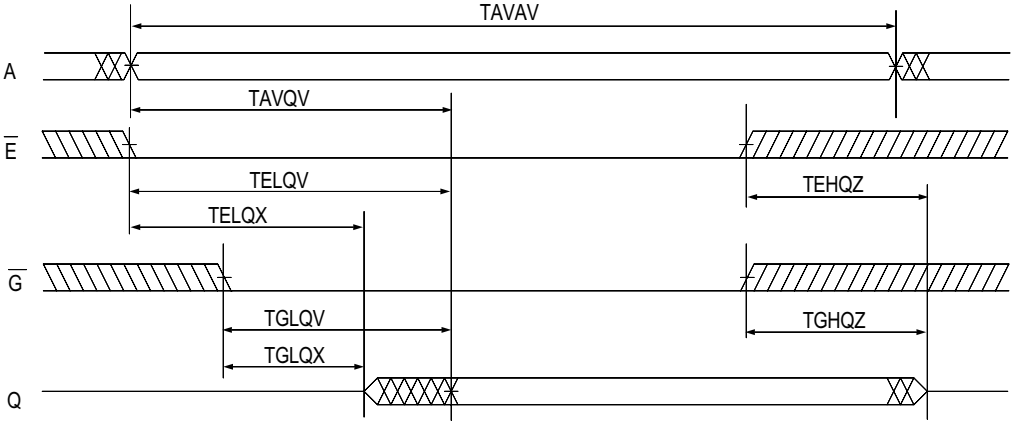
	Symbol		10ns*		12ns*		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	10		12		15		20		25		ns
Address Access Time	TAVQV	TAA		10		12		15		20		25	ns
Chip Enable Access	TELQV	TACS		10		12		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		5		6		8		10		12	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		5		6		13		15	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		4		4		5		8		10	ns

Note 1: Parameter guaranteed, but not tested. *BICMOS

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

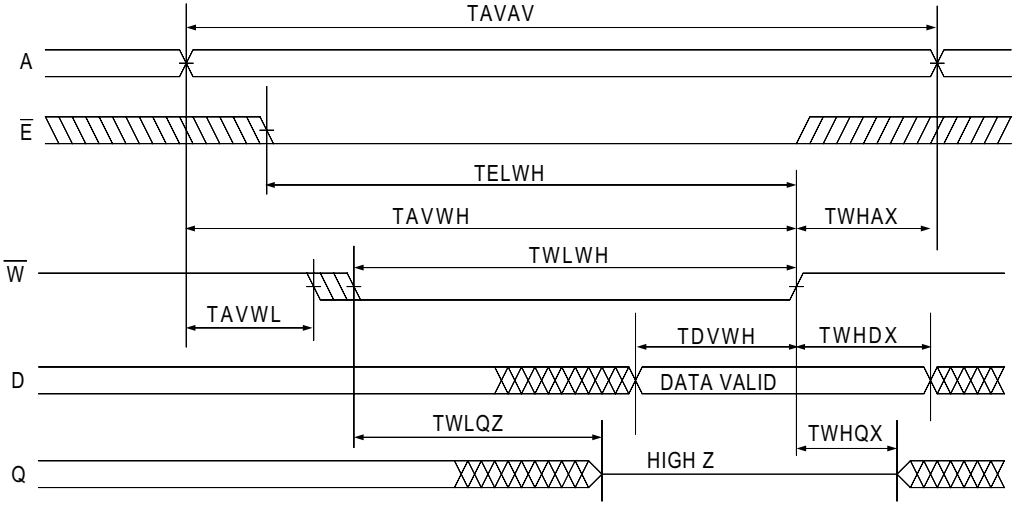


AC Characteristics Write Cycle

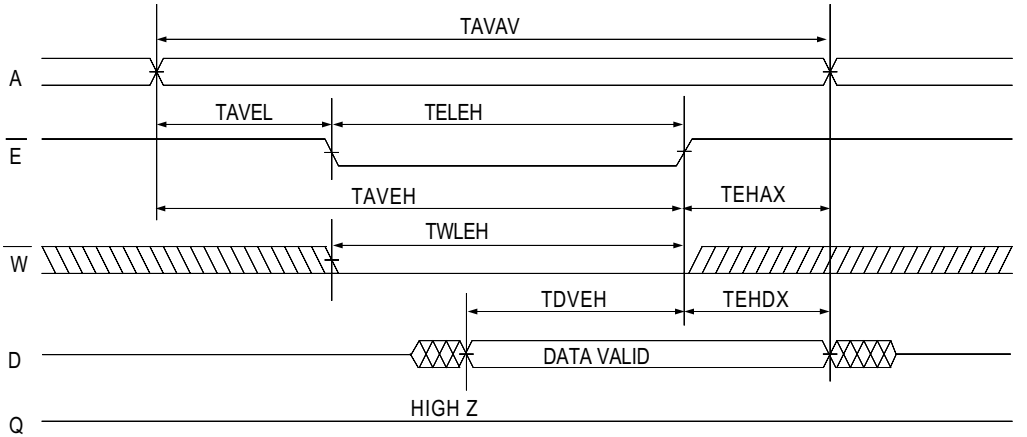
	Symbol		10ns*		12ns*		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	10		12		15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	7		8		10		15		20		ns
	TWLEH	TCW	7		8		10		15		20		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	7		8		10		15		20		ns
	TAVEH	TAW	7		8		10		15		20		ns
Write Pulse Width	TWLWH	TWP	7		8		10		15		20		ns
	TELEH	TWP	7		8		10		15		20		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		3		3		ns
	TEHDX	TDH	3		3		3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	0	7	0	10	0	12	ns
Data to Write Time	TDVWH	TDW	5		6		7		12		15		ns
	TDVEH	TDW	5		6		7		12		15		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		3		3		ns

Note 1: Parameter guaranteed, but not tested. *BICMOS

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\bar{E}$ Controlled



Ordering Information

Part Number	Speed (ns)	Package No.
BiCMOS		
EDI8G32130B10MMC	10	405
EDI8G32130B12MMC	12	405

Part Number	Speed (ns)	Package No.
CMOS		
EDI8G32130C15MMC	15	405
EDI8G32130C20MMC	20	405
EDI8G32130C25MMC	25	405

Package Description

Package No. 405

72 pad SIMM