DS1617/DS3617 Bubble Memory Sense Amplifier

General Description

The DS1617 and the DS3617 are bubble memory sense amplifiers that convert low level signals from magneto-resistive detectors of the bubble memory into TTL compatible output levels. Internal functions consist of an input bias circuit, an internally AC coupled amplifier, a high speed precision comparator, two flip-flops, a TRI-STATE® output stage and a power fail detector.

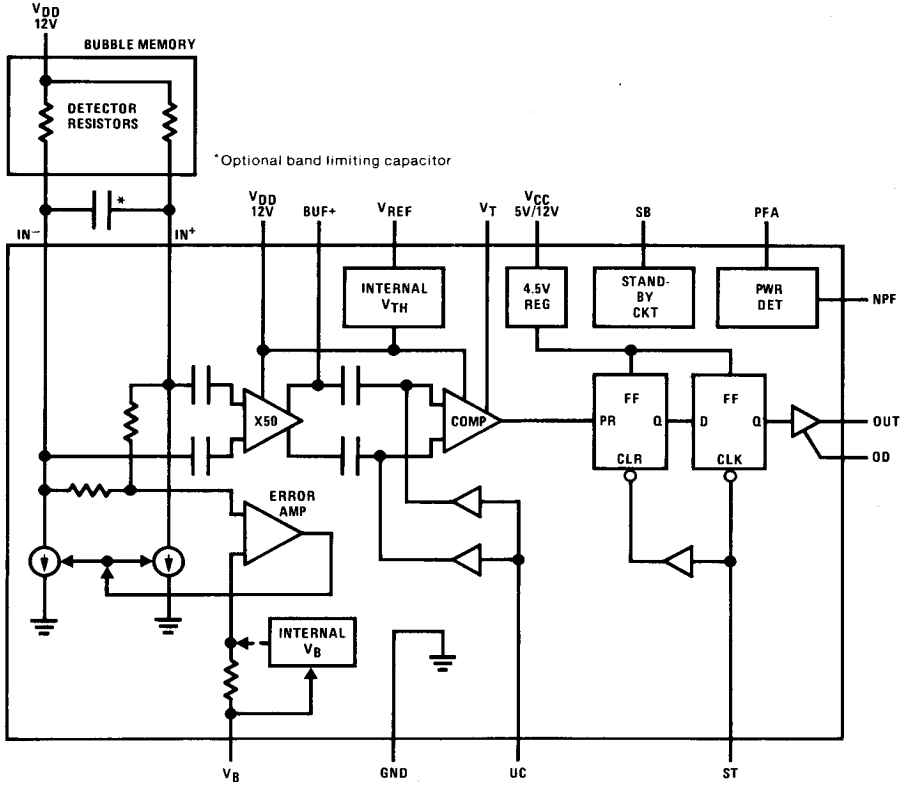
TTL compatible control inputs allow either average-to-peak or the conventional clamp and strobe (peak-to-peak) sensing of the input signal. The threshold voltage and the input bias voltage are externally adjustable allowing compatibility with different types of bubble memories.

Although specifically designed for bubble memory interfacing, they are easily adaptable for any application requiring detection of mV level signals in the 25 kHz to 4 MHz range. Typical application areas include fiber optic receivers, plated wire memory sense amplifiers and pulse discriminators.

Features

- Single 12V or 12V/5V operation
- On-chip adjustable detector bias circuit
- Choice of average-to-peak or clamp and strobe sensing
- Guaranteed tight threshold limits over the specified temperature and supply voltage range
- Threshold externally adjustable over 0 mV to 20 mV range (typical)
- On-chip reference for a 3.2 mV threshold (typical)
- TRI-STATE output
- No offset nulling requirement due to on-chip AC coupling at the input
- Power fail detector with adjustable trip level senses both supplies
- Compatible with a wide range of bubble memories
- Standard 16-pin dual-in-line package

Block Diagram



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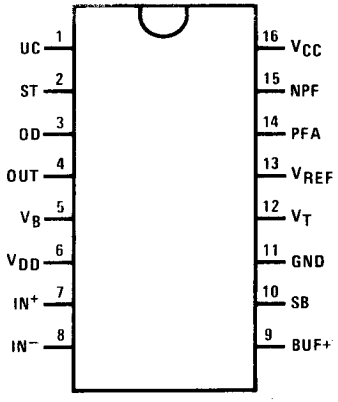
Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS1617J, DS3617J or DS3617N
See NS Package J16A or N16A

Functional Pin Description

ANALOG INPUTS

Differential Analog Inputs (IN^+ and IN^-): These are high impedance inputs for bubble memory detectors. They also provide the bias current to the detectors at a constant DC voltage. The sense-amp threshold is positive with respect to the IN^+ input.

Bias Voltage Input (V_B): When an external DC voltage (between 4V and 8V) is applied to this input, the internal error amplifier will adjust the bias current sources to maintain the average common-mode voltage of IN^+ and IN^- inputs at this value. This input can be connected to V_{DD} to obtain an internally set bias voltage of 7V typical. This voltage is derived on-chip from a resistor divider connected across the V_{DD} supply.

Threshold Adjust Input (V_T): An externally applied DC voltage in the range of 0V to 10V at this input will set the threshold of the sense-amplifier in the 0 mV to 20 mV range. The threshold is linearly related to this voltage.

Power Fail Adjust Input (PFA): The trip voltage of 5V and 12V supplies can be set to a fraction of their nominal values by applying an external reference voltage to this input (see graph). When precise power fail detection is not required this input may be grounded to obtain a trip voltage between 35% and 65% of the nominal supply levels (i.e., 5V and 12V).

ANALOG OUTPUTS

Buffered Bubble Signal Output (BUF+): This is the preamplifier output which is in phase with the IN^+ input. It provides an amplified version of the input differential signal (X25) at a low impedance for monitoring purposes.

Internal Reference for V_T (V_{REF}): This output, when connected to V_T input, provides a threshold of 3.2 mV typical. This voltage is derived on the chip from a potential divider connected across the V_{DD} supply. When V_B is also derived in the same fashion, the threshold will track the amplitude variations of the bubble signal resulting from the V_{DD} supply variations.

DIGITAL INPUTS

Unclamp Input (UC): A logic low level on this input causes clamping of the differential inputs of the comparator to a common voltage. When a logic high level is applied, the inputs are unclamped within a few nanoseconds (5 ns typ). The capacitive coupling of the preamplifier outputs to the inputs of the comparator enables referencing of the threshold to any point on the input waveform by using this input. This pin is shorted to V_{CC} or V_{DD} when the average-to-peak sensing method is used.

Strobe Input (ST): A high-to-low transition of this input causes the transfer of data from an internal latch to the output flip-flop. As long as this input is low the internal latch cannot be set by the comparator. For clamp and strobe sensing, this input can be tied to the unclamp input and used as a single UC/ST control line.

Output Disable (OD): A logic high level at this input causes the data output to go into the high impedance state (TRI-STATE).

Standby Input (SB): When the sense-amp is not in use this input can be used to reduce power consumption. A logic high level applied to this input puts the sense-amp in standby mode and TRI-STATEs the data output pin. The power fail detector circuit is not affected by this input.

DIGITAL OUTPUTS

Data Output (OUT): This output is high for signals crossing the threshold and low for those below the threshold. The data on this pin is valid a short time after the negative transition of the strobe signal and will remain valid until the next negative transition of the strobe signal.

Power Fail Detect Output (NPF): This output goes low when either one or both of the supplies fall below the trip voltage. It will remain low until both of the supplies fall below a minimum level which is 4V for V_{DD} and 2.8V for V_{CC}. It is an open collector output with an internal pull-up of 5 kΩ (typical). The circuit is insensitive to transients on the supplies and will typically reject a 500 ns pulse that goes 1V below the trip voltage.

POWER SUPPLIES

Analog Supply (V_{DD}): 12V.

Digital Supply (V_{CC}): 5V to 12V. This supply is internally regulated to 4.5V and hence can be tied to V_{DD} for single supply operation, but a standard 5V logic supply reduces power consumption and also permits power fail detection of the 5V supply.

Absolute Maximum Ratings (Note 1)

Supply Voltages (V_{DD}, V_{CC})	14V
Input Voltages	
Sense Inputs (IN^+, IN^-)	14V
V_T Input	14V
V_{BIAS} Input (V_B)	14V
Control Inputs (UN, ST, OD, SB)	14V
PFA Input	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1635 mW
Molded Package	1687 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.9 mW/°C above 25°C; derate molded package 13.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
V_{DD} Supply Voltage			
DS1617	10.8	13.2	V
DS3617	11.4	12.6	V
V_{CC} Supply Voltage			
DS1617	4.5	13.2	V
DS3617	4.75	12.6	V
Temperature (T_A)			
DS1617	−55	125	°C
DS3617	0	70	°C
PFA Input Voltage	0	1.5	V
V_{BIAS} Input Voltage (V_B)	0	13.2	V
V_T Input Voltage (V_T) (Threshold Adjust)	−0.25	10	V
Sense Input Common-Mode Voltage (V_{CM})	4	8	V
Input Bias Current (I_B) (Into IN^+ and IN^- Inputs)	0.1	10	mA

DC Electrical Characteristics (Notes 2 and 3)

Parameter			Conditions		Min	Typ	Max	Units
ANALOG INPUTS AND OUTPUTS								
V_{IB}	Input Bias Voltage (at IN^+ and IN^- Inputs)		Internal (Note 4)	I_B in mA	Typ −0.15	0.588 V_{DD} + 0.01 I_B	Typ +0.15	V
			External (Note 5)	I_B in mA	Typ −0.1	V_B + 0.01 I_B	Typ +0.1	
$\Delta V_{IB\,(temp)}$	Input Bias Voltage Variation with Temperature (IN^+ and IN^- Inputs)		I_B = 5 mA					
			−55°C < T_A < 125°C (DS1617)			±10		mV
			0°C < T_A < 70°C (DS3617)			±5		mV
I_{VT}	Input Current for V_T Input		V_T = 0V to 5V			−1	−10	μA
I_{VB}	Input Current for V_B Input		V_B = 4V to 8V			−2	−10	μA
V_{REF}	Internal Reference Voltage				0.98 Typ	0.125 V_{DD}	1.02 Typ	V
$\Delta V_{TP\,(temp)}$ (V_{CC}, V_{DD})	Temperature Variation of Power Fail Threshold		Set by V_{PFA} (See Graphs)					
			−55°C < T_A < 125°C (DS1617)			±0.6		%
			0°C < T_A < 70°C (DS3617)			±0.2		%
DIGITAL OUTPUTS (OUT, NPF)								
V_{OH}	Logical "1" Output Voltage	OUT	OD = 0.8V, SB = 0.8V, I_{OH} = −400 μA		2.4	2.8		V
		NPF	I_{OH} = −100 μA		2.4	3.8		
V_{OL}	Logical "0" Output Voltage	OUT	OD = 0.8V, SB = 0.8V, I_{OL} = 10 mA			0.4	0.5	V
		NPF	V_{CC} = 4V, V_{DD} = 10V, V_{PFA} = 1.5V, I_{OL} = 5 mA			0.35	0.5	
I_{OS}	Output Short Circuit Current		V_O = 0V, V_{CC} = V_{DD} = Max					mA
		OUT	OD = 0.8V, SB = 0.8V		−10	−20	−50	
		NPF	V_{PFA} = 0V		−0.5	−1	−1.5	
I_{OD}	TRI-STATE Output Current	OUT Only	OD = 2.0V, SB = 0.8V or OD = 0.8V, SB = 2.0V	V_O = 0.4V			−100	μA
				V_O = 4.0V			100	
I_{PS}	Output Sink Current on NPF Output During Power Fail		V_O = 0.5V, V_{PFA} = 1.5V	V_{CC} = 0V, V_{DD} = 4V	1	6		mA
				V_{CC} = 2.8V, V_{DD} = 0V	1	6		
CONTROL INPUTS (UC, ST, OD, SB)								
V_{IH}	Logical "1" Input Voltage				2			V
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IH}	Logical "1" Input Current		V_{IN} = 4V				20	μA
I_{IL}	Logical "0" Input Current		V_{IN} = 0.4V				−200	μA
POWER SUPPLY CURRENTS								
I_{DDA}	Active V_{DD} Supply Current		SB = 0.8V			25	45	mA
I_{CCA}	Active V_{CC} Supply Current		SB = 0.8V			10	20	
I_{DDS}	Standby V_{DD} Supply Current		SB = 2.0V			12	25	
I_{CCS}	Standby V_{CC} Supply Current		SB = 2.0V			2	4	

AC Electrical Characteristics (Note 2)

Parameter		Conditions		Min	Typ	Max	Units
SENSE INPUT CHARACTERISTICS							
V_{TH}	Differential Input Threshold Voltage	$V_B = 7V$ See *Figure 5* for Test Waveforms		0.97 × Typ − 0.0005	0.00213 × V_T	1.03 × Typ + 0.0005	V
V_{TR}	Threshold Adjustment Range		DS1617	0 to 8	− 0.5 to 20		mV
			DS3617	0 to 10	− 0.5 to 20		mV
f_{BW}	Preamp Bandwidth	@ ± 3 dB, $V_B = 7V$, $-55°C < T_A < 125°C$			0.025 to 4		MHz
		@ ± 0.1 dB, $V_B = 7V$, $-55°C < T_A < 125°C$			0.1 to 1		MHz
R_{IN}	Differential Input Resistance				150		kΩ
C_{IN}	Differential Input Capacitance				12		pF
$\Delta V_{TH(temp)}$	Threshold Variation with Temperature	$V_{DD} = 12V$	$-55°C < T < 125°C$ (DS1617)		± 0.1		mV
			$0°C < T < 70°C$ (DS3617)		± 0.05		mV
T_{PC}	Effective Time Constant of Preamp AC Couplings	(From Sense Input to Comparator Inputs) UC = 3V			6		µs
T_{CL}	Clamp Circuit Time Constant	(Time Constant Associated with the Comparator Inputs when UC = 3V)			12		µs
TIMING REQUIREMENTS							
t_d	Delay Time, UC or ST Input High to Sense Input High	*Figure 2*		50			ns
t_s	Data Set-Up Time, Sense Input High to UC or ST Input Low	*Figure 2*		100			ns
t_{pwi}	Minimum Input Pulse Width at Threshold	*Figure 2*		100			ns
t_{pws}	Minimum Strobe Pulse Width	*Figure 2*		30			ns
t_{ON}	Power-Up Time from SB Low to Full Operation					100	µs
t_{OFF}	Power-Down Time from SB High to Reduced Power					1	µs
SWITCHING CHARACTERISTICS							
t_P	ST Input Low to Valid Data at the Output	*Figures 1 and 3*, OD = 0.8V, $C_L = 30$ pF, R1 = 5k, R2 = 1k			30	50	ns
TRI-STATE DELAYS FROM OD TO OUT							
t_{LZ}	Output Low to TRI-STATE	*Figures 1 and 4* $C_L = 15$ pF, R1 = 1k, R2 = 1k			15	35	ns
t_{HZ}	Output High to TRI-STATE				15	35	ns
t_{ZL}	Output TRI-STATE to Active Low				15	40	ns
t_{ZH}	Output TRI-STATE to Active High				15	40	ns

Note 1: "Absolute maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" and "Recommended Operating Conditions" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of "Recommended Operating Conditions". All typical values are for $V_{CC} = 12V$, $V_{CC} = 5V$ and $T_A = 25°C$ unless otherwise specified.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: V_B pin tied to V_{DD}.

Note 5: V_B pin connected to the external bias voltage.

Example Threshold Calculations

1. Find external voltage V_T to be applied for a 5 mV typical threshold. What is this tolerance of this threshold?

V_{TH} (typ) = 0.00213 × V_T = 0.005V
Therefore, V_T = 0.005/0.00213 = **2.347V**
V_{TH} (min) = 0.97 × 0.005 − 0.0005 = 4.35 mV
V_{TH} (max) = 1.03 × 0.005 + 0.0005 = 5.65 mV
Hence, **V_{TH} = 5 ± 0.65 mV**
and **Tolerance = ± 0.65 mV**

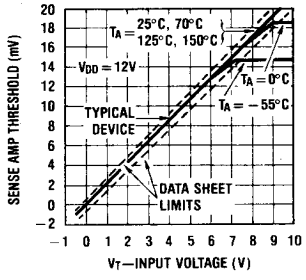
2. Find V_{TH} and its tolerance for V_{DD} = 12V when internal reference (V_{REF}) is used for V_T.

V_T (typ) = V_{REF} (typ) = 0.125 × V_{DD} = 1.5V
V_T (min) = V_{REF} (min) = 0.98 × 1.5 = 1.47V
V_T (max) = V_{REF} (max) = 1.02 × 1.5 = 1.53V
V_{TH} (typ) = 0.00213 × V_T (typ) = 3.20 mV
V_{TH}(min) = 0.97 × 0.00213 × V_T(min) − 0.0005 = 2.54 mV
V_{TH}(max) = 1.03 × 0.00213 × V_T(max) + 0.0005 = 3.86 mV
Hence, **V_{TH} = 3.20 ± 0.66 mV**

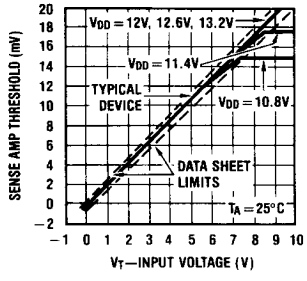
Note. Since V_{REF} is directly related to V_{DD}, the V_{TH} will follow the supply variations. But as long as the input bias voltage V_B is also derived in the same way (i.e., using a potential divider across V_{DD}), the threshold will track the amplitude changes in the bubble detector signal resulting from the V_{DD} supply variations.

Performance Characteristics

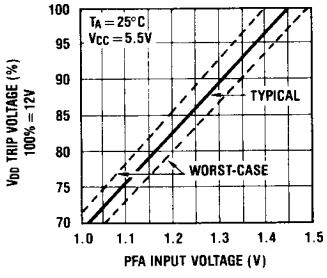
Threshold Transfer Function at Various Temperatures



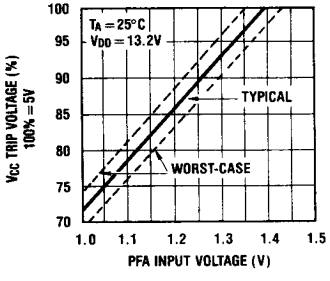
Threshold Transfer Function at Various Supply Voltages



Power Fail Trip Voltage Transfer Function for V_{DD}



Power Fail Trip Voltage Transfer Function for V_{CC}



AC Test Circuit and Switching Time Waveforms

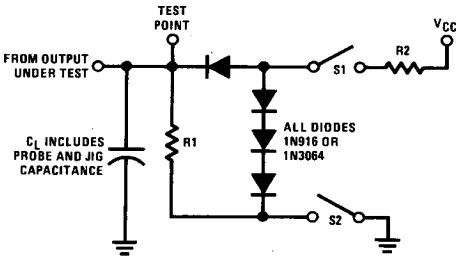
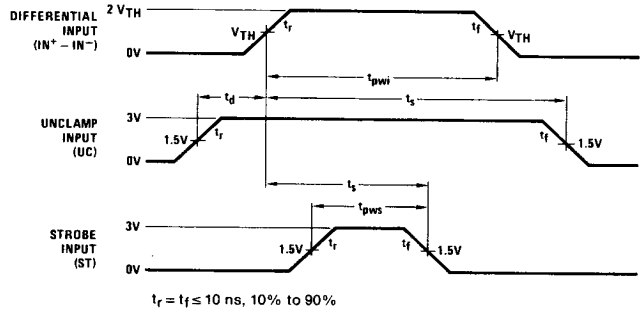


FIGURE 1. Output Load Circuit



$t_r = t_f \leq 10$ ns, 10% to 90%

FIGURE 2. Delay, Set-Up and Hold Times

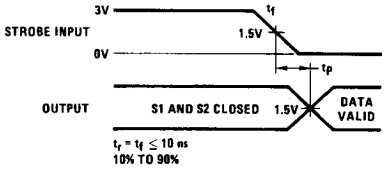
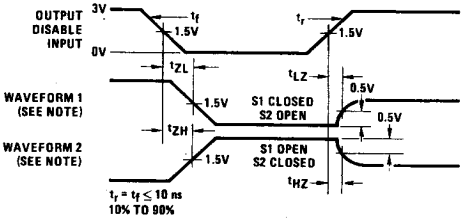
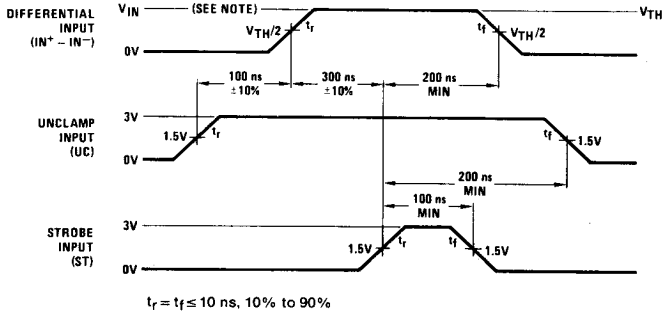


FIGURE 3. Propagation Delay from Strobe Input to Output



Note. Waveform 1 shows the output with internal conditions such that the output is low except when disabled by the output disable input. Waveform 2 shows the output with internal conditions such that the output is high except when disabled by the output disable input.

FIGURE 4. Propagation Delay from Output Disable to Output



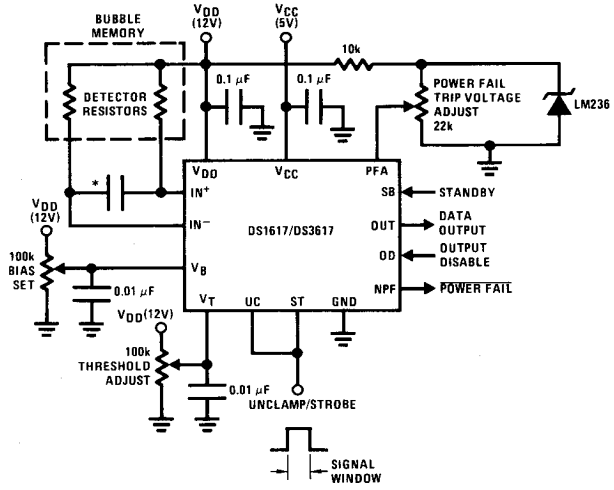
$t_r = t_f \leq 10$ ns, 10% to 90%

Note. To determine the sense amplifier threshold, the input signal amplitude, V_{IN}, is varied around the set threshold value, V_{TH}, while monitoring the OUT pin on a scope. When V_{IN} is close to the threshold, the output will switch between Logic 0 and Logic 1 due to the noise on the input signal. The mid value of the threshold can be determined by adjusting V_{IN} to obtain equal brightness of high (V_{OH}) and low (V_{OL}) level output traces on the scope. In the above set-up, the signal is strobed after a 300 ns delay to allow for any overshoot or transients to settle. This method results in accurate threshold measurement that is relatively independent of input signal rise time. But due to AC coupling of the preamp, with an effective time constant of 6 μs, the signal at the input of the comparator droops by 5% in 300 ns, which has to be accounted for. Hence, $V_{TH} = V_{IN} \times 0.95$.

FIGURE 5. Sense Input Threshold Measurement

Typical Applications

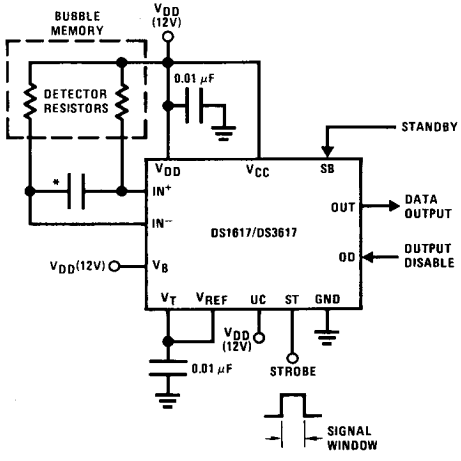
Bubble Memory Sense Amplifier with Adjustable Threshold and Bias Voltage



Note. The control inputs are set up for clamp-strobe or peak-to-peak sensing

*Optional band limiting capacitor

Bubble Memory Sense Amplifier with Internally Set Threshold (3 mV typ) and Input Bias Voltage (7V typ)



Note. The control inputs are set up for average-to-peak sensing

*Optional band limiting capacitor

A General Purpose Precision Sense Amplifier with the Threshold Controlled by an External Reference