.995 714

CT1612 for MIL-STD-1553B

Remote Terminal or Bus Controller Hybrid with Status Word Control

GENERAL DESCRIPTION

The CT1612 design incorporates five LSI chips that accomplish the dual redundant MIL-STD-1553B Bus Controller and Remote Terminal Functions. A sixth LSI chip (CT7100) allows programming of the Terminal Flag and Subsystem Flag Status Bits and allows setting of the Message Error Bit by the Subsystem. The unit dissipates only 75 mW and connects directly to all CTI single and dual transceivers. This CT1612 Data Sheet is designed to be used in conjunction with the CTI MIL-STD-1553B Monolithic Chip Set Booklet, and the CT1561 Data Sheet.

FEATURES

- Performs the complete dual-redundant Remote Terminal and Bus Controller Protocol Functions of MIL-STD-1553B
- Allows setting of the Message Error Bit on illegal commands
- Provides programmable control over Terminal Flag and Subsystem Flag Status Bits
- 75 mW typical power dissipation
- Compatible with all CTI Driver/Receiver Units
- Screened to applicable portions of MIL-STD-883 Level B
- Small size
- Available in plug-in or flatpack configuration
- 5 VDC operation
- -55°C to +125°C operation

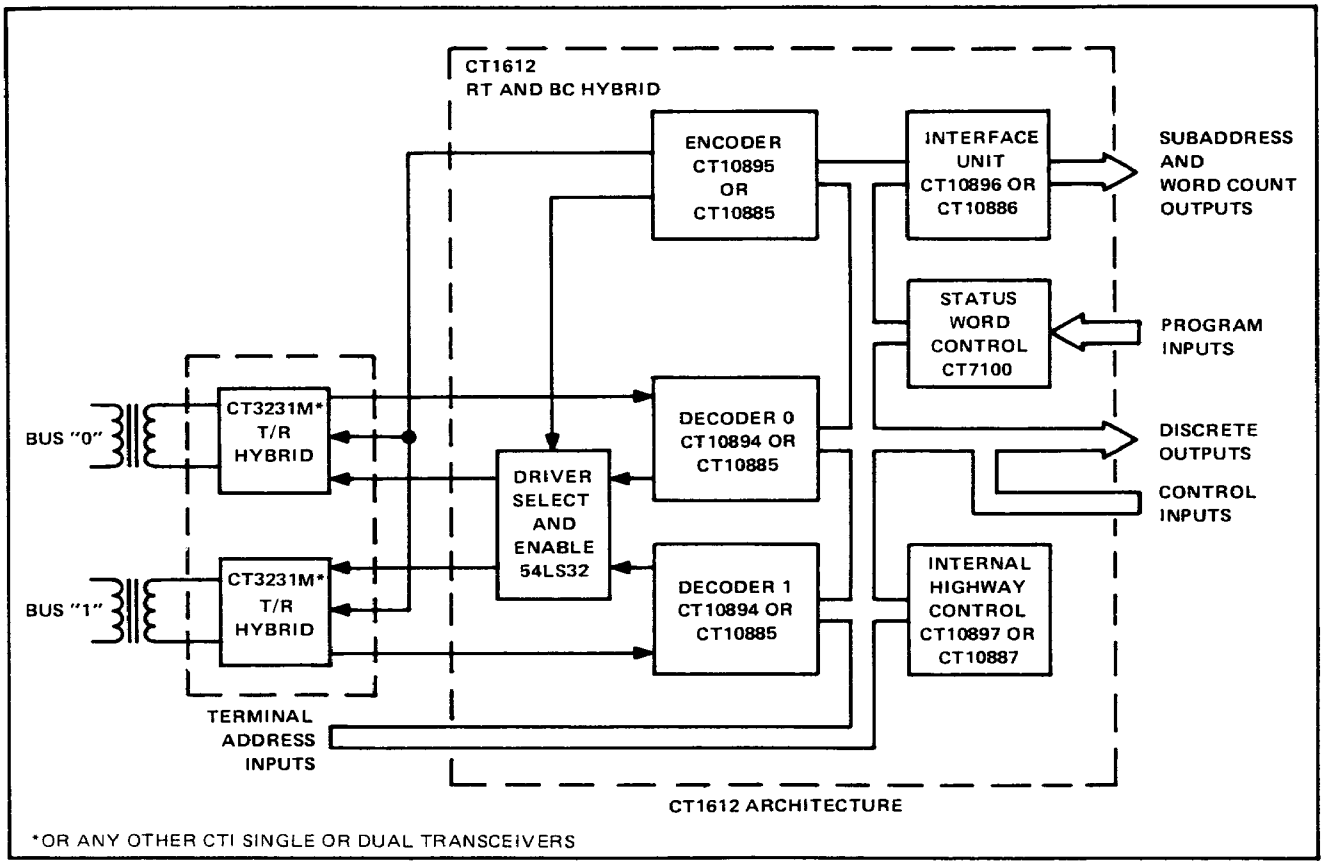

FIGURE 1. FUNCTIONAL DIAGRAM

186 orig

005339

5339 CTI

CIRCUIT TECHNOLOGY INC. 160 Smith St., Farmingdale, NY 11735 516–293–8686 TWX: 510–224–6555 CA: 213–374–7446

CT1612 SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

Supply voltage, V_{CC} 7V
Input voltage 7V
Operating free-air temperature . . . . . -55°C to +125°C
Storage temperature range . . . . . -65°C to +150°C

CLOCK REQUIREMENTS:

Frequency . . . . . 6.0 MHz
Stability -55°C to +125°C . . . . . ±0.01% (100 ppm)
Maximum asymmetry 60-40%
Rise/fall time . . . . . 10 ns max
Output level TTL . . . . . Logic "0" 0.4V max
Logic "1" 2.4V min

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX
Supply voltage V_{CC}	4.5V	5.0V	5.5V
High level output current I_{OH}			
54LS32			-400 μA
CT10894, CT10895, CT10896, CT10897			-0.8mA
Low level output current I_{OL}			
54LS32			4mA
CT10894, CT10895, CT10896, CT10897			2mA

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} high level input voltage	CMOS	V_{CC}-1		V_{CC}	V
	TTL	2.0		V_{CC}	V
V_{IL} low level input voltage	CMOS	0		1.0	V
	TTL	0		0.7	V
V_{OH} high level output voltage	V_{CC} = MIN, I_{OH} = I_{OH} MAX				
	CMOS	V_{CC}-0.5			V
	TTL	2.4			V
V_{OL} low level output voltage	V_{CC} = MAX, I_{OL} = I_{OL} MAX				
	CMOS			0.5	V
	TTL			0.4	V
I_{IL} high level input current	V_{CC} = MAX, V_I = V_{OH} MIN				
	CMOS			5	μA
	TTL			20	μA
I_{IL} low level input current	V_{CC} = MAX, V_I = V_{OL} MAX			-500	μA
I_{CC} supply current	V_{CC} = MAX				
	CMOS			30	mA
	TTL			10	mA

NOTE: All max/min values shown are for worst case operating conditions, where appropriate, at -55°C or +125°C.

REMOTE TERMINAL OPERATION

RECEIVE DATA OPERATION

All valid Data Words associated with a valid Receive Data Command Word for the Remote Terminal (RT) are passed to the subsystem. The RT examines all Command Words from the bus and will respond to valid (i.e. correct Manchester, Parity Coding, etc.) commands which have the correct RT address (or broadcast address if the RT broadcast option is enabled). When the Data Words are received, they are decoded and checked by the RT and, if valid, passed to the subsystem on a word by word basis at 20 μs intervals. This applies to Receive Data Words in both Bus Controller to RT and RT to RT messages. When the RT detects that the message has finished, it checks that the correct number of words has been received and if the message is fully valid, then a Good Block Received signal is sent to the subsystem, which must be used by the subsystem as permission to use the data just received.

The subsystem must therefore have a temporary buffer store up to 32 words long into which these Data Words can be placed. The Good Block Received signal will allow use of the buffer store data once the message has been validated.

If a block of data is not validated, then Good Block Received will not be generated. This may be caused by any sort of message error or by a new valid command for the RT being received on another bus to which the RT must switch.

TRANSMIT DATA OPERATION

If the RT receives a valid Transmit Data Command addressed to the RT, then the RT will request the Data Words from the subsystem for transmission on a word by word basis. To allow maximum time for the subsystem to collect each Data Word, the next word is requested by the RT as soon as the transmission of the current word has commenced.

It is essential that the subsystem should provide all the Data Words requested by the RT once a transmit sequence has been accepted. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

CONTROL OF DATA TRANSFERS

This section describes the detailed operation of the data transfer mechanism between the RT and subsystems. It covers the operations of the signals $\overline{\text{DTRQ}}$, $\overline{\text{DTAK}}$, IUSTB, H/$\overline{\text{L}}$, $\overline{\text{GBR}}$, $\overline{\text{NBGT}}$, and TX/$\overline{\text{RX}}$ during receive data and transmit data transfers.

Figure 6 shows the operation of the data handshaking signals during a Receive Command with two Data Words. When the RT has fully checked the Command Word, $\overline{\text{NBGT}}$ is pulsed low, which can be used by the subsystem as an initialization signal. TX/$\overline{\text{RX}}$ will be set low indicating a Receive Command; however, if $\overline{\text{ENABLE}}$ is held active (low), the TX/$\overline{\text{RX}}$ line will pulse to its opposite state for 80 to 300 ns starting from 100 to 300 ns after the falling edge of $\overline{\text{INCMD}}$, as shown in Figure 12. When the first Data Word has been fully validated, $\overline{\text{DTRQ}}$ is set low. The subsystem must then reply within approximately 1.5 μs by setting $\overline{\text{DTAK}}$ low. This indicates to the RT that the subsystem is ready to accept data. The Data Word is then passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/$\overline{\text{L}}$ as the byte indicator (high byte first followed by low byte). Data is valid about both edges of IUSTB. Signal timing for this handshaking is shown in Figure 11.

If the subsystem does not declare itself busy, then it must respond to $\overline{\text{DTRQ}}$ going low by setting $\overline{\text{DTAK}}$ low within approximately 1.5 μs. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

It should be noted that IUSTB is also used for internal working in the RT. $\overline{\text{DTRQ}}$ being low should be used as an enable for clocking data to the subsystem with IUSTB.

Once the receive data block has finished and been checked by the RT, $\overline{\text{GBR}}$ is pulsed low if the block is entirely correct and valid. This is used by the subsystem as permission to make use of the data block. If no $\overline{\text{GBR}}$ signal is generated, then an error has been detected by the RT and the entire data block is invalid and no Data Words in it may be used.

If the RT is receiving data in an RT to RT transfer, the data handshaking signals will operate in an identical fashion but there will be a delay of approximately 70 μs between $\overline{\text{NBGT}}$ going low and $\overline{\text{DTRQ}}$ first going low. See Figure 9.

Figure 5 shows the operation of the data handshaking signals during Transmit Command with three Data Words. As with the Receive Command discussed previously, $\overline{\text{NBGT}}$ is pulsed low if the command is valid and for the RT. TX/$\overline{\text{RX}}$ will be set high indicating a Transmit Data Command; however, if $\overline{\text{ENABLE}}$ is held active (low), the TX/$\overline{\text{RX}}$ line will pulse to its opposite state for 80 to 300 ns starting from 100 to 300 ns after the falling edge of $\overline{\text{INCMD}}$, as shown in Figure 12. While the RT is transmitting its Status Word, it requests the first Data Word from the subsystem by setting $\overline{\text{DTRQ}}$ low. The subsystem must then reply within approximately 13.5 μs by setting $\overline{\text{DTAK}}$ low. By setting $\overline{\text{DTAK}}$ low, the subsystem is indicating that it has the Data Word ready to pass to the RT. Once $\overline{\text{DTAK}}$ is set low by the subsystem, $\overline{\text{DTRQ}}$ should be used together with H/$\overline{\text{L}}$ and TX/$\overline{\text{RX}}$ to enable first the high byte and then the low byte of the Data Word onto the internal highway IH08-IH715. The RT will latch the data bytes during IUSTB, and will then return $\overline{\text{DTRQ}}$ high. Data for each byte must remain stable until IUSTB has returned low. Signal timing for this handshaking is shown in Figure 10.

ADDITIONAL DATA INFORMATION SIGNALS

At the same time as data transfers take place, a number of information signals are made available to the subsystem. These are $\overline{\text{INCMD}}$, the subaddress lines SA0-SA4, the word count lines WC0-WC4, and current word count lines CWC0-CWC4. Use of these signals is optional.

$\overline{\text{INCMD}}$ will go active low while the RT is servicing a valid command for the RT. The subaddress, Transmit/Receive Bit, and word count from the Command Word are all made available to the subsystem as SA0-SA4, TX/$\overline{\text{RX}}$, and WC0-WC4, respectively. They may be sampled when $\overline{\text{INCMD}}$ goes low and will remain valid while $\overline{\text{INCMD}}$ is low, except as noted for TX/$\overline{\text{RX}}$ in the preceding section.

The subaddress is intended to be used by the subsystem as an address pointer for the data block. Subaddress 0 and 31 are Mode Commands, and there can be no receive or transmit data blocks associated with these. (Any Data Word associated with a Mode Command uses different handshaking operations. If the subsystem does not use all the subaddresses available, then some of the subaddress lines may be ignored.)

The TX/$\overline{\text{RX}}$ signal indicates the direction of data transfer across the RT-subsystem interface. Its use is described in the previous section.

The word count tells the subsystem the number of words to expect to receive or transmit in a message, up to 32 words. A word count of all 0s indicates a count of 32 words.

The current word count is set to 0 at the beginning of a new message and is incremented following each Data Word transfer across the RT-subsystem interface. (It is clocked on the falling edge of the second IUSTB pulse in each word transfer.) There is no need for the subsystem to compare the word count and current word count to validate the number of words in a message. This is done by the RT.

SUBSYSTEM USE OF STATUS BITS AND MODE COMMANDS

General Description

The CT1612 allows full use to be made of all the Status Bits, and also implements all the Mode Commands. Inclusion of the CT7100 array allows external programming of the Terminal Flag and Subsystem Flag Bits plus setting of the Message Error Bit on reception of an illegal command when externally decoded. The subsystem is given the opportunity to make use of Status Bits, and is only involved in Mode Commands which have a direct impact on the subsystem.

The Mode Commands in which the subsystem may be involved are Synchronize, Synchronize with Data Word, Transmit Vector Word, Reset, and Dynamic Bus Control Allocation. The Status Bits to which the subsystem has access, or control are Service Request, Busy, Dynamic Bus Control Acceptance, Terminal Flag, Subsystem Flag, and Message Error Bit. Operation of each of these Mode Commands and of the Status Bits is described in the following sections.

All other Mode Commands are serviced internally by the RT. The Terminal Flag and Message Error Status Bits and BIT Word contents are controlled by the RT; however the subsystem has the option to set the Message Error Bit and to control the reset conditions for the Terminal Flag and Subsystem Flag Bits in the Status Word, and the Transmitter Timeout, Subsystem Handshake, and Loop Test Fail Bits in the BIT Word.

Synchronize Mode Commands

Once the RT has validated the Command Word and checked for the correct address, the $\overline{\text{SYNC}}$ line is set low. The signal WC4 will be set low for Synchronize Mode Command (Figure 15) and high for a Synchronize with Data Word Mode Command (Figure 14). In a Synchronize With Date Word Mode Command, $\overline{\text{SYNC}}$ remains low during the time that the Data Word is received. Once the Data Word has been validated, it is passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/$\overline{\text{L}}$ as the byte indicator (high byte first followed by low byte). $\overline{\text{SYNC}}$ being low should be used on the enable to allow IUSTB to clock Synchronize mode data to the subsystem.

If the subsystem does not need to implement either of these Mode Commands, the $\overline{\text{SYNC}}$ signal can be ignored, since the RT requires no response from the subsystem.

Transmit Vector Word Mode Command

Figure 13 illustrates the relevant signal timings for an RT receiving a valid Transmit Vector Word Mode Command. The RT requests data by setting $\overline{\text{VECTEN}}$ low. The subsystem should use H/$\overline{\text{L}}$ to enable first the high byte and then the low byte of the Vector Word onto the internal highway IH08-IH715.

It should be noted that the RT expects the Vector Word contents to be already prepared in a latch ready for enabling onto the internal highway when $\overline{\text{VECTEN}}$ goes low. If the subsystem has not been designed to handle the Vector Word Mode Command, it will be the fault of the Bus Controller if the RT receives such a command. Since the subsystem is not required to acknowledge the Mode Command, the RT will not be affected in any way by Vector Word circuitry not being implemented in the subsystem. It will however transmit a Data Word as the Vector Word, but this word will have no meaning.

Reset Mode Command

Figure 7 shows the relevant signal timings for an RT receiving a valid Reset Mode Command. Once the command Word has been fully validated and serviced, the $\overline{\text{RESET}}$ signal is pulsed low. This signal may be used as a reset function for subsystem interface circuitry.

Dynamic Bus Allocation

This Mode Command is intended for use with a terminal which has the capability of configuring itself into a Bus Controller on command from the bus. The line $\overline{\text{DBCREQ}}$ cannot go true unless the $\overline{\text{DBCACC}}$ line was true at the time of the valid command (i.e. tied low). For terminals acting only as RTs, the signal $\overline{\text{DBCACC}}$ should be tied high (inactive), and signal $\overline{\text{DBCREQ}}$ should be ignored and left unconnected.

Use of Busy Status Bit

The Busy Bit is used by the subsystem to indicate that it is not ready to handle data transfers either to or from the RT.

The RT sets the bit to logic "1" if the $\overline{\text{BUSY}}$ line from the subsystem is active low at the time of the second falling edge of !NCLK after $\overline{\text{INCMD}}$ goes low. This is shown in Figure 12. Once the Busy Bit is set, the RT will stop all Receive and Transmit Data Word transfers to and from the subsystem. The data transfers in the Synchronize with Data Word and Transmit Vector Word Mode Commands are not affected by the Busy Bit and will take place even if it has been set.

It should be noted that minimum of 0.5 μs subaddress decoding time is given to the subsystem before setting of Status Bits. This allows the subsystem to selectively set the Busy Bit if for instance one subaddress is busy but others are ready. This option will prove useful when an RT is interfacing with multiple subsystems.

Use of Service Request Status Bit

The Service Request Bit is used by the subsystem to indicate to the Bus Controller that an asynchronous service is requested.

The timing of the setting of this bit is the same as the Busy Bit and is shown in Figure 12. Use of $\overline{\text{SERVREQ}}$ has no effect on the RT apart from setting the Service Request Bit.

It should be noted that certain Mode Commands require that the last Status Word be transmitted by the RT instead of the current one, and therefore a currently set Status Bit will not be seen by the Bus Controller. Therefore the user is advised to hold $\overline{\text{SERVREQ}}$ low until the requested service takes place.

Use of the Subsystem Status Bit

This Status Bit is used by the RT to indicate a subsystem fault condition. If the subsystem sets $\overline{\text{SSERR}}$ low, the subsystem fault condition in the RT will be set, and the Subsystem Flag Status Bit will subsequently be set. The fault condition will also be set if a handshaking failure takes place during a data transfer to or from the subsystem. The fault condition is cleared on power-up or by a Reset Mode Command or as described in the Optional Status Word Control section. It should be noted that if $\overline{\text{ENABLE}}$ has been selected (held low) and a subsystem fault is to be reported by pulling $\overline{\text{SSERR}}$ low, then the $\overline{\text{SSERR}}$ line must be latched low until the fault condition no longer exists.

Dynamic Bus Control Acceptance Status Bit

$\overline{\text{DBCACC}}$, when set true, enables an RT to configure itself into a Bus Controller, if the subsystem has the capability, by allowing $\overline{\text{DBCREQ}}$ to pulse true and BIT TIME 18 to be set in the status response. If Dynamic Bus Control is not required, then $\overline{\text{DBCACC}}$ must be tied high. $\overline{\text{DBCACC}}$ tied high inhibits $\overline{\text{DBCREQ}}$ and clears BIT TIME 18 in the status response.

OPTIONAL STATUS WORD CONTROL

Message Error Bit

The CT1612 monitors all receptions for errors and sets the Message Error Bit as prescribed in MIL-STD-1553B. The subsystem designer may, however, exercise the option of monitoring for illegal commands and forcing the Message Error Bit to be set.

The word count and subaddress lines for the current command are valid when $\overline{\text{INCMD}}$ goes low. The subsystem must then determine whether or not the word count or subaddress is to be considered illegal by the RT. If either of them is considered illegal, the subsystem must produce a positive-going pulse called MEREQ. The positive-going edge of MEREQ must occur within 500 ns of the falling edge of $\overline{\text{INCMD}}$.

Subsystem Flag and Terminal Flag Bits

The conditions that cause the Subsystem Flag and Terminal Flag Bits in the Status Word to be reset may be controlled by the subsystem using the $\overline{\text{ENABLE}}$, $\overline{\text{BIT DECODE}}$, $\overline{\text{NEXT STATUS}}$, and $\overline{\text{STATUS UPDATE}}$ inputs. If $\overline{\text{ENABLE}}$ is inactive (high), then the Terminal Flag and Subsystem Flag behavior is the same as described in the CTI MIL-STD-1553B Monolithic Chip Set Booklet (i.e. the other three option lines are disabled). If $\overline{\text{ENABLE}}$ is held low, then the three options described below are available and are essentially independent. Any, all, or none may be selected. Also, reporting of faults by the subsystem requires that $\overline{\text{SSERR}}$ be latched (not pulsed) low until the fault is cleared.

Resetting SSF and TF on Receipt of Valid Commands

If $\overline{\text{ENABLE}}$ is selected and the other three option lines are held high, then the Status Word Register will be reset on receipt of any valid command with the exception of Transmit Status and Transmit Last Command. Note that in this mode, the TF will never be seen in the Status Word, and the SSF will only be seen if $\overline{\text{SSERR}}$ is latched low. Also note that the SSF will not be seen in response to Transmit Status or Transmit Last Command if the preceding Status Word was clear, regardless of actions taken on the $\overline{\text{SSERR}}$ line after the clear status transmission.

Status Register Update at Fault Occurrence

If $\overline{\text{STATUS UPDATE}}$ is selected (held low), then the TF or SSF will appear in response to a Transmit Status or Transmit Last Command issued as the first command after the fault occurs. Any other command (except as noted in the Preserving the BIT Word section) will reset the TF and SSF. Repeated Transmit Status or Transmit Last Command immediately following the fault will continue to show the TF and/or SSF in the Status Word. Note that this behavior may not meet the "letter-of-the spec" as described in MIL-STD-1553B, but is considered the "preferred" behavior by some users.

TF and SSF Reporting in the Next Status Word After the Fault

If $\overline{\text{NEXT STATUS}}$ is selected (held low), then the TF or SSF will appear in response to the very next valid command after the fault except for Transmit Status or Transmit Last Command. The flag(s) will be reset on receipt of any valid command following the status transmission with the flag(s) set except for Transmit Status, Transmit Last Command, or as noted in the following section on Preserving the BIT Word.

Preserving the BIT Word

In order to preserve the Transmitter Timeout Flag, Subsystem Handshake Failure, and Loop Test Failure Bits in the BIT Word, it is necessary to select $\overline{\text{BIT DECODE}}$ (hold it low). This will prevent resetting those bits if the Transmit Bit Word Mode Command immediately follows the fault or follows a Transmit Last Command or Transmit Status immediately following the fault. It will also prevent resetting the TF and SSF Bits in the Status Word. Any other valid commands will cause those BIT Word Bits and the Status Word Bits to be reset.

BUS DRIVER/RECEIVER INTERFACE

Receive Data

The decoder chip requires two TTL signals (PDIN and NDIN) to represent the data coming in from the bus. PDIN should be driven to a logic level "1" when the bus waveform exceeds a specified positive threshold and NDIN should be driven to a logic level "1" when a specified negative threshold is exceeded. During the quiet period on the bus, the signals should be at the same logic level. All the Bus Receivers must be permanently enabled, the selection of the bus in use is done within the chip set.

Transmit Data

The signals generated by the encoder chip ($\overline{\text{PDOUT}}$ and $\overline{\text{NDOUT}}$) are of the same format as the receive data. The only difference is that the TTL signals are negative logic (e.g. the signal is active when on logic level "0"). This means that when the encoder is quiet both $\overline{\text{PDOUT}}$ and $\overline{\text{NDOUT}}$ are at logic level "1". TX INHIBIT 0 and TX INHIBIT 1 enable the appropriate driver when it should be transmitting.

Figure 4 shows an example of a typical interface circuit between CT1612 and a driver/receiver unit.

BUS CONTROLLER OPERATION

To enable its use as a Bus Controller each chip in the chip set has additional logic within it. This logic can be enabled by pulling the pin labeled RT/$\overline{\text{BC}}$ low. Once the chip set is in Bus Control mode, all data transfers must be initiated by the Bus Control processor correctly commanding the chip set via the subsystem interface. In Bus Control mode six inputs are activated which in RT mode are inoperative and four signals with dual functions exercise the second function (the first being for the RT operation).

To use the CT1612 as a 1553B Bus Control interface, the Bus Control processor must be able to carry out four basic bus-related functions. Two inputs (BCOPA and BCOPB) allow these four options to be selected. The option is then initiated by sending a negative-going strobe on the $\overline{\text{BCOPSTB}}$ input. $\overline{\text{BCOPSTB}}$ must only be strobed low when $\overline{\text{NDRQ}}$ is high. This is particularly important when two options are required during a single transfer.

With these options all message types and lengths can be handled. Normal BC/RT exchanges are carried out in the chip set option zero. This is selected by setting BCOPA and BCOPB to a zero and strobing $\overline{\text{BCOPSTB}}$. On receipt of the strobe, the CT1612 loads the Command Word from an external latch using $\overline{\text{CWEN}}$ and H/$\overline{\text{L}}$. The Command Word is transmitted down the bus. The TX/$\overline{\text{RX}}$ Bit is, however, considered by the chip set as being its inverse and so, if a Transmit Command is sent to an RT (Figure 16), the chip set in BC mode believes it has been given a Receive Command. As the RT returns the requested number of Data Words plus its status, the BC chip set carries out a full validation check and passes the data into the subsystem using $\overline{\text{DTRQ}}$, $\overline{\text{DTAK}}$, H/$\overline{\text{L}}$, IUSTB, and CWC as in RT operation. It also supplies $\overline{\text{GBR}}$ at the end of a valid transmission. Conversely, a Receive Command sent down the bus is interpreted by the BC chip set as a Transmit Command, and so the requisite Data Words are added to the Command Word (Figure 17).

For Mode Commands, where a single Command Word is required, option one is selected by strobing $\overline{\text{BCOPSTB}}$ when BCOPA is high and BCOPB is low. On receiving the strobe, the Command Word is loaded from the external latch using $\overline{\text{CWEN}}$ and H/$\overline{\text{L}}$, the correct Sync and Parity Bits are added and the word transmitted (Figure 19). Mode Commands followed by a Data Word require option two. Option two, selected by strobing $\overline{\text{BCOPSTB}}$ while BCOPA is low and BCOPB is high, loads a Data Word via $\overline{\text{DWEN}}$ and H/$\overline{\text{L}}$, adds Sync and Parity, and transmits them to the bus (Figure 20). If the mode code transmitted required the RT to return a Data Word, then selecting option three by strobing $\overline{\text{BCOPSTB}}$ when BCOPA and BCOPB are both

high will identify that Data Word and if validated, output it to the subsystem interface using RMDSTB and H/$\overline{L}$. This allows Data Words resulting from mode codes to be identified differently from ordinary Data Words and routed accordingly (Figure 21). All received Status Words are output to the subsystem interface using STATSTB and H/$\overline{L}$.

In BC option three, if the signal $\overline{PASMON}$ is active, then all data appearing on the selected bus is output to the subsystem using STATSTB for Command and Status Words or RMDSTB for Data Words.

RT to RT transfers require the transmission of two Command Words. A Receive Command to one RT is continguously followed by a Transmit Command to the other RT. This can be achieved by selecting option one followed by option zero for the second command. The strobe ($\overline{BCOPSTB}$) for option zero must be delayed until $\overline{NDRQ}$ has gone low and returned high following the strobe for option one. The RT transmissions are checked and transferred in the subsystem interface to the Bus Controller processor (Figure 18).

NOTE: For all BC operations, BCOPA and BCOPB must remain valid and stable for a minimum of 1 μs following the leading (negative-going) edge of $\overline{BCOPSTB}$.

PIN DESCRIPTION CT1612

SIGNAL MNEMONIC	HYBRID SINK OR SOURCE	SIGNAL DESCRIPTION
BCOPA	SINK	Bus Control Operation A. Least significant bit of the Bus Controller operation select lines.
BCOPB	SINK	Bus Control Operation B. Most significant bit of the Bus Controller operation select lines.
$\overline{\text{BCOPSTB}}$	SINK	Bus Controller Operation Strobe. When functioning as a Bus Controller, a low-going pulse on this line will initiate the selected Bus Controller operation on the requested bus, using BCOPA&B and REQBUSA&B.
BCSTEN 0/1	SINK	Broadcast Enable. When low, the recognition of Broadcast Command is prevented on the specified bus.
$\overline{\text{BIT DECODE}}$	SINK	Built-In Test Decode. When held low, prevents resetting TXTO Bit, HSFAIL Bit, and LTFAIL Bit in the BIT Word (as well as TF and SSF Bits in the Status Word) upon receipt of a Transmit Bit Word Mode Command.
$\overline{\text{BITEN}}$/RMDSTB	SOURCE	Built-In Test Enable/Receive Mode Data Strobe. This line pulses low when servicing a valid and legal Mode Command to transmit the internal BIT Word. This signal is for information only and must not be used to enable data from the subsystem. This line also double pulses high when in the Bus Control mode when mode data is received to be passed to the subsystem and when data is passed to the subsystem during $\overline{\text{PASMON}}$.
$\overline{\text{BUSY}}$	SINK	Busy. This signal should be driven low if the subsystem is not ready to perform a data transfer to or from the chip set.
C/$\overline{\text{D}}$		Command/Data. Internal signal, not available to user.
$\overline{\text{CMSYNC}}$	SOURCE	Command Word Sync. This line goes low if a Command Word Sync and two Manchester Biphase Bits are valid.
CWC0-CWC4	SOURCE	Current Word Count. These five lines define which Data Word in the message is currently being transferred.
$\overline{\text{CWEN}}$		See $\overline{\text{LSTCMD}}$/$\overline{\text{CWEN}}$.
$\overline{\text{DBCACC}}$	SINK	Dynamic Bus Control Accept. This line should be permanently tied low if a subsystem is able to accept control of the bus if offered.
$\overline{\text{DBCREQ}}$	SOURCE	Dynamic Bus Control Request. This line will pulse low when the status reply for a mode code Dynamic Bus Control has finished where the Accept Bit was set.
$\overline{\text{DTAK}}$	SINK	Data Transfer Acknowledge. Should be set low to indicate that the subsystem is ready for the data transfer.
$\overline{\text{DTRQ}}$	SOURCE	Data Transfer Request. Goes low to request a data transfer between the chip set and subsystem. Goes high at end of the transfer.
$\overline{\text{DWEN}}$		See $\overline{\text{VECTEN}}$/$\overline{\text{DWEN}}$.
$\overline{\text{DWSYNC}}$	SOURCE	Data Word Sync. This line goes low if a Data Word Sync and two Manchester Biphase Bits are valid.
$\overline{\text{ENABLE}}$	SINK	Enable. When held low, enables Bit Decode, Next Status, and Status Update program lines.
$\overline{\text{EOT}}$	SOURCE	End of Transmission. Goes low if a valid sync plus two Data Bits do not appear in time to be contiguous with preceding word.

PIN DESCRIPTION CT1612 (Cont.)

SIGNAL MNEMONIC	HYBRID SINK OR SOURCE	SIGNAL DESCRIPTION
$\overline{\text{ERROR}}$	SOURCE	Error. This line latches low if a Manchester or parity error is detected. It is reset by the next $\overline{\text{CMSYNC}}$ (RT mode) and also by $\overline{\text{RTO}}$ in the Bus Control mode.
$\overline{\text{GBR}}$	SOURCE	Good Block Received. Pulses low for 500 ns when a block of data has been received by the chip set and has passed all the validity and error checks.
H/$\overline{\text{L}}$	SOURCE	High/Low. Indicates which byte of data is on the internal highway. Logic level "0" for least significant byte.
$\overline{\text{HSFAIL}}$	SOURCE	Handshake Failure. This line pulses low if the allowable time for $\overline{\text{DTAK}}$ response has been exceeded during the chip set/subsystem data transfer handshaking.
IH08, IH19, IH210, IH311, IH412, IH513, IH614, IH715	SINK/ SOURCE	Internal Highway. Bidirectional 8-bit highway on which 16-bit words are passed in two bytes. IH715 is the most significant bit of each byte, the most significant byte being transferred first. The highway should only be driven by the subsystem when data is to be transferred to the RT.
INCLK	SOURCE	Internal Clock (2 MHz). This is made available for synchronization use by the subsystem if required. However, many of the outputs to the subsystem are asynchronous.
$\overline{\text{INCMD}}$	SOURCE	In Command. Goes low when the RT is servicing a valid command. The subaddress and word count lines are valid while the signal is low.
IUSTB	SOURCE	Interface Unit Strobe. This is a double pulse strobe used to transfer the two bytes of data.
$\overline{\text{LSTCMD}}$/$\overline{\text{CWEN}}$	SOURCE	Last Command/Command Word Enable. This line pulses low when servicing a valid and legal Mode Command to Transmit Last Command. When in RT mode, this line must not be used to enable data from the subsystem. This line also pulses low, when in the Bus Control mode, when a Command Word is required for transmission.
$\overline{\text{LTFAIL}}$	SOURCE	Loop Test Fail. This line goes low if any error in the terminal's own transmitted waveform is detected or if any parity error in the hardwired RT address is detected.
$\overline{\text{MANER}}$	SOURCE	Manchester Error. This line will pulse low if a Manchester error is detected by the decoder.
MEREQ	SINK	Message Error Request. Positive-going edge will cause Message Error Bit in Status Word to be set.
$\overline{\text{NBGT}}$	SOURCE	New Bus Grant. Pulses low whenever a new command is accepted by the chip set.
$\overline{\text{NDRQ}}$	SOURCE	No Data Required. This line goes low if the encoder transmit buffer is full (i.e. another word is going to be transmitted). This signal is for information only and must not be used to enable data from the subsystem.
$\overline{\text{NEXT STAT}}$	SINK	Next Status. When held low, causes TF or SSF to appear in very next Status Word after fault occurrence (except for Transmit Status or Transmit Last Command).
$\overline{\text{PARER}}$	SOURCE	Parity Error. This line will pulse low if a parity error is detected by the decoder.

PIN DESCRIPTION CT1612 (Cont.)

SIGNAL MNEMONIC	HYBRID SINK OR SOURCE	SIGNAL DESCRIPTION
$\overline{\text{PASMON}}$	SINK	Passive Monitor. When functioning as a Bus Controller this line acts as a passive monitor select. The active going edge of this line will cause the REQBUS lines to be latched and that bus, now selected will be monitored so long as $\overline{\text{PASMON}}$ remains low. All traffic on the bus will be handed, after validation, to the subsystem via STATSTB for Status and Commands Words, and RMDSTB for Data Words.
PDIN		Same as RX DATA.
$\overline{\text{PDOUT}}$		Same as TX $\overline{\text{DATA}}$.
REQBUS A	SINK/ SOURCE	Request Bus A. This line, when in RT mode, is the least significant bit of the bus request lines which specify the origin of the command, i.e. they are sources. When in Bus Control mode, these lines are sinks and specify which bus is to be used for the next command.
REQBUS B	SINK/ SOURCE	Request Bus B. Most significant bit of the bus request lines. (See above for description.) Should be held low for BC operation and ignored for RT operation.
$\overline{\text{RESET}}$	SOURCE	Reset. This line pulses low for 500 ns on completion of the servicing of a valid and legal Mode Command to reset the RT.
RMDSTB		See $\overline{\text{BITEN}}$/RMDSTB.
RTAD0-RTAD4	SINK	RT Address Lines. These should be hardwired by the user. RTAD4 is most significant bit.
$\overline{\text{RTADER}}$	SOURCE	Remote Terminal Address Error. This line goes low if an error is detected in the RT address parity of the selected receiver. Any receiver detecting an error in the RT address will turn itself off.
RTADPAR	SINK	RT Address Parity. This must be hardwired by the user to give odd parity.
RT/$\overline{\text{BC}}$	SINK	Remote Terminal/Bus Control. This line, when high, causes the chip set to function as a remote terminal. When low, the chip set functions as a Bus Controller or Passive Monitor.
$\overline{\text{RTO}}$	SOURCE	Reply Time Out. This signal will pulse low whenever quiet bus time has exceeded the reply time for a transmitting terminal. This line is intended for the Bus Controller use.
RX DATA 0/1	SINK	Positive Data In. This should be a TTL description of the positive half of the Manchester code data on the bus. It should be driven to a logic level "1" when a predetermined positive threshold is exceeded on the bus.
RX $\overline{\text{DATA}}$ 0/1	SINK	Negative Data In. This should be a TTL description of the negative half of the Manchester code data on the bus. It should be driven to a logic level "1" when a predetermined negative threshold is exceeded on the bus.
SA0-SA4	SOURCE	Subaddress. These five lines are a label for the data being transferred. Valid when $\overline{\text{INCMD}}$ is low.
$\overline{\text{SERVREQ}}$	SINK	Service Request. This signal should be driven low to request an asynchronous transfer and left low until the transfer has taken place.
$\overline{\text{SSERR}}$	SINK	Subsystem Error. By taking this line low, the subsystem can set the Subsystem Flag in the Status Word.

PIN DESCRIPTION CT1612 (Cont.)

SIGNAL MNEMONIC	HYBRID SINK OR SOURCE	SIGNAL DESCRIPTION
$\overline{\text{STATEN}}$/ STATSTB	SOURCE	Status Enable/Status Strobe. This line pulses low to enable the Status Word onto the internal highway for transmission. When in RT mode, this line must not be used to enable data from the subsystem. This line also double pulses high, when in the Bus Control mode, to strobe received Status Words into the subsystem. When $\overline{\text{PASMON}}$ is true, this line double pulses high for Command and Status Words.
$\overline{\text{STAT UPDATE}}$	SINK	Status Update. When held low, causes TF or SSF to appear in Status Word response to Transmit Status or Transmit Last Command issued immediately after fault occurrence.
$\overline{\text{SYNC}}$	SOURCE	Synchronize. Goes low when a Synchronize mode code is being serviced.
TREQ		Internal signal, not available to user.
TX DATA	SOURCE	Positive Data Out. When this signal goes high, the bus should be driven positive.
TX $\overline{\text{DATA}}$	SOURCE	Negative Data Out. When this signal goes high, the bus should be driven negative.
$\overline{\text{TXEN}}$		Transmitter Enable. Goes to a logic "0" when transmitting. Used to enable the bus drivers via TX INHIBIT. Internal signal, not available to user.
TX INHIBIT 0/1	SOURCE	Transmitter Enable. Goes low when the transmitter is transmitting. Should be used to enable the bus drivers.
TX/$\overline{\text{RX}}$	SOURCE	Transmit/Receive. The state of this line informs the subsystem whether it is to transmit or receive data. The signal is valid while $\overline{\text{INCMD}}$ is low.
$\overline{\text{TXTO}}$	SOURCE	Transmitter Time Out. This line goes low if the transmitter time out limits are exceeded.
$\overline{\text{VALC}}$		Valid Command. Internal signal, not available to user.
$\overline{\text{VALD}}$	SOURCE	Valid Data. This line will pulse low when a valid Data Word is received.
$\overline{\text{VECTEN}}$/ $\overline{\text{DWEN}}$	SOURCE	Vector Word Enable/Data Word Enable. In the RT mode, this signal is provided to enable the contents of the Vector Word latch (which is situated in the subsystem) onto the chip set's internal highway. This signal, when in the Bus Controller mode, is used to enable mode code data from the subsystem onto the internal highway.
WC0-WC4	SOURCE	Word Count. These five lines specify the requested number of Data Words to be received or transmitted. Valid when $\overline{\text{INCMD}}$ is low.
6 MCK	SINK	6 MHz Master Clock

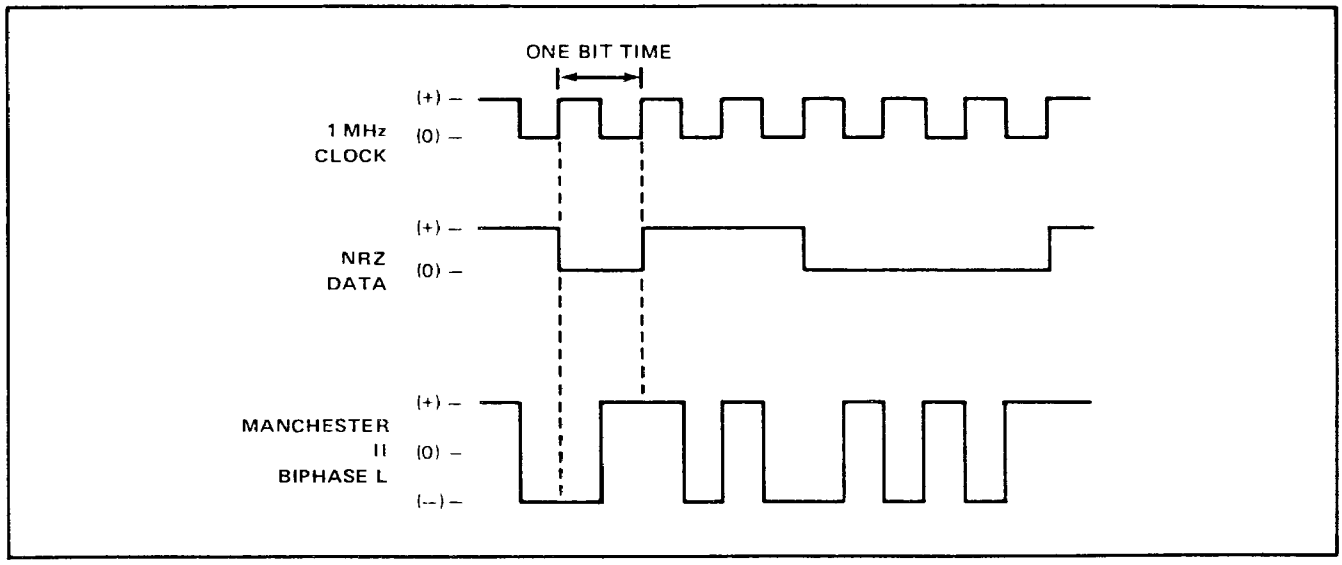

FIGURE 2. DATA ENCODING

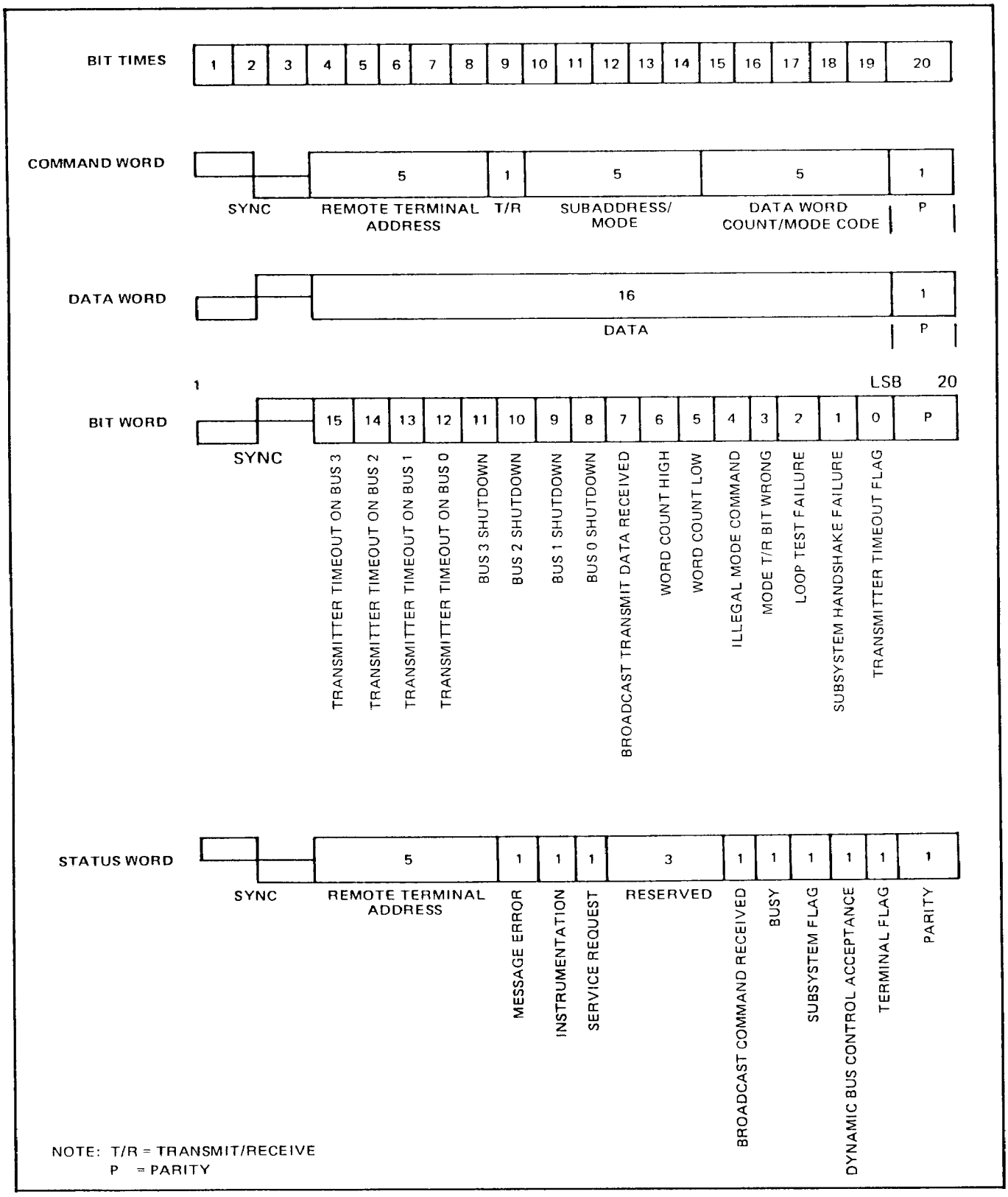

FIGURE 3. WORD FORMATS

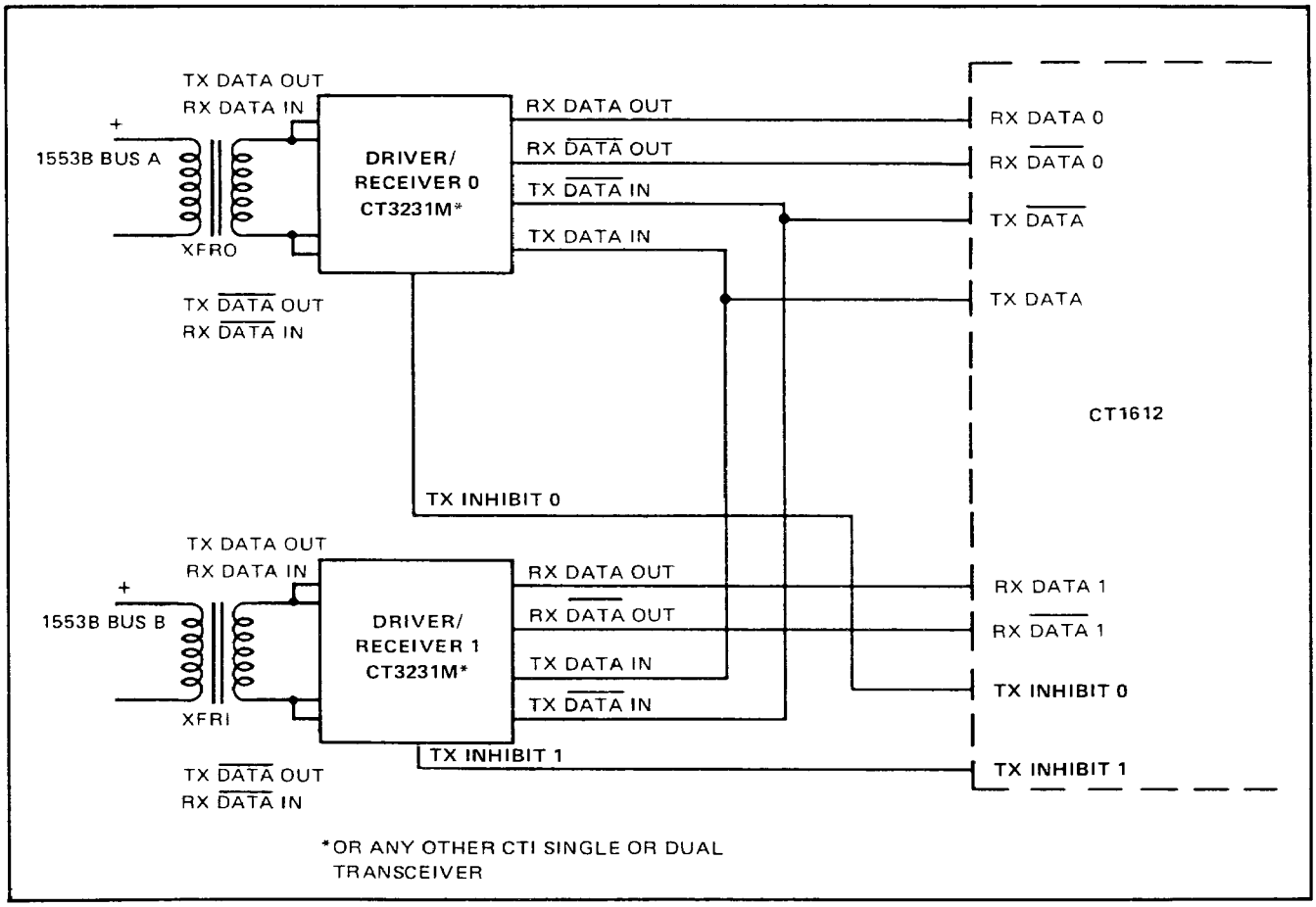

FIGURE 4. EXAMPLE OF AN INTERFACE BETWEEN CT1612 AND DRIVER/RECEIVER

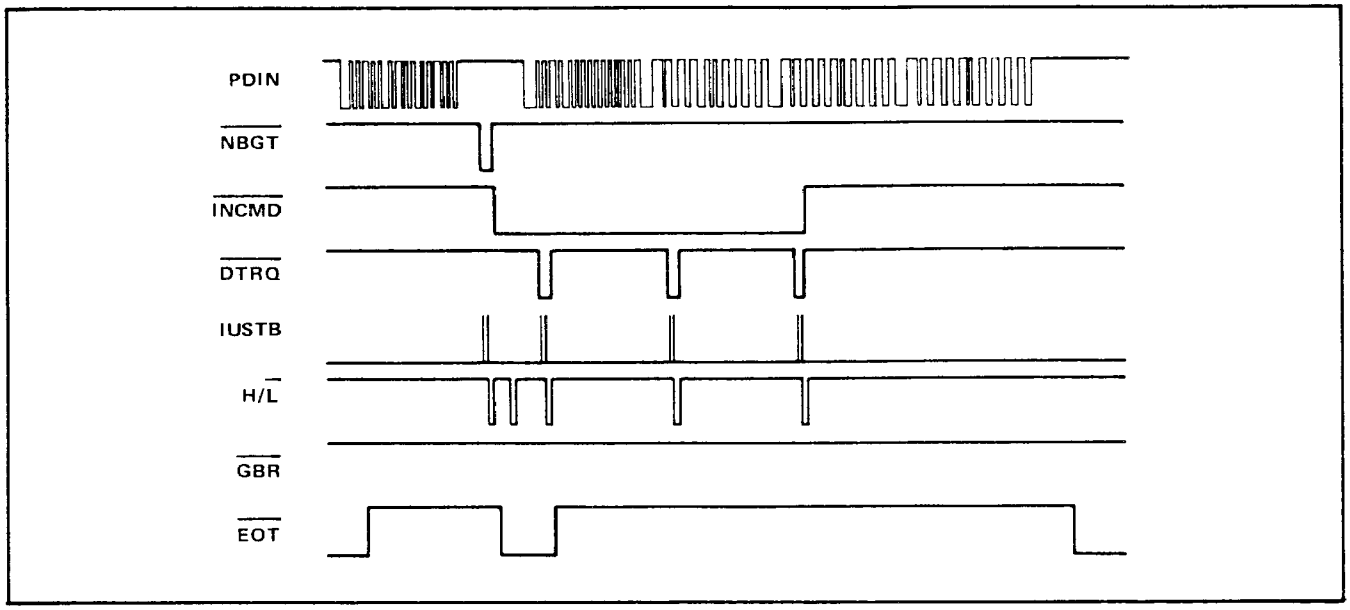

FIGURE 5. TRANSFER OF THREE DATA WORDS FROM RT 03 TO BC

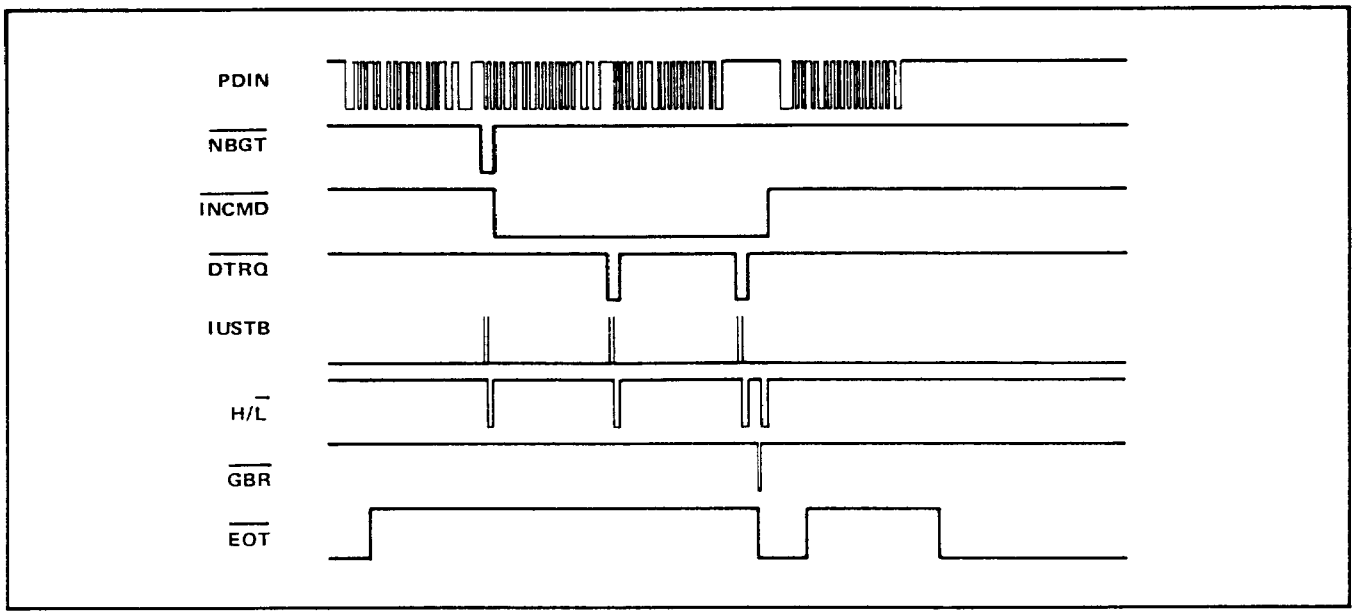

FIGURE 6. TRANSFER OF TWO DATA WORDS FROM BC TO RT 03

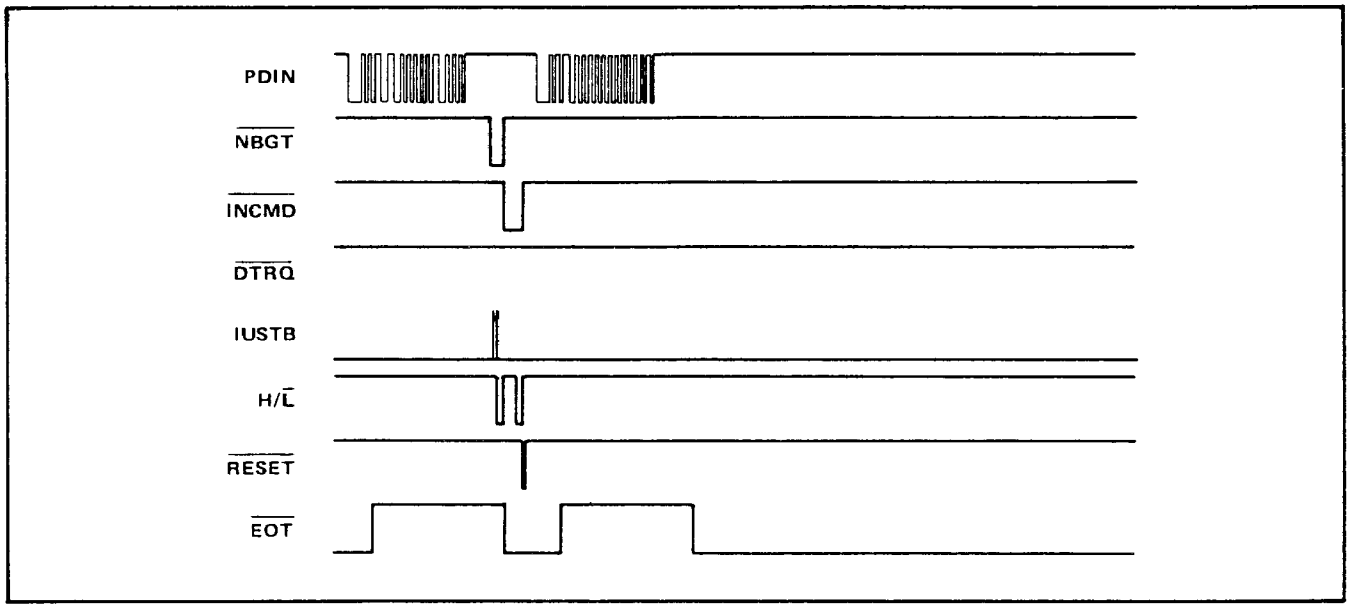

FIGURE 7. MODE COMMAND RESET REMOTE TERMINAL

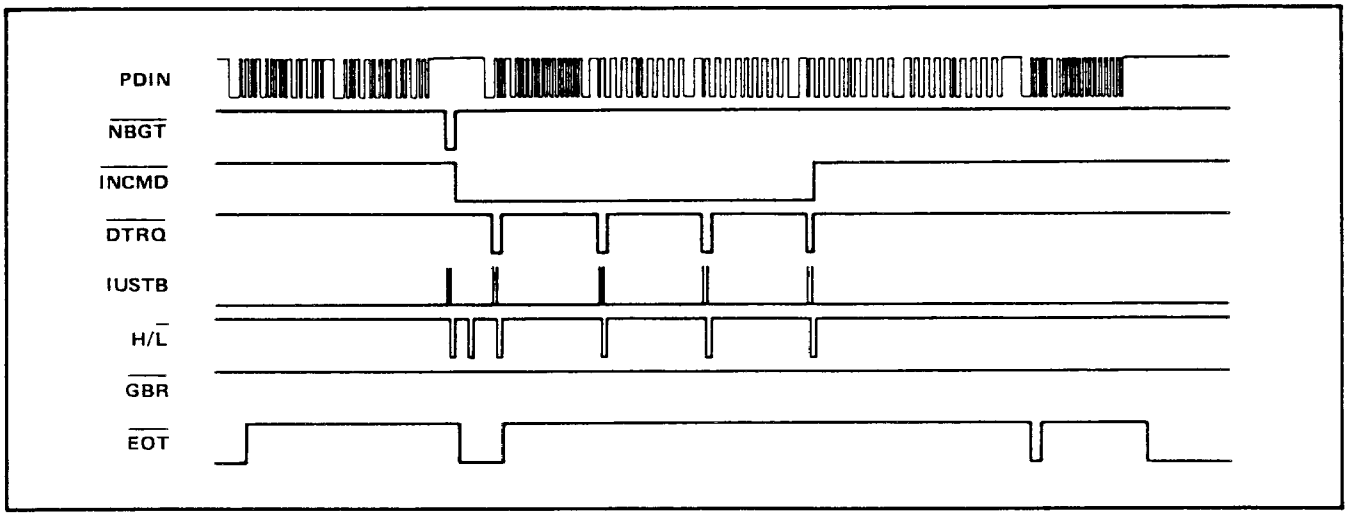

FIGURE 8. RT TO RT TRANSFER OF FOUR DATA WORDS (THIS RT SENDING DATA)

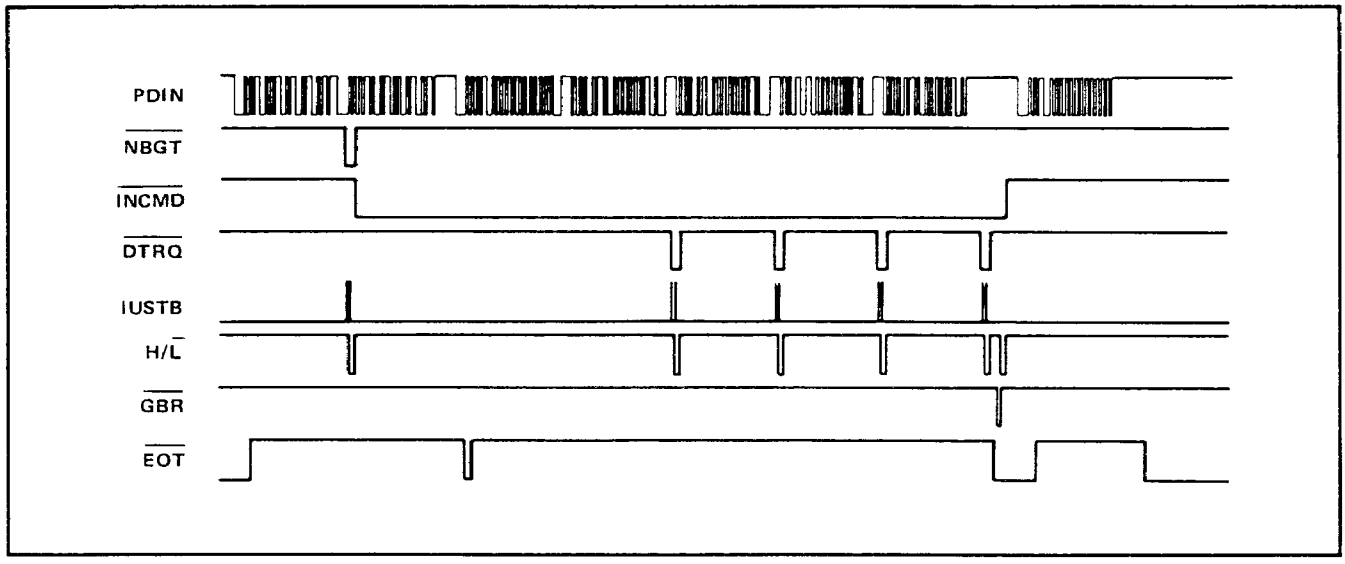

FIGURE 9. RT TO RT TRANSFER OF FOUR DATA WORDS (THIS RT RECEIVING DATA)

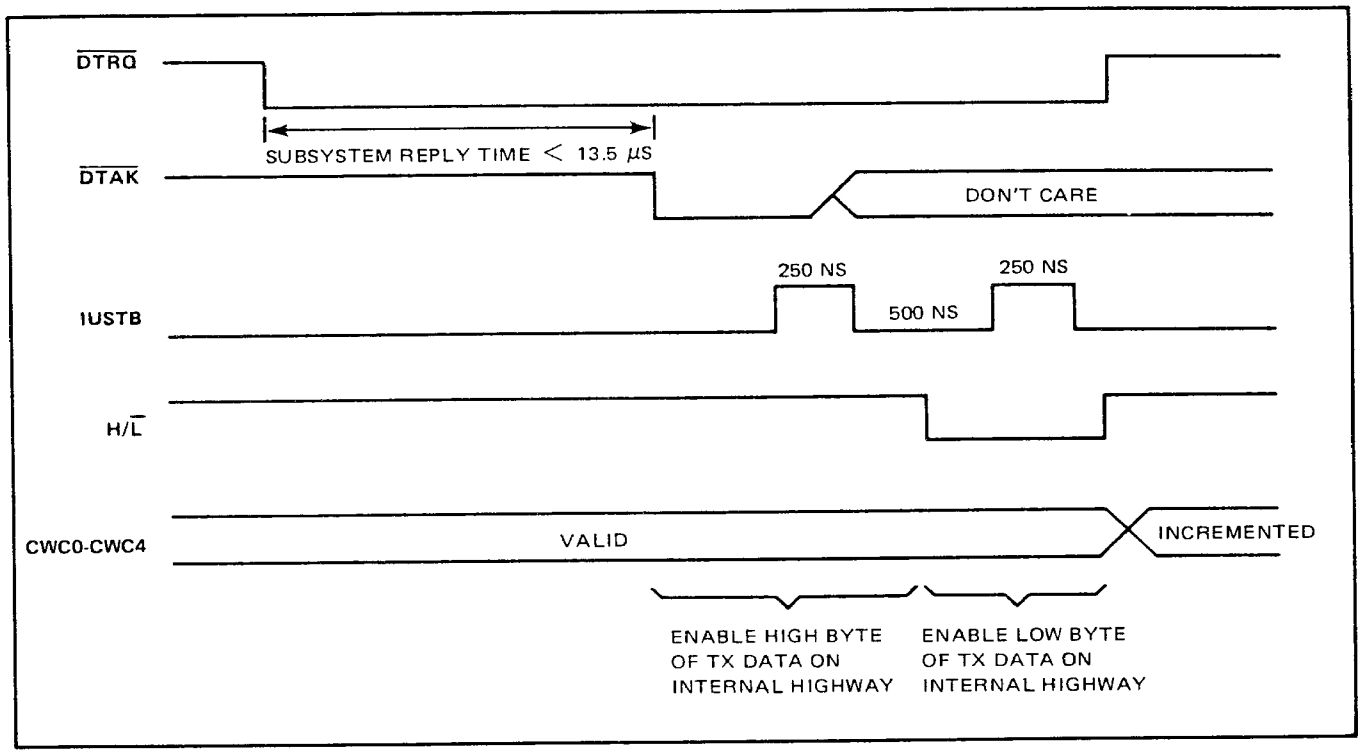

FIGURE 10. HANDSHAKING FOR TX DATA TRANSFERS

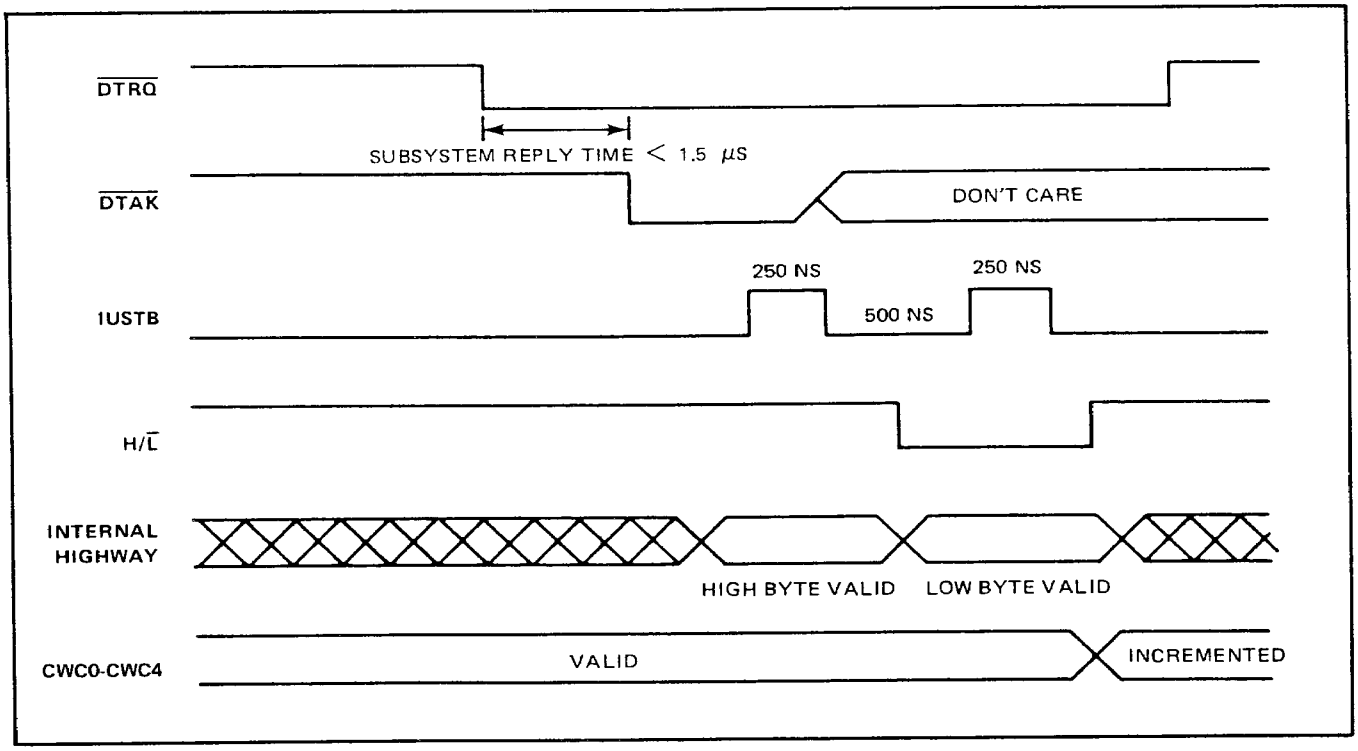

FIGURE 11. HANDSHAKING FOR RX DATA TRANSFERS

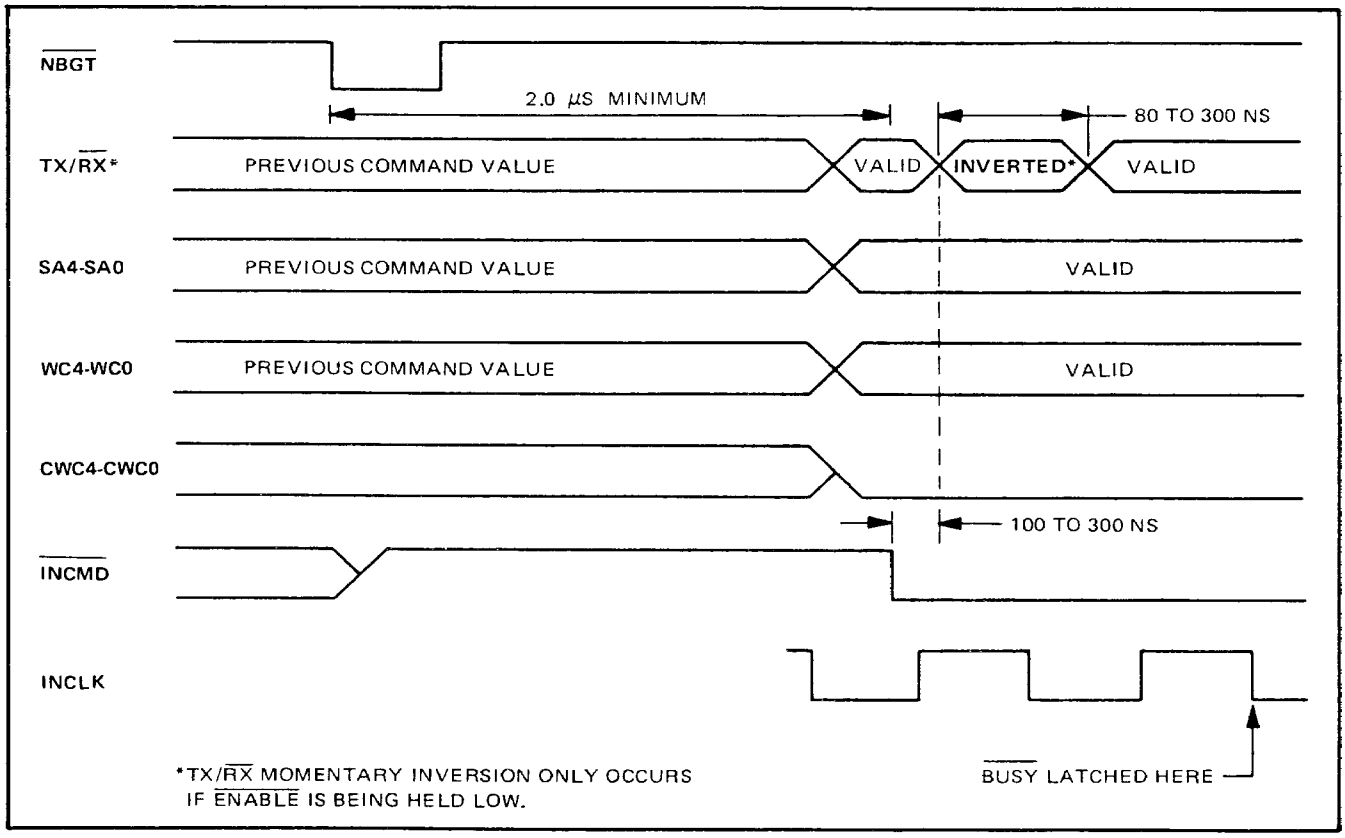

FIGURE 12. NEW COMMAND INITIALIZATION

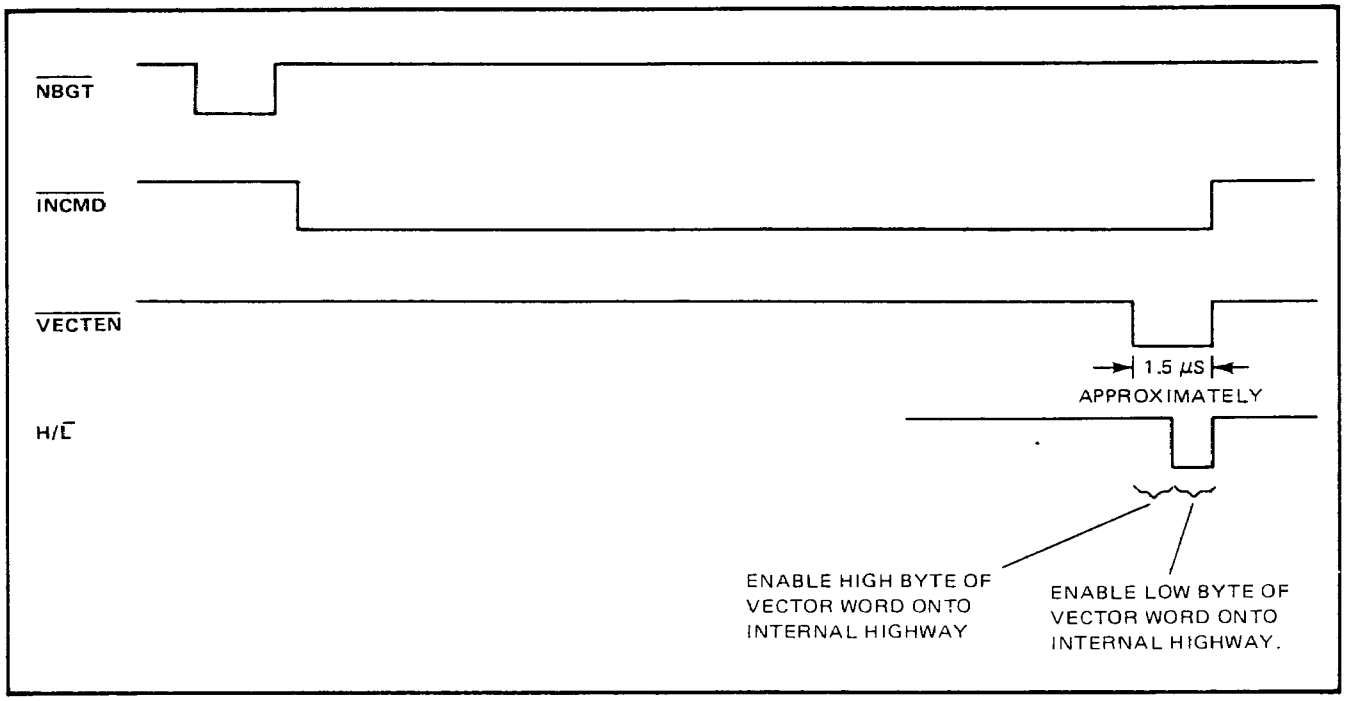

FIGURE 13. TRANSMIT VECTOR WORD MODE COMMAND

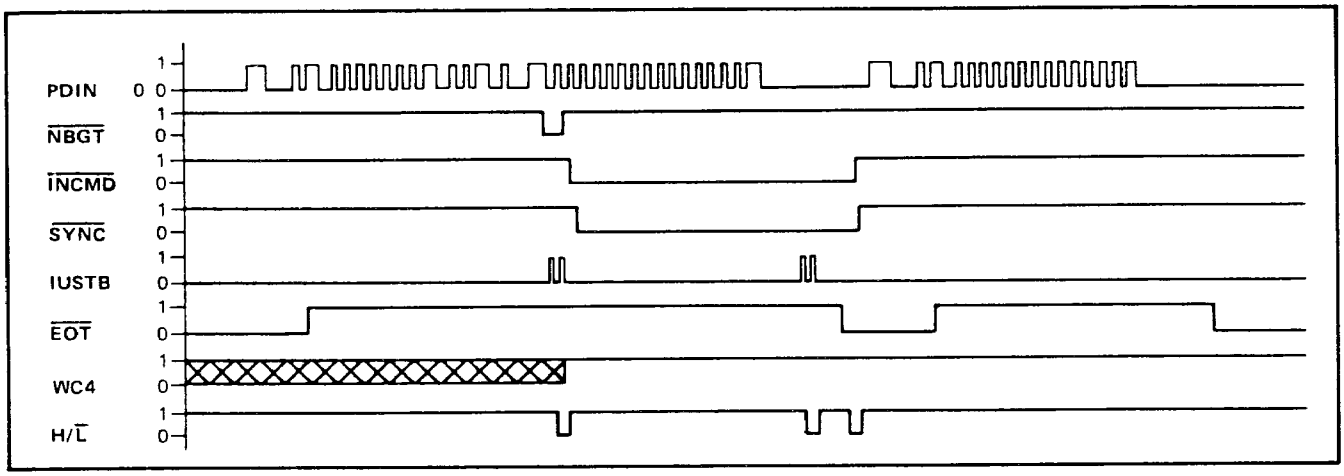

FIGURE 14. SYNCHRONIZE (WITH DATA) MODE COMMAND

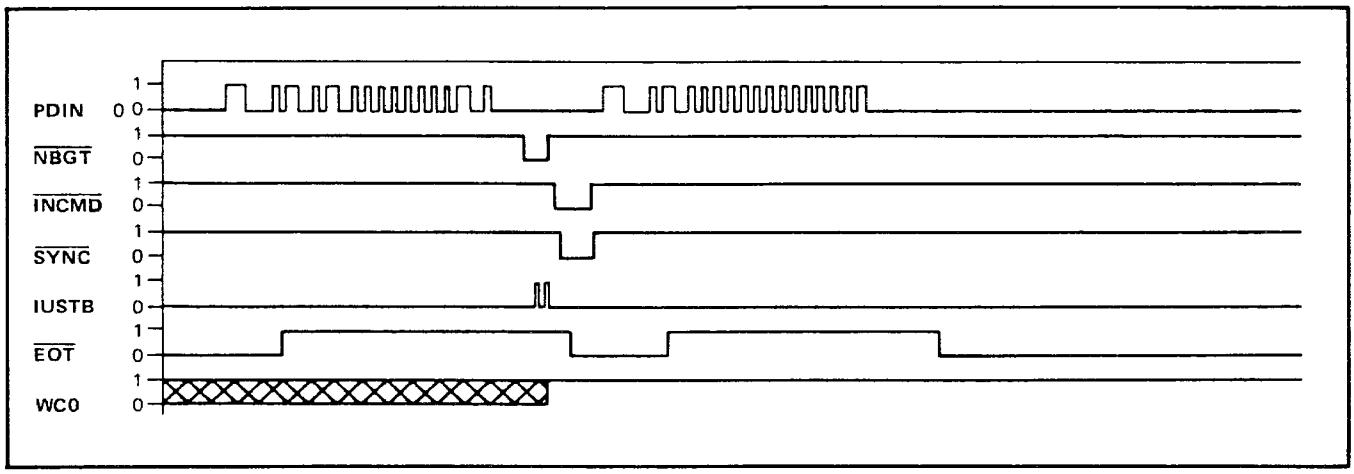

FIGURE 15. SYNCHRONIZE (NO DATA) MODE COMMAND

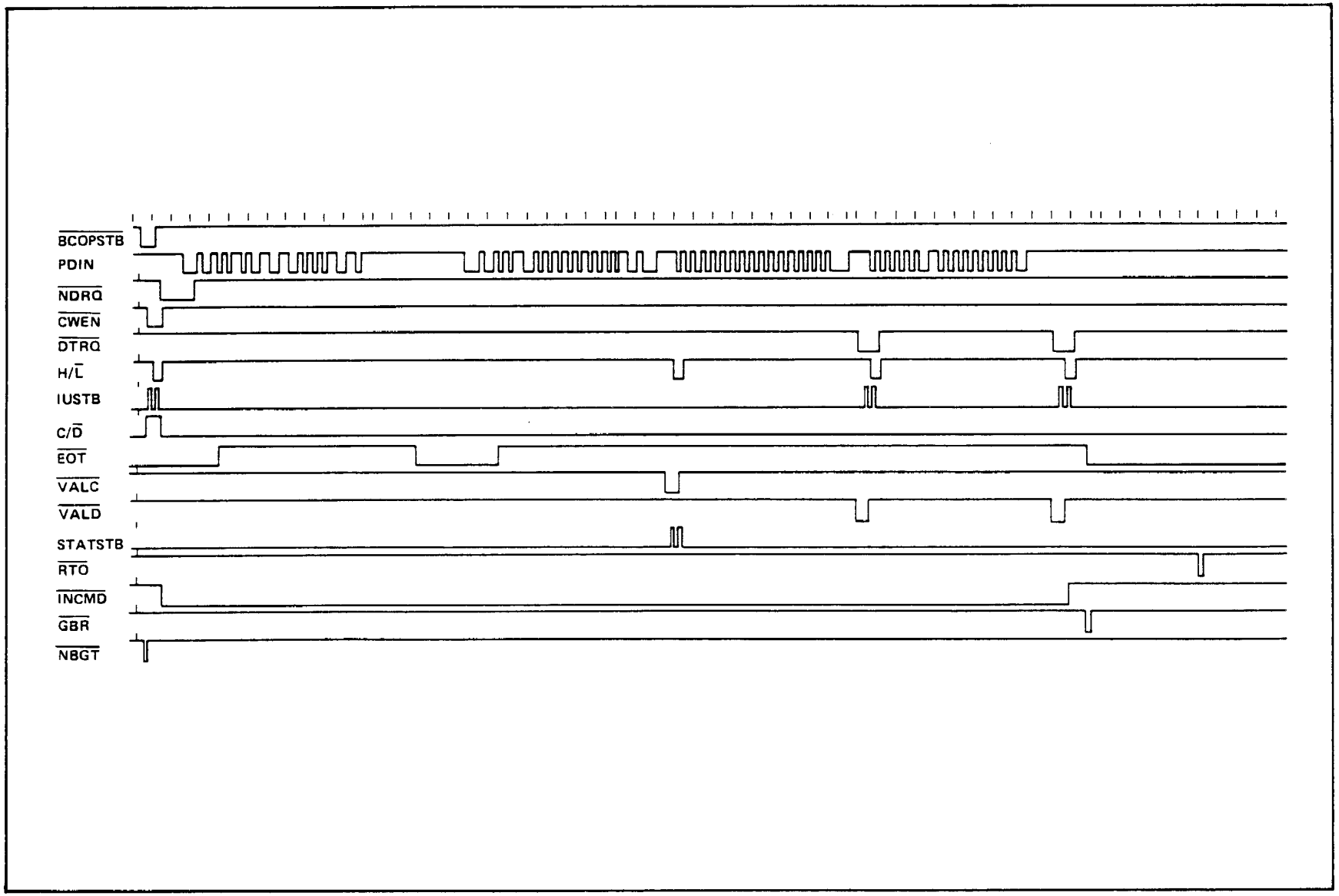

FIGURE 16. BUS CONTROLLER SENDING COMMAND TO RT 10001 TO TRANSMIT TWO DATA WORDS

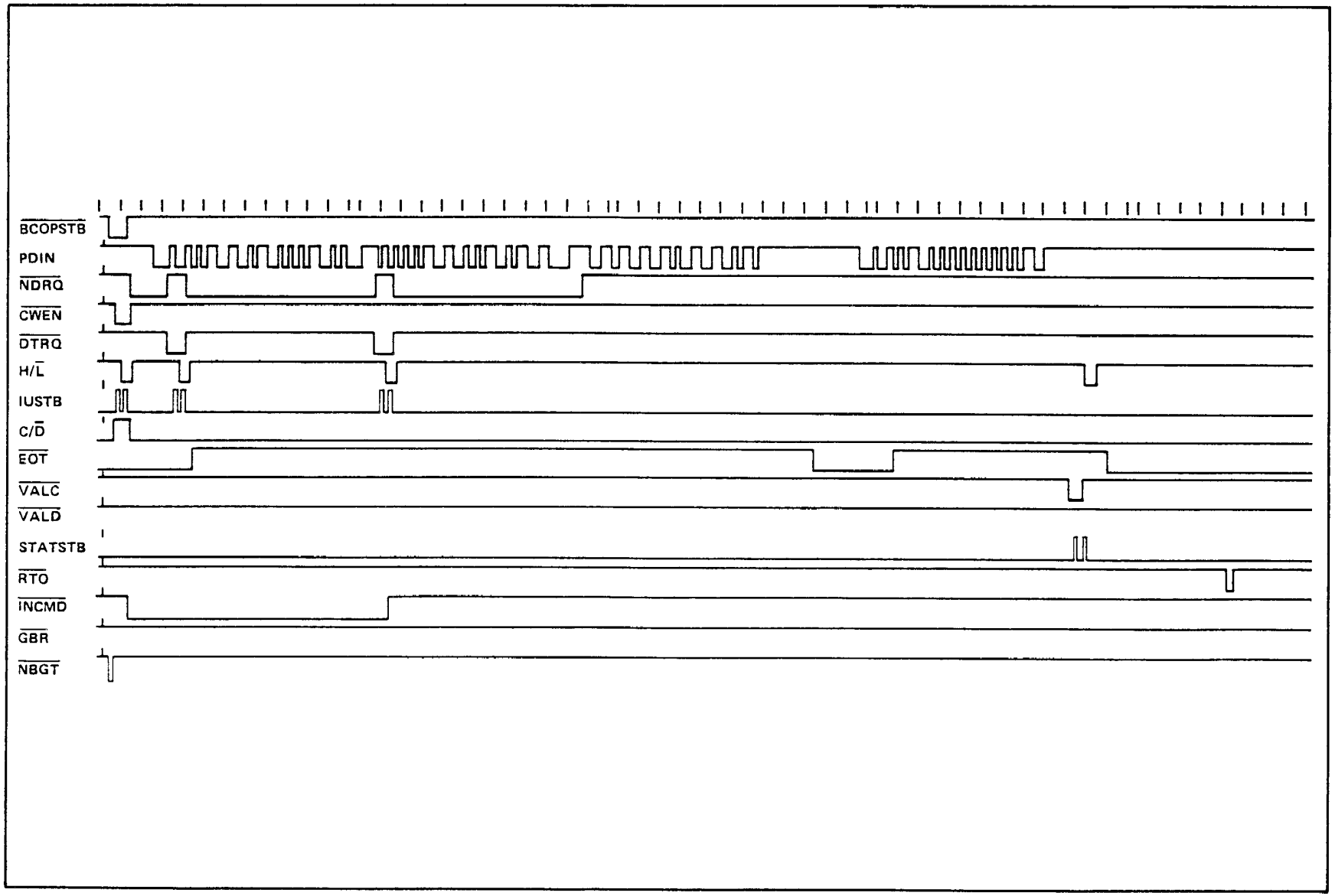

FIGURE 17. BUS CONTROLLER SENDING COMMAND TO RT 10001 TO RECEIVE TWO DATA WORDS

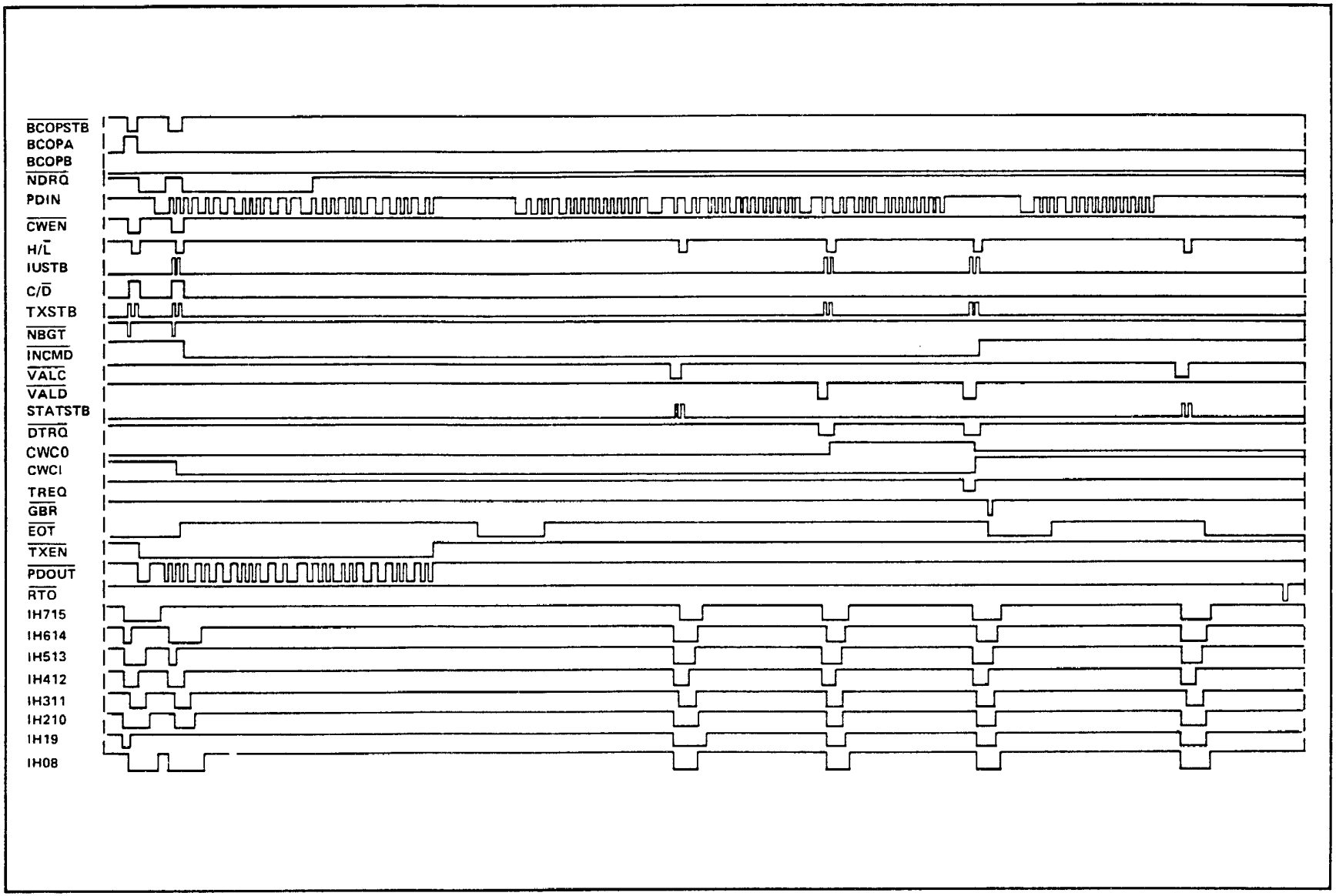

FIGURE 18. BUS CONTROLLER COMMANDING RT 10001 TO TRANSMIT TWO DATA WORDS TO RT 00001

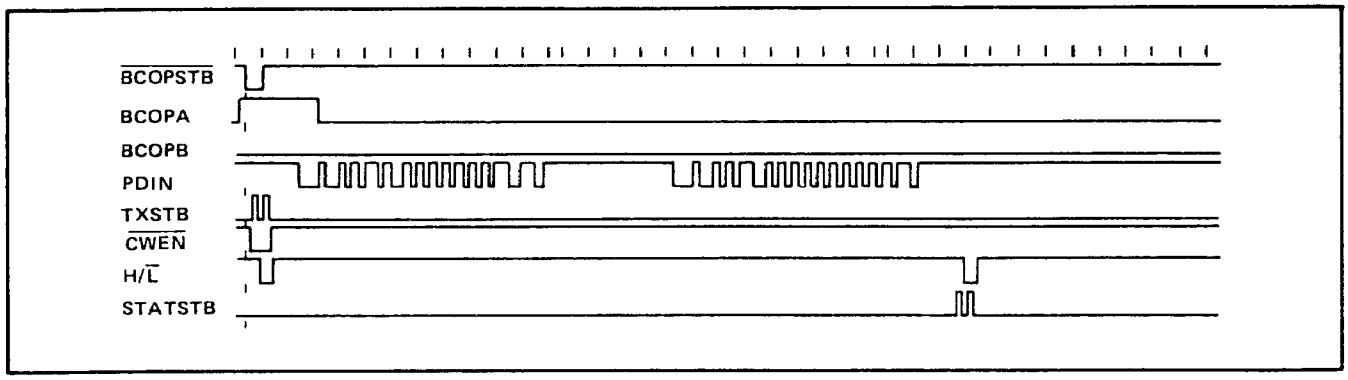

FIGURE 19. BUS CONTROLLER SENDING MODE COMMAND TRANSMIT STATUS WORD MODE CODE 00010

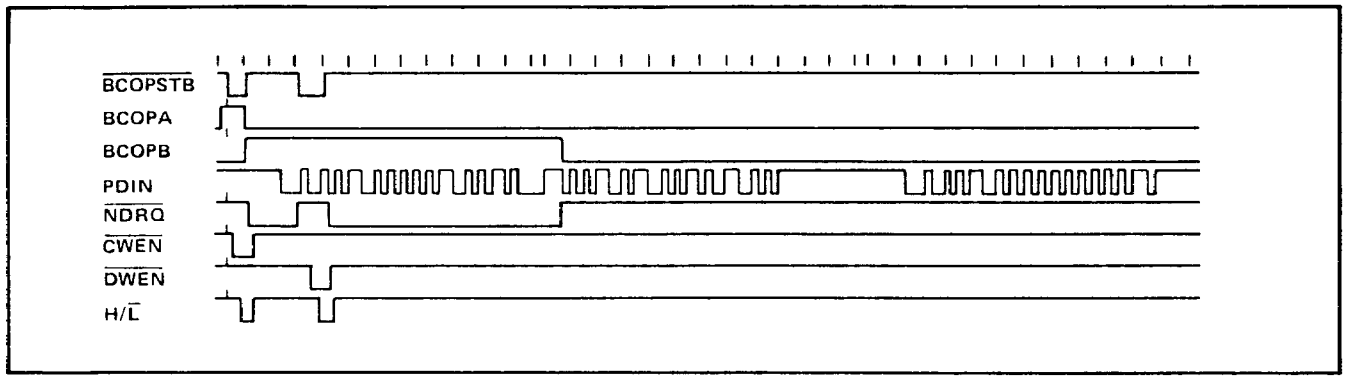

FIGURE 20. BUS CONTROLLER SENDING MODE COMMAND SYNCHRONIZE MODE CODE 10001

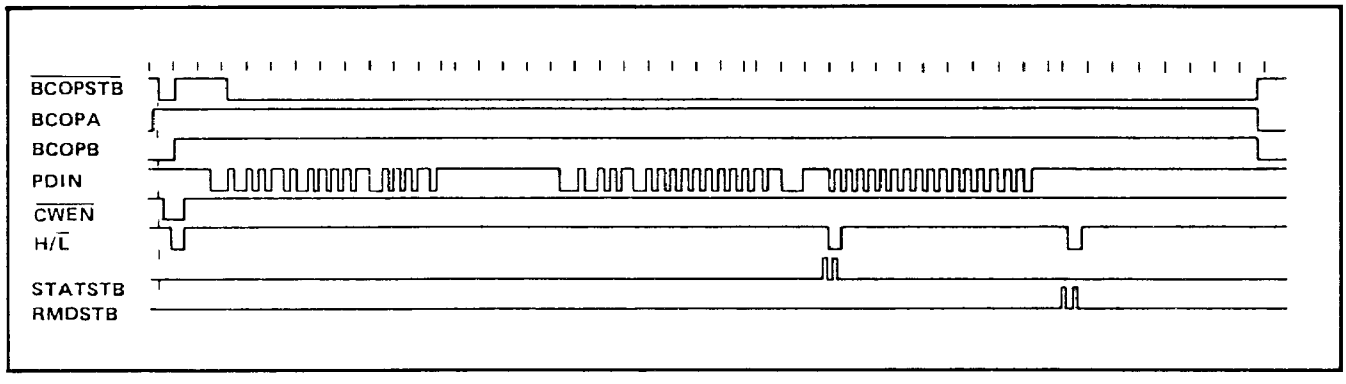

FIGURE 21. BUS CONTROLLER SENDING MODE COMMAND TRANSMIT VECTOR WORD MODE CODE 10000

PIN OUT

CT1612 PIN	CT1612FP PIN	FUNCTION
1	1	$\overline{\text{BIT DECODE}}$
2	2	CWC0 (LSB)
3	3	SA4 (MSB)
4	4	SA3
5	5	SA2
6	6	CWC4 (MSB)
7	7	CWC3
8	8	CWC2
9	9	CWC1
10	10	$\overline{\text{GBR}}$
11	11	H/$\overline{\text{L}}$
12	12	$\overline{\text{STATEN}}$/STATSTB
13	13	$\overline{\text{EOT}}$
14	14	SA1
15	15	SA0 (LSB)
16	16	$\overline{\text{INCMD}}$
17	17	TX/$\overline{\text{RX}}$
18	18	$\overline{\text{DTRQ}}$
19	19	$\overline{\text{VECTEN}}$/$\overline{\text{DWEN}}$
20	20	$\overline{\text{NBGT}}$
21	21	$\overline{\text{SYNC}}$
22	22	INCLK
23	23	IUSTB
24	24	$\overline{\text{NEXT STAT}}$
25	25	$\overline{\text{DTAK}}$
26	26	BCOPA
27	27	$\overline{\text{BCOPSTB}}$
28	28	BCOPB
29	29	$\overline{\text{PASMON}}$
30	30	$\overline{\text{NDRQ}}$
31	31	REQBUSB
32	32	REQBUSA
33	33	COMMON AND CASE
34	34	$\overline{\text{ENABLE}}$
35	35	$\overline{\text{STAT UPDATE}}$
36	36	MEREQ
37	37	IH08 (LSB)
38	38	IH19
39	39	IH210
40	40	IH311
41	41	IH412
42	42	IH513
43	43	IH614
44	44	IH715 (MSB)
45		NC

CT1612 PIN	CT1612FP PIN	FUNCTION
46		NC
47	45	RTADPAR
48	46	RTAD0 (LSB)
49	47	RTAD1
50	48	RTAD2
51	49	RTAD3
52	50	RTAD4 (MSB)
53	51	$\overline{\text{CMSYNC}}$
54	52	$\overline{\text{DWSYNC}}$
55	53	BCSTEN 0
56	54	RX DATA 0
57	55	RX $\overline{\text{DATA}}$ 0
58	56	BCSTEN 1
59	57	$\overline{\text{RT0}}$
60	58	6 MCK
61	59	$\overline{\text{ERROR}}$
62	60	$\overline{\text{LTFAIL}}$
63	61	$\overline{\text{MANER}}$
64	62	$\overline{\text{PARER}}$
65	63	$\overline{\text{VALD}}$
66	64	$\overline{\text{RTADER}}$
67	65	RX DATA 1
68	66	RX $\overline{\text{DATA}}$ 1
69	67	+5 VIN
70	68	TX INHIBIT 1
71	69	TX INHIBIT 0
72	70	TX DATA
73	71	TX $\overline{\text{DATA}}$
74	72	$\overline{\text{SERVREQ}}$
75	73	$\overline{\text{TXT0}}$
76	74	$\overline{\text{DBCACC}}$
77	75	$\overline{\text{RESET}}$
78	76	RT/$\overline{\text{BC}}$
79	77	$\overline{\text{DBCREQ}}$
80	78	$\overline{\text{HSFAIL}}$
81	79	$\overline{\text{LSTCMD}}$/$\overline{\text{CWEN}}$
82	80	$\overline{\text{BITEN}}$/RMDSTB
83	81	$\overline{\text{BUSY}}$
84	82	WC4 (MSB)
85	83	WC3
86	84	WC0 (LSB)
87	85	$\overline{\text{SSERR}}$
88	86	WC2
89	87	WC1
90	88	NC

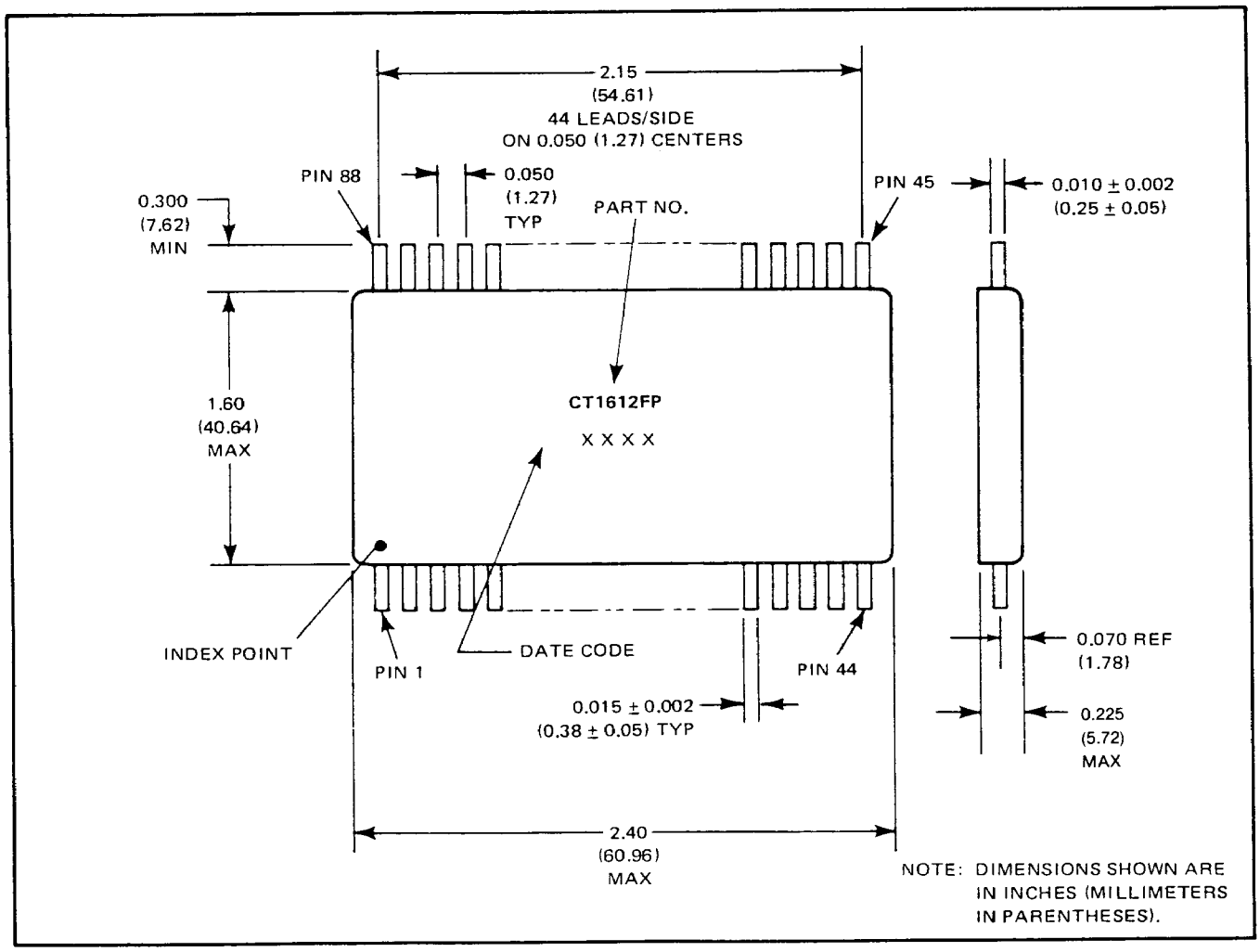

FIGURE 22. FLAT PACK

PACKAGE OUTLINES

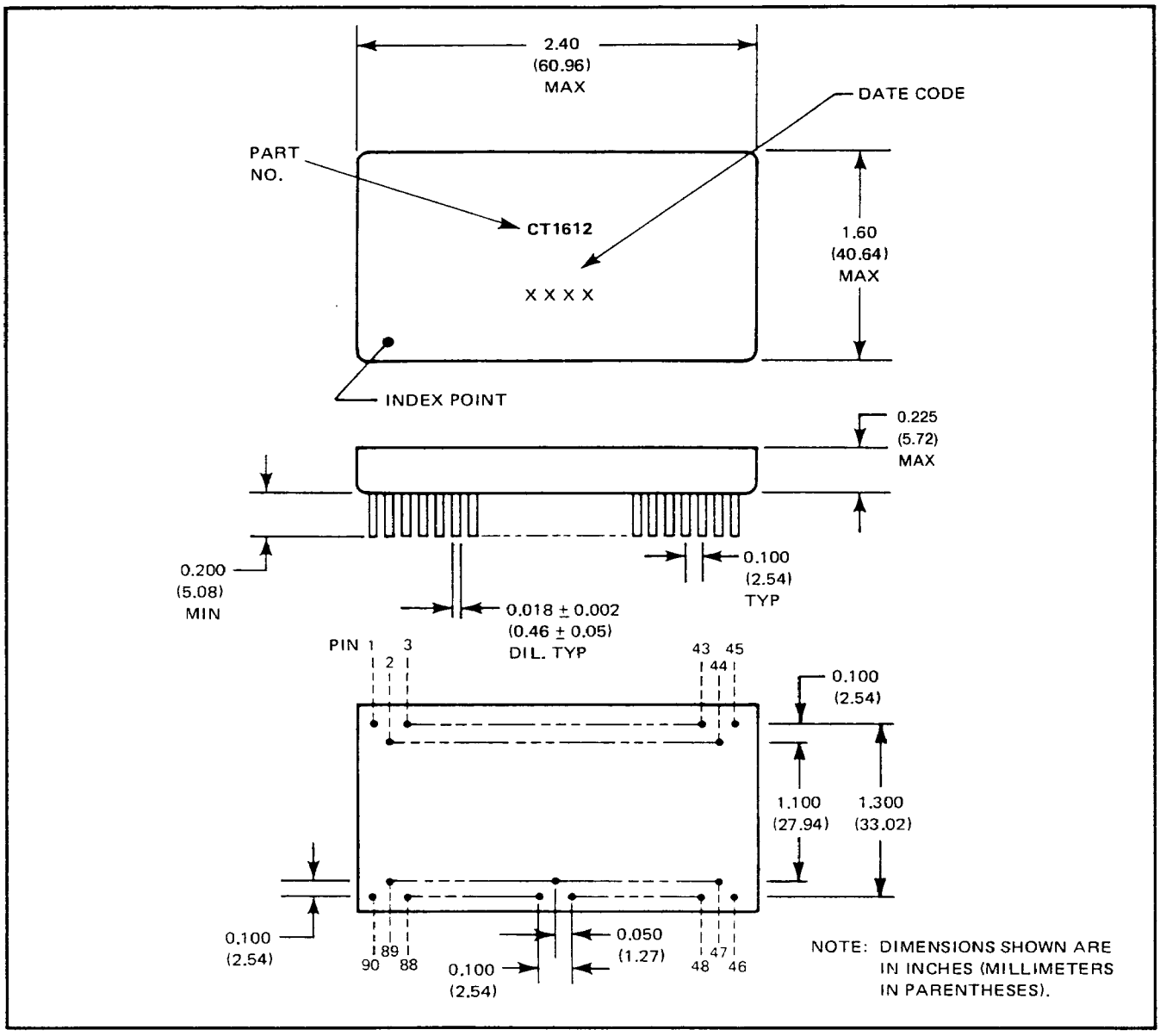

FIGURE 24 . PLUG-IN