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SSI 32P4910A
PRML Read Channel with PR4, 8/9 ENDEC, 4-burst Servo
Advance Information

February 1996

DESCRIPTION

The SSI 32P4910A is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 42 to 125 Mbit/s or 33 to 100 Mbit/s. Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 8,9 GCR ENDEC, data synchronizer, time base generator, and 4-burst servo. Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones. The part requires a single +5V power supply. The SSI 32P4910A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- Register programmable data rates from 42 to 125 Mbit/s or 33 to 100 Mbit/s
- Sampled data read channel with Viterbi qualification
- Programmable filter for PR4 equalization
- Five tap transversal filter with adaptive PR4 equalization
- 8/9 GCR ENDEC
- Data Scrambler/Descrambler
- Presettable Precoder State
- Programmable write precompensation
- Low operating power (0.925W typical at 5V)
- Register programmable power management (<5 mW power down mode)
- 4-bit nibble and byte wide bi-directional NRZ data interfaces
- 8-bit direct write mode automatically configured for RCLK = VCO/8
- Serial interface port for access to internal program storage registers
- Single power supply (5V ± 10%)
- Small footprint 80-lead PTQFP, 100-lead TQFP and 100-lead QFP packages

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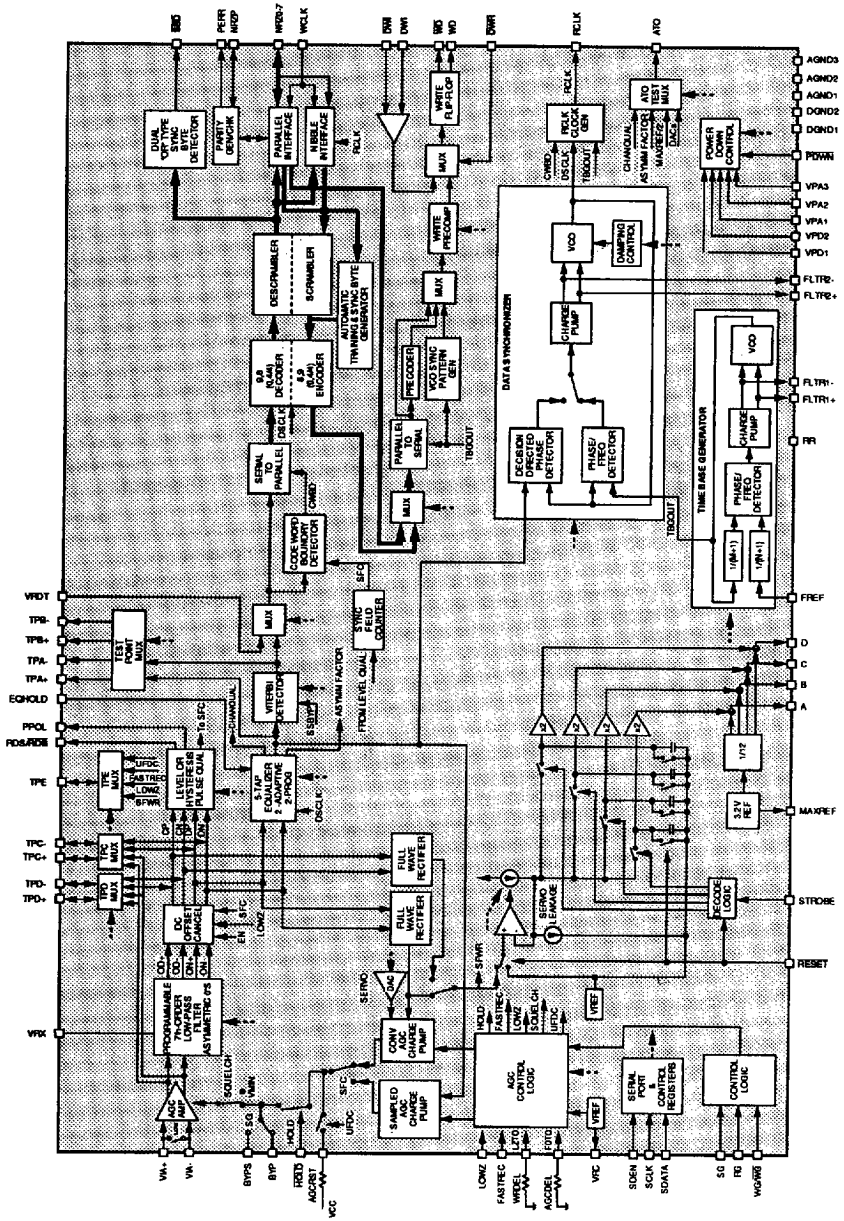
BLOCK DIAGRAM



FEATURES (continued)

AUTOMATIC GAIN CONTROL

- Dual mode AGC, analog during acquisition, sampled during data reads
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery (analog)
- Programmable, symmetric, charge pump currents for data reads (sampled)
- Charge pump currents track programmable data rate during data reads (sampled)
- Low drift AGC hold circuitry
- Low-Z circuitry at AGC input provides for rapid external coupling capacitor recovery
- AGC Amplifier squelch during Low-Z
- Wide bandwidth, precision full-wave rectifier
- Programmable AGC controls
  - Separate external input pins for AGC hold, fast recovery, and Low-Z control

  or

  - Internal Low-Z and fast decay timing for rapid transient recovery and AGC acquisition. Timing set with external resistors (2). Ultra fast decay current set with external resistor. AGC input impedance vs LOWZ = 5:1.
- 2-bit DAC to control AGC voltage in servo mode between 1.1 and 1.4V

FILTER/EQUALIZER

- Programmable, 7-pole, continuous time filter provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 4 to 34 MHz
  - Programmable boost/equalization of 0 to 13 dB
  - Programmable "zeros" equalization provides time asymmetry compensation
  - ±0.5 ns group delay variation from 0.3 fc to fc, with fc = 34 MHz
  - Minimizes size and power
  - Low-Z switch at filter output for fast offset recovery
  - No external coupling capacitors required
  - DC offset compensation provided at filter output
  - Five tap transversal filter for fine equalization to PR4
  - Self adapting inner taps (symmetric)
  - Programmable outer taps (symmetric, 4 bits)
  - Equalization hold input
  - "Zeros" channel quality output
  - Amplitude asymmetry factor output

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Register programmable window or hysteresis pulse qualifier for servo reads
- Selectable RDS pulse width and polarity for servo gray code reads

TIME BASE GENERATOR

- Less than 1% frequency resolution
- Up to 141 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

FEATURES (continued)

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 8,9 GCR ENDEC
- Register programmable to 125 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Adaptive clock recovery thresholds
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 4-bit nibble and byte wide NRZ data interfaces
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync byte detection, single byte or dual ("or" type)
- Semi-auto training and sync byte generation available for single sync byte operation
- Surface defect scan mode

SERVO

- 4-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- "Soft Landing" charge pump architecture
- Separate, automatically selected, registers for servo fc, boost, and threshold
- Programmable charge pump current
- Wide bandwidth, precision full-wave rectifier
- Programmable selection of normal or differentiated filter output to servo capture block
- Programmable AGC gain in servo mode (2 bits)
- Full wave rectifier observation point

FUNCTIONAL DESCRIPTION

The SSI 32P4910A implements a complete high performance PR4 read channel, including an AGC, programmable filter/equalizer, adaptive transversal filter, Viterbi pulse qualifier, time base generator, data separator with 8,9 ENDEC and scrambler/descrambler, and FWR servo, that supports data rates from 42 to 125 Mbit/s. Data rates from 33 to 100 Mbit/s are supported by changing a single resistor.

A serial port is provided to write control data to the 17 internal program storage registers.

AGC CIRCUIT DESCRIPTION

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the input of the pulse detector and sampled data processor while the input to the amplifier varies. The circuit consists of an AGC loop that includes an AGC amplifier, charge pump, programmable continuous time filter, and a precision, wide band, full wave rectifier. Depending on whether the read is of servo or data type, the specific blocks utilized in the loop are slightly different. Both loop paths are fully differential to minimize susceptibility to noise. AGC control can be programmably selected between direct and timed modes.

AGC Operation in Servo Read Mode

During servo reads the loop consists of the AGC amplifier with a continuous dual rate charge pump, the programmable continuous time filter, and the full wave rectifier. The gain of the AGC amplifier is controlled by the voltage stored on the BYPS hold capacitor (C_{BYPS}). The dual rate charge pump drives C_{BYPS} with currents that drive the differential voltage at DP/DN to the value programmed by the 2 SAGCLVL bits in the LDS register. These 2 bits allow adjustment of the filter's normal output voltage from 1.10 to 1.40 Vp-pd. Attack currents lower the voltage at the BYPS pin which reduces the amplifier gain. Decay currents raise the voltage at the BYPS pin which increases the amplifier gain. The sensitivity of the amplifier gain to changes in the BYPS voltage is approximately 38 dB/V. When the voltage at BYPS is equal to VRC, the gain from the AGC input to DP/DN will be about 24.9 dB. The charge pump is continuously driven by the instantaneous voltage at DP/DN. When the signal at DP/DN is greater than 100% of

the programmed AGC level, the normal attack current (ICH) of 416.5 µA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed level, the fast attack current (ICHF) of 3.50 mA is used to reduce the gain very quickly. This dual rate approach allows the AGC gain to be quickly decreased when it is too high and minimizes distortion when the proper AGC level has been acquired. The 100% and 125% levels are relative to the selected AGC level in servo mode.

A constant normal decay current (ID) of 24.5 µA acts to increase the amplifier gain when the signal at DP/DN is less than 100% of the programmed AGC level. The large ratio (416.5 µA:24.5 µA) of the normal attack and normal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. As a result the AGC loop will not be able to quickly increase its gain if required to do so. A fast recovery mode is provided to allow the gain to be rapidly increased to reduce recovery time between mode switches. In the fast recovery mode, the decay current is increased by a factor of 8 to 196 µA (IDFR) and the attack current is increased by a factor of 4.18 to 1.74 mA (ICHFR). This has the effect of speeding up the AGC loop between 4 and 8 times.

It is recommended that the fast recovery mode be asserted when the AGC fields from a sector are being read. Typically, this will be just after each transition of SG (Servo Gate), after powerup, and after WG/$\overline{\text{WG}}$ is de-asserted. For example, if C_{BYPS} is 500 pF and FASTREC is asserted for 0.5 µs in servo mode, the voltage at BYPS can increase at most by 0.5 µs • 196 µA/500 pF = 196 mV, which will allow the gain to increase by 6 dB in that time. If FASTREC is asserted for 0.5 µs in non-servo mode and CBYP is 1000 pF, then the voltage at BYP can increase at most by 0.5 µs • 196 µA/1000 pF = 98 mV, which will allow the gain to increase by 3 dB in that time. It is recommended that LOWZ be asserted for 0.5 µs just prior to any assertion of FASTREC in order to null any internal DC offsets. However, it is possible to assert both LOWZ and FASTREC simultaneously to reduce sector overhead. This method should be evaluated under the actual system operating conditions.

The programmable AGC level in servo mode is provided to allow the servo demodulator dynamic range to be adjusted over a narrow range.

AGC Operation in Data Read Mode

For data reads, the loop described above is used until the data synchronizer is locked to the incoming VCO preamble, except that the BYP hold capacitor (C_{BYP}) is used instead of BYPS and (C_{BYPS}). The normal decay current is 24.5 µA, the normal attack current is 416.5 µA, and the fast attack current is 3.5 mA. The fast recovery mode decay current is 196 µA and the fast recovery mode attack current is 1.74 mA. The above mentioned attack and decay currents are not scaled with the data rate setting. After the data synchronizer PLL is locked (SFC), the AGC loop is switched to include the AGC amplifier with a sampled charge pump, the programmable continuous time filter, full wave rectifier, and the sampling 5-tap equalizer to more accurately control the signal amplitude into the Viterbi qualifier. In this sampled AGC mode, a symmetrical attack and decay charge pump is used. The "1" sample amplitudes are sampled and held and compared to the ideal "1" value of 500 mV to generate the error current. The maximum charge pump current value can be programmed from the Sample Loop Control Register to 0, 34, 68, or 102 µA for maximum data rate and will scale downward with reduced Data Rate Register values.

AGC CONTROL MODES

The AGC control mode is determined by the state of bit 6 (AGCSEL) of the Control Operating Register #1. If this bit is 0 then the direct, external AGC control method is selected, i.e., AGC uses external signals provided to the FASTREC, LOWZ, and $\overline{\text{HOLD}}$ input pins. If bit 6 is a 1, the timed AGC control method is selected for generating the internal hold, fast recovery, squelch, and Low-Z signals.

Direct AGC Control Mode

For maximum application flexibility, all AGC mode control inputs are to be externally provided. When the LOWZ input is high, Low-Z mode is activated. In the Low-Z mode, the AGC amplifier input resistance is reduced to allow quick recovery of the AGC amplifier input ac coupling capacitors. The ratio of Low-Z to Non Low-Z resistance can be selected as either 15:1 or 5:1 by programming the LZTC bit in the Data Boost Register. During Low-Z mode, the time constant of the

Direct AGC Control Mode (continued)

internal AC coupling networks at the filter outputs are also reduced by the ratio determined by the LZTC bit. This time constant is 300 ns in Low-Z and either 5 µs or 1.5 µs when not in Low-Z mode, depending on the state of the LZTC bit. Low-Z also forces the AGC amplifier gain to be reduced to near 0 V/V. This mode should be activated during and for a short time after a write operation. It should also be activated for a short time after each transition of the SG input and on initial power up.

When the $\overline{\text{HOLD}}$ input is low, the charge pumps are disabled. This de-activates the AGC loop. The AGC amplifier gain will be held constant at a level set by the voltage at the BYP or BYPS pins. The value of the capacitor placed at these pins should be selected to give adequate droop performance when in hold mode as well as to insure stability of the AGC loop when it is active.

The signal provided to the FASTREC input pin determines if the AGC is in fast recovery mode. During the fast recovery (FASTREC = 1), the attack and decay currents are increased to allow faster recovery to the proper AGC level. If faster recovery than is provided by FASTREC alone is desired, an ultra fast recovery can be effected by connecting a resistor between the AGCRST pin and the positive supplyVPA. If this resistor is present, whenever FASTREC is entered, the voltage on the BYP or BYPS capacitor will be pulled up. This causes an extremely rapid increase in the AGC amplifier gain. The ultra fast current will be disabled the first time that the signal at DP/DN reaches the 125% point. The FASTREC attack and decay currents are used as long as the FASTREC pin is held high.

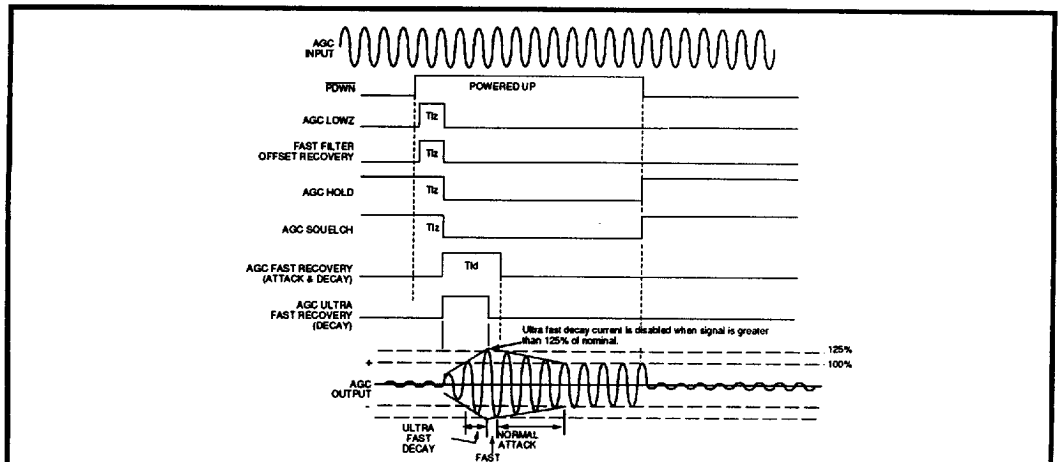


FIGURE 1: AGC Timing (Internal) Diagrams - Power-On Mode

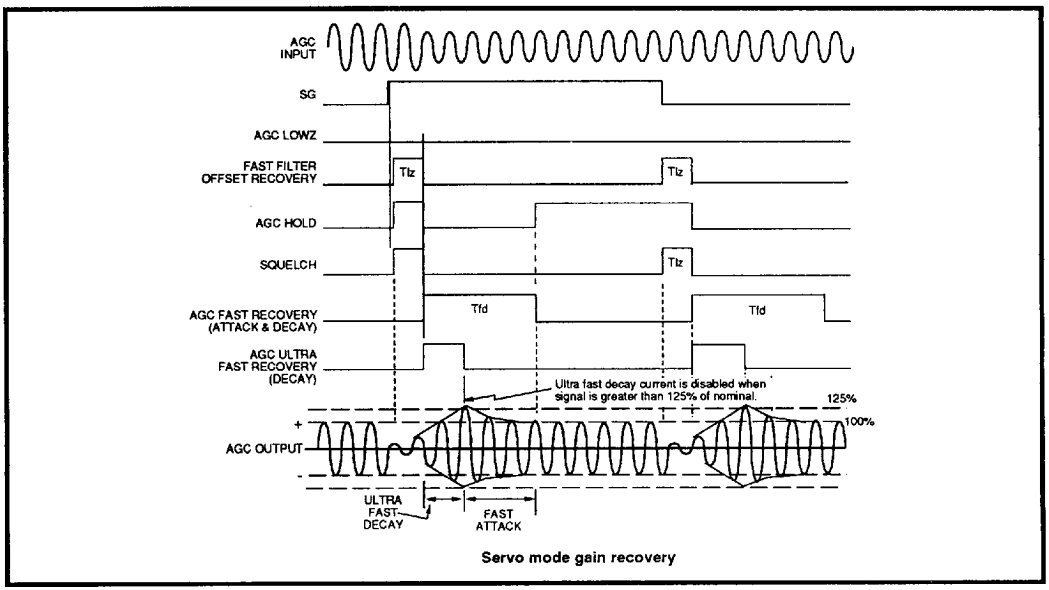


FIGURE 2: AGC Timing Diagrams - Servo Mode

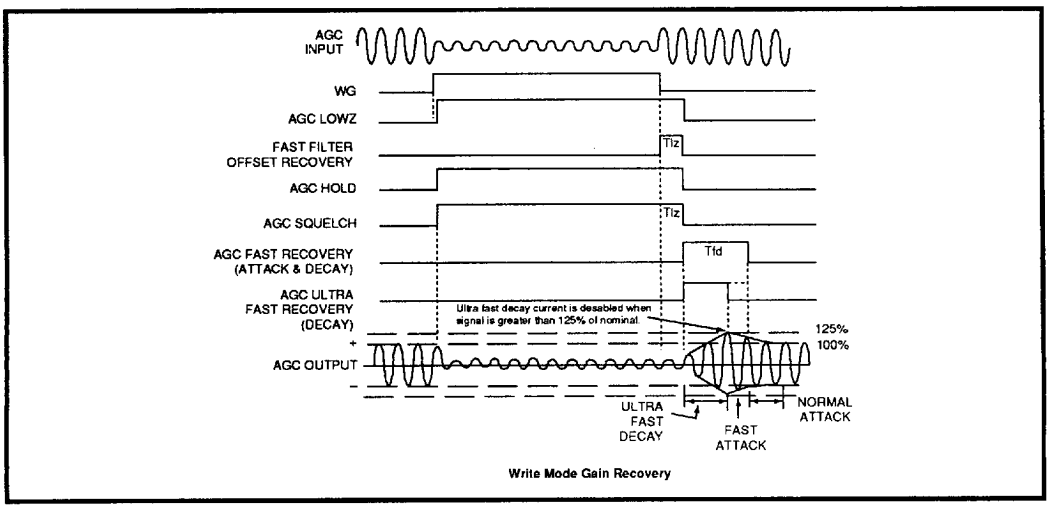


FIGURE 3: AGC Timing Diagrams - Write Mode

AGC CONTROL MODES (continued)

Timed AGC Control Mode

This timed AGC control mode differs from the direct control mode in that the external control inputs LOWZ, FASTREC, and $\overline{HOLD}$, are typically not used and therefore must be deasserted. The equivalent signals are generated internal to the SSI 32P4910A. These internal signals are generated by one-shots that are triggered by various conditions of the WG/$\overline{WG}$, SG, and $\overline{PDWN}$ inputs. The one-shot timings for the Low-Z and fastrec signals are set by the resistors connected to the WRDEL and AGCDEL input pins, respectively and analog ground. The time Low-Z period = 0.1 µs • $R_{WRDEL}(k\Omega)$ and the fast recovery period = 0.1 µs • $R_{AGCDEL}(k\Omega)$. The current for the ultra fast decay mode is set by the resistor connected between the AGCRST input pin and VPA. In the timed mode, the AGC shall use the C_{BYP} and C_{BYPS} for non-servo and servo modes respectively. The nominal and fast attack and decay currents are the same in both of the SSI 32P4910A's AGC control modes. In internally timed mode, the LOWZ, FASTREC, and $\overline{HOLD}$ input pins are logically or'ed with their respective internal control signals but do not affect the internal sequencing of the one-shot generated AGC control signals.

PULSE QUALIFICATION CIRCUIT DESCRIPTIONS

This device utilizes three different types of pulse qualification, one exclusively for servo reads, one primarily for servo reads, and the other for data reads.

Servo Read Mode

For servo gray code reads, either a dual level (window type) qualifier or a hysteresis type level qualifier may be selected. If the PDM bit in the filter cutoff servo register is set to 0, then the window qualifier is selected, and if the PDM bit is a 1, the hysteresis qualifier is selected. The polarity of the RDS/$\overline{RDS}$ is selected by the SMS bit (Servo Mode Select) in the Data Rate Register. If SMS = 0 then RDS is active low and if SMS = 1 then RDS is active high.

Dual Level (Window) Qualifier

During servo reads (SG high) a dual level type of pulse qualifier is used. The level qualification thresholds are set by a 6-bit DAC which is controlled by the (LDS) servo level threshold register. The register value is relative to the peak voltage at the output of the continuous time filter, derived off of the same reference voltage internal to the chip. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the WP/LT register does not affect this DAC's reference. The RDS/$\overline{RDS}$ and the PPOL outputs of the level qualifier indicate a qualified servo pulse and the polarity of the pulse, respectively. The RDS/$\overline{RDS}$ and PPOL outputs are only active when the SG input is high.

Hysteresis Qualifier

The hysteresis qualifier performs the same as the window qualifier except that the hysteresis qualifier guarantees that the second of two consecutive pulses of the same polarity will not be qualified. The hysteresis qualifier will only qualify pulses of alternating polarity.

Data Read Mode

In data read mode (RG high), the dual level qualifier used for servo reads, is used during VCO sync field counting. It's qualification thresholds are set by a 6-bit DAC which is controlled by the (LD) Data Level Threshold Register. The register value is relative to the peak voltage at output of the continuous time filter and the DAC both referenced to bandgap voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the WP/LT Register does not affect the DAC's reference until the sync field count has been achieved. The RDS/RDS and the PPOL outputs of the level qualifier are not active in data read mode.

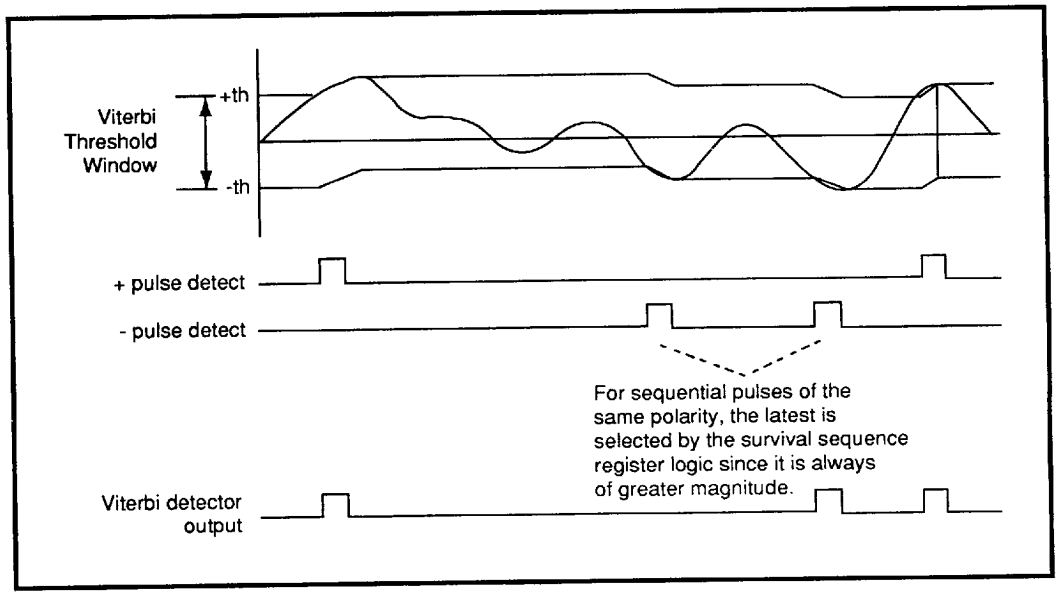


FIGURE 4: Viterbi Detection

Viterbi Qualifier

The second type of pulse qualification, the Viterbi qualifier, is only used during data read mode after the sync field count has been achieved. The Viterbi qualifier has two significant blocks, one that feeds the other. The first block is the sampled pulse detector and the second is the survival sequence register.

The sampled pulse detector performs the pulse acquisition/detection in the sampled domain. It acquires pulses by comparing the code clock sampled analog waveform to the positive and negative thresholds established by the programmable Viterbi threshold window. The Viterbi threshold window is defined to be the difference between the positive and negative threshold levels. The threshold window, Vth, is set by a 7-bit DAC which is controlled by the Viterbi Detector Threshold Register (VDT). While the window size is fixed by the programmed Vth value, the actual positive and negative thresholds track the most positive and the most negative samples of the equalized input signal. For example, the Viterbi positive signal threshold, Vpt = Vpeak (+) max if the previous detected level was (+). If the previous detect level was (-), Vpt = Vpeak(-)max + Vth, where Vpeak(-)max is the maximum amplitude of the previously detected negative signal. Normally Vth is set to equal Vpeak (approx. 500 mV).

After the pulses have been detected they must be further qualified by the survival sequence registers and associated logic. This logic guarantees that for sequential pulses of the same polarity within the maximum run length, only the latest is qualified. In this way, only the pulse of greatest amplitude will be qualified.

The Viterbi qualifier is implemented as two parallel qualifiers that operate on interleaved samples. Each qualifier has a survival sequence register length of 5.

To facilitate media scan testing, the Viterbi survival sequence register may be bypassed by setting the BYPSR bit in the Viterbi Detector Threshold (VDT) Register.

FUNCTIONAL DESCRIPTION (continued)

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The on-chip, continuous time, low pass filter has register programmable cutoff and boost settings, and provides both normal and differentiated outputs. It is a 7th order filter that provides a 0.05° phase equiripple response. The group delay is relatively constant up to twice the cutoff frequency. For pulse slimming two zero programmable boost equalization is provided with no degradation to the group delay performance. The differentiated output is created by a single-pole, single-zero differentiator. Both the boost and the filter cutoff frequency for data reads and the filter cutoff frequency for servo reads are programmed through internal 7-bit DACs, which are accessed via the serial port logic. The nominal boost range at the cutoff frequency is 0 to 13 dB for data reads and is controlled by the Data Boost Register. In servo mode, the boost can be programmed in 2 dB steps from 0 to 6 dB by programming the two FBS bits (bits 6 and 7) in the Filter Boost Servo Register. The cutoff frequency, fc is variable from 4 to 34 MHz and controlled by the Data Cutoff Register or Servo Cutoff Register in the servo mode. The cutoff and boost values for servo reads are automatically switched when servo mode is entered.

The filter zero locations can be programmed asymmetrically about zero to compensate for MR head time asymmetry. The asymmetry is adjusted by programming the 6 FGD bits (bits 0 - 5) in the Filter Boost Servo Register. The asymmetric zero's are not usable while in servo mode.

The normal low pass filter is of a seven-pole two-real-zero type. Figure 5 illustrates the normalized transfer function normalized to 1 rad/s. The response can be denormalized to the cutoff frequency of fc (Hz) by replacing s by $s/2\pi fc$, while the boost & group delay equalization are controlled by varying the α and β.

With a zero at the origin, the filter provides a time-differentiated filter output. This is used in time qualification of the peak detection. To ease the timing requirement in peak detection of a signal slightly above the qualification threshold, the time-differentiated output is purposely delayed by 1.2 ns relative to the normal low pass output.

The normal low pass output feeds the data qualifier (DP/DN), and the differentiated output feeds the clock comparator (CP/CN).

Five definitions are introduced for the programmable filter control discussion (Figure 6):

CUTOFF FREQUENCY: The cutoff frequency is the -3 dB low pass bandwidth with no boost & group delay equalization, i.e., $\alpha=0$ and $\beta=0$.

ACTUAL BOOST: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha\neq0$ and/or $\beta\neq0$.

ALPHA BOOST: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha\neq0$ and without group delay equalization. In general, the actual boost with group delay equalization is higher than the alpha boost. However, with >3 dB alpha boost, the difference is minimal.

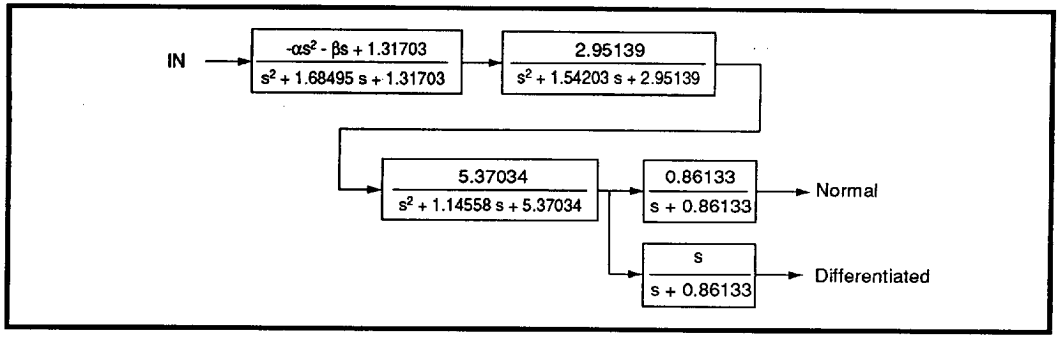


FIGURE 5: Programmable Filter Normalized Transfer Function

GROUP DELAY Δ%: The group delay Δ% is the percentage change in absolute group delay at DC with respect to that without equalization applied (β = 0).

GROUP DELAY VARIATION: The group delay variation is the change in group delay from DC to the cutoff frequency. This can be expressed as a percentage defined as: (change in group delay ÷ absolute group delay with β = 0) • 100%. An alternative is to express the group delay variation in nanosecond. Because the absolute group delay variation in nanosecond is scaled by the programmed cutoff frequency, the percentage expression is used in this specification.

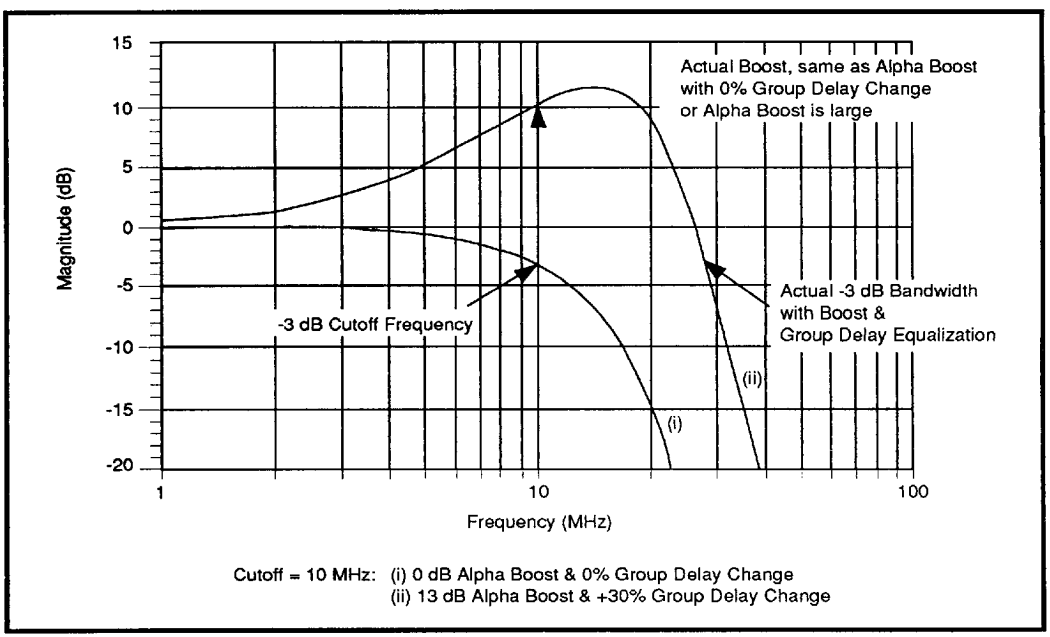


FIGURE 6: Filter Magnitude Response

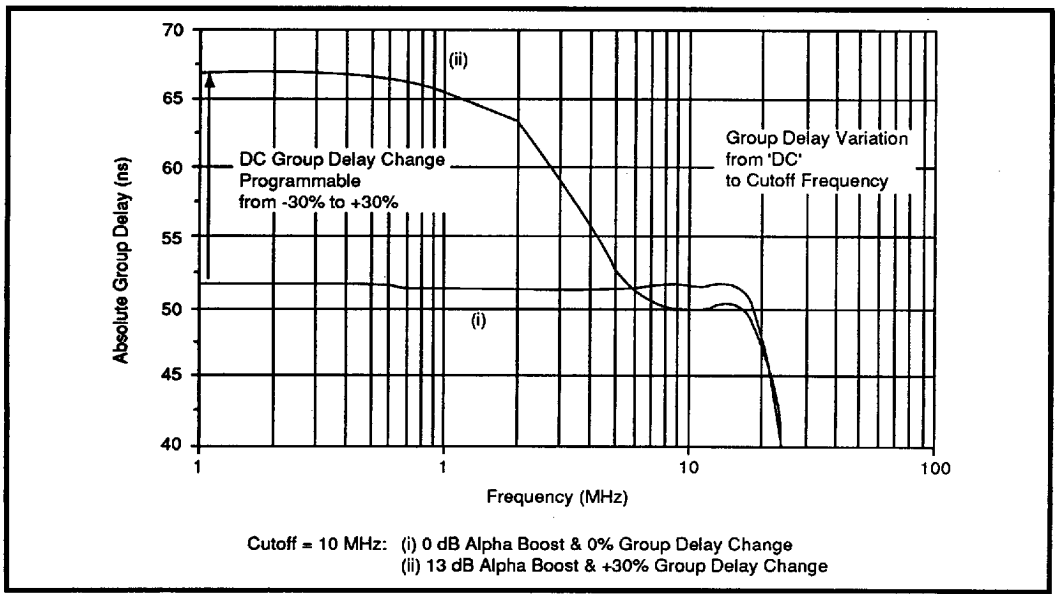


FIGURE 7: Filter Group Delay Response

FUNCTIONAL DESCRIPTION (continued)

Filter Operation

Direct coupled differential signals from the AGC amplifier output are applied to the filter. The programmable bandwidth and equalization characteristics of the filter are controlled by 3 internal DACs. The registers for these DACs (FC, FB, and FGD) are programmed through the serial port. The current reference for the DACs is set using a single external resistor connected from pin VRX to ground. The voltage at pin VRX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. This establishes the excellent temperature stability for the filter characteristics.

The cutoff frequency can be set independently in the servo mode and the data mode. In the data mode, the cutoff frequency is controlled by the Data Cutoff Register. In the servo mode, the cutoff frequency is controlled by the Servo Cutoff Register.

Cutoff Control

The programmable cutoff frequency from 4 to 34 MHz is set by the 7-bit linear FC DAC. The FC register holds the 7-bit DAC control value. The cutoff frequency is set as:

for data zones:

$$fc\ (\text{MHz}) = 0.301 \cdot \text{FC} - 1.142 \quad 44 \le \text{FC} \le 117$$

for servo zones:

$$fc\ (\text{MHz}) = 0.277 \cdot \text{FCS} + 0.08 \quad 14 \le \text{FCS} \le 43$$

The filter cutoff (fc) is defined as the -3 dB bandwidth with no boost applied. When boost/equalization is applied, the actual -3 dB point will move out. The ratio of the actual -3 dB bandwidth to the programmed cutoff is tabulated in Table 1 as a function of applied boost & group delay equalization.

TABLE 1: Ratio of Actual -3 dB Bandwidth to Cutoff Frequency

Alpha Boost	Group Delays Δ%						
	±30%	±25%	±20%	±15%	±10%	±5%	0%
0 dB	1.62	1.47	1.31	1.16	1.06	1.01	1.00
1	1.74	1.62	1.50	1.38	1.28	1.21	1.19
2	1.87	1.79	1.71	1.63	1.56	1.51	1.49
3	2.01	1.96	1.91	1.87	1.83	1.80	1.79
4	2.14	2.11	2.09	2.07	2.05	2.04	2.03
5	2.25	2.24	2.23	2.22	2.21	2.20	2.20
6	2.35	2.34	2.34	2.33	2.33	2.32	2.32
7	2.44	2.44	2.43	2.43	2.42	2.42	2.42
8	2.52	2.52	2.51	2.51	2.51	2.51	2.51
9	2.59	2.59	2.59	2.59	2.59	2.59	2.59
10	2.67	2.66	2.66	2.66	2.66	2.66	2.66
11	2.73	2.73	2.73	2.73	2.73	2.73	2.73
12	2.80	2.80	2.80	2.80	2.80	2.80	2.80
13	2.87	2.87	2.86	2.86	2.86	2.86	2.86

Boost Control

The programmable alpha boost from 0 to 13 dB is set by the 7-bit linear FB DAC in data mode or 2-bit linear FBS DAC in servo mode. The FB register holds the 7-bit DAC control value and the FBS register holds the 2-bit control value. The alpha boost in data mode is set as:

$$\text{Alpha boost (dB)} = 20 \cdot \log \frac{[0.021848 \cdot FB + 0.000046]}{\cdot FB \cdot FC + 1} \quad 0 \le FB \le 127$$

The alpha boost in servo mode is set as:

$$\text{Alpha boost (dB)} = \frac{2 \cdot FBS}{} \quad 0 \le FBS \le 3$$

That is, the boost in servo mode can be changed in 2 dB steps from 0 to 6 dB.

The programmed alpha boost is the magnitude gain at the cutoff frequency with no group delay equalization. When finite group delay equalization is applied, the actual boost is higher than the programmed alpha boost. However, the difference becomes negligible when the programmed alpha boost is >3 dB. Table 2 tabulates the actual boost as a function of the applied alpha boost & group delay equalization.

Group Delay Equalization

The group delay Δ% can be programmed between -30% to +30% by the 6-bit linear FGD DAC. The FGD register holds the 6-bit DAC control value. The group delay Δ% is set as:

Group delay Δ% = 0.9783 • (FGD4:0) • -0.665
$0 \le FGD4:0 \le 31$ and FGD5 = sign bit

The group delay Δ% is defined to be the percentage change of the absolute group delay due to equalization from the absolute group delay without equalization at DC.

The current reference for the filter DACs is set using a single 12.1 kΩ resistor, from the VRX pin to ground. The voltage at VRX is proportional-to-absolute-temperature (PTAT).

The outputs of the filter are internally AC coupled to the qualifier inputs and buffers for the filter monitoring test points TPC+/TPC- and TPD+/TPD-.

TABLE 2: Actual Boost vs Alpha Boost & Group Delay Change

Alpha Boost	Group Delays Δ%						
	±30%	±25%	±20%	±15%	±10%	±5%	0%
0 dB	2.81	2.12	1.47	0.89	0.42	0.11	0.00
1	3.36	2.76	2.21	1.72	1.33	1.09	1.00
2	3.97	3.45	2.99	2.58	2.27	2.07	2.00
3	4.63	4.19	3.80	3.47	3.21	3.05	3.00
4	5.34	4.97	4.65	4.38	4.17	4.04	4.00
5	6.10	5.79	5.52	5.30	5.14	5.03	5.00
6	6.89	6.64	6.42	6.24	6.11	6.03	6.00
7	7.72	7.51	7.34	7.19	7.09	7.02	7.00
8	8.58	8.41	8.27	8.15	8.07	8.02	8.00
9	9.47	9.33	9.22	9.12	9.05	9.01	9.00
10	10.4	10.3	10.2	10.1	10.1	10.0	10.0
11	11.3	11.2	11.1	11.1	11.0	11.0	11.0
12	12.2	12.2	12.1	12.1	12.0	12.0	12.0
13	13.2	13.1	13.1	13.1	13.0	13.0	13.0

FUNCTIONAL DESCRIPTION (continued)

INTERNAL AC COUPLING

The conventional external ac coupling at the filter to qualifier interface has been replaced by a pair of feedback circuits, one for the normal and one for the differentiated outputs of the filter. The offset of the filter outputs are sensed, integrated, and fed back to the filter output stage. The feedback loop forces the filter offset nominally to zero. In the normal read mode, (LOWZ = 0), the integration time constant is set to 5 µs until the sync field counter reaches the programmed SFC count. At the SFC count, the offset sensing is switched into sampled mode and the time constant is reduces to 300 ns. In sampled mode the offset correction voltage is generated from the zeros qualified by the quantizer. This ensures that the sampled voltage level, not DP/DN, will be offset free.

AMPLITUDE ASYMMETRY DETECTION AND CORRECTION

In the presence of amplitude asymmetry, such as that generated by MR heads, the sampled data processor (SDP) will be presented with zeros generated in one of two ways. The first is due the lack of a magnetic transition and will be referred to as a "real" zero. The second is produced by the superposition of adjacent +1 and -1 magnetic transitions and results in zero samples that shall be referred to as "cancelled" zeros. In the presence of amplitude asymmetry from an MR head, the "real" zeros are zero, but the "cancelled" zeros are offset by the difference between the +1 and -1 samples.

The offset correction circuit forces the ground reference of the sampled data processor to the center of the "real" and "cancelled" zero sample levels.

The integration time constant is increased by a factor of 4 to 1.0 µs, after the sync byte has been detected.

Amplitude Asymmetry Monitor Point

An amplitude asymmetry quality factor "Qasym" may be selected to be output on the ATO output pin by programming the ASEL bits in the Power Down Register. This signal is derived by computing the average distance of the 'real" and "cancelled" zeros from the sampled data processor's system ground which was established between the two zeros levels by the offset correction circuit. The average distance is a measure of the asymmetry present in the MR read back signal. A gain of 4 from the sampled values is utilized and is low pass filtered with a time constant that is programmable to one of four different values by programming the two QTC bits in the Control Operating Mode Register 2.

The signal is then buffered and differentially multiplexed to the ATO pin. The signal is referenced to MAXREF/2.

The asymmetry quality factor can be held at the value present at sync byte detect by setting the FREZQ bit in the WP/LT Register. The value will be held for 10 ms and is NOT reset. The ATO output may also be externally filtered to provide time constants that are appropriate for averaging over major portions of, or an entire sector. The capacitors on externally added filters must be externally reset. Note that any external filtering added to ATO output pin will affect both the amplitude asymmetry monitor signal and the equalization quality monitor signal since they are both muxed to the ATO output pin.

ADAPTIVE EQUALIZER CIRCUIT DESCRIPTION

Up to 7 dB of equalization for fine shaping of the incoming read signal to the PR4 waveshape is provided by a 5 tap, sampled analog, transversal filter. This filter provides a self adaptive multiplier coefficient for the inner taps and a programmable coefficient for the outer taps. Both inner taps use the same coefficient (km_1), and both outer taps use the same coefficient (km_2).

For the adaptive inner taps, the value of km_1 is adjusted to force "zero" samples to zero volts. A special equalizer training pattern, located after the VCO sync field in the sector format, is used to provide an optimum signal for the equalizer to adapt to. The adaptive property of these taps is enabled or disabled by the AEE bit in the Sample Loop Register. If the adaptive property is enabled, whether adaptation occurs only during the training pattern or both during the training pattern and the user data is controlled by the AED bit in the Sample Loop Register.

The adaptation can be observed when the equalizer control voltage is selected as the TPA+/TPA- output. The equalizer control voltage is approximately related to km1 by:

km1 = 0.009 • Date Rate (Mbit/s) • (TPA+ - TPA-)

The multiplier coefficients for the adaptive taps can be held for up to 10 ms if the EQHOLD input is brought high after sync byte detect has occurred during a previous read in which proper training has occurred. The EQHOLD input pin may be asserted at any time during a read cycle and the adaptive coefficient Km1 present at that time will be held, provided no leakage occurs, until the EQHOLD input is de-asserted.

The multiplier coefficient, km_2 for the outer taps is programmable between +0.117 and -0.135 by the 4 km bits (bits 4 - 7) in the Control Operating Mode Register #2.

Equalization Quality Monitor Point

An equalization quality factor "Q" may be selected to be output on the ATO output pin by programming the ATOSEL bits in the Power Down Register and should be used as a guide for selection of the appropriate value for km_2. This signal is derived by computing the absolute distance of the 'real" and "cancelled" zeros from the sampled data processor's system ground which was established between the two zeros levels by the offset correction circuit. Then the asymmetry factor (QASYM) is subtracted and the resulting signal is full wave rectified and low pass filtered using one of the four time constants that may be programmed with the two QTC bits in the Control Operating Mode Register #2. The signal is then buffered and differentially multiplexed to the ATO pin. The overall gain to the ATO pin is 4. The signal is referenced to MAXREF/2.

The equalization quality factor can be held at the value present at sync byte detect by setting the FREZQ bit in the WP/LT Register. The value will be held for approx. 10 ms and is NOT reset. The ATO output may also be externally filtered to provide time constants that are appropriate for averaging over major portions of, or an entire sector. The capacitors on externally added filters must be externally reset.

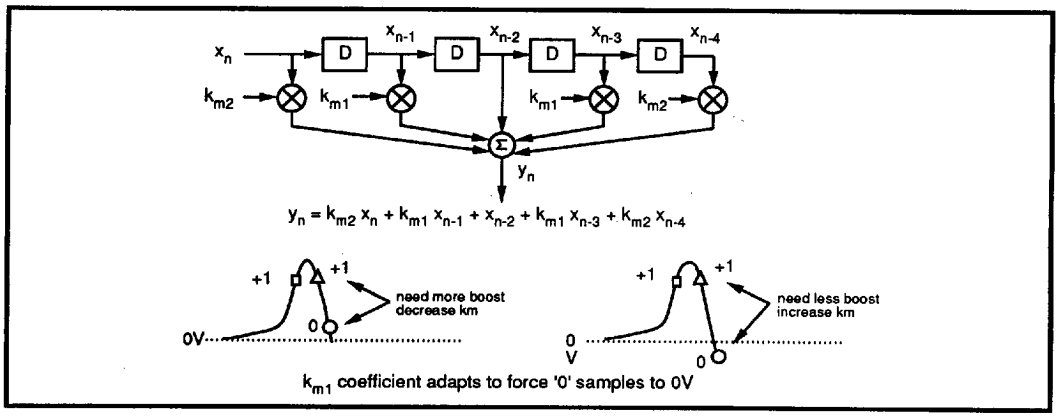


FIGURE 8: Block Diagram of 5-Tap Equalizer

FUNCTIONAL DESCRIPTION (continued)

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator (TBG) is a PLL based circuit, that provides a programmable reference frequency to the data separator for constant density recording applications. This time base generator output frequency can be programmed with a less than 1% accuracy via the M, N and DR registers. The TBG output frequency, Fout, should be programmed as close as possible to ((9/8) • NRZ Data Rate). The time base also supplies the timing reference for write precompensation so that the precompensation tracks the reference time base period.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully-differential and balanced in order to reduce the effects of common mode noise.

In read, write and idle modes, the programmable time base generator is used to provide a stable reference frequency for the data separator. In the write and idle modes, the time base generator output, when selected by the Control Test Mode Register, can be monitored at the TPB+ and TPB- test pins. In the read mode, the TBG output should not be selected for output on the test pins so that the possibility of jitter in the data separator PLL is minimized.

The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$F_{TBG} = FREF \cdot [(M + 1) \div (N + 1)]$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The data rate register must be set to the correct VCO center frequency. The time base generator PLL responds to any changes to the M and N registers, only after the DR register is updated.

The DR register value, directly affects the following:

- center frequency of the time base generator VCO,
- center frequency of the data separator VCO,
- phase detector gain of the time base generator phase detector,
- phase detector gain of the data separator phase detector,
- write precompensation

The reference current for the DR DAC is set by an external resistor, RR, connected between the RR pin and ground.

RR = 10.0 kΩ for 42 to 125 Mbit/s data rate range

RR = 12.1 kΩ for 33 to 100 Mbit/s data rate range

DATA SEPARATOR CIRCUIT DESCRIPTION

The data separator circuit provides complete encoding, decoding, and synchronization for 8,9 (0,4,4) GCR data. In data read mode, the circuit performs clock recovery, code word synchronization, decoding, sync byte detection, descrambling, and NRZ interface conversion. In the write mode, the circuit generates the VCO sync field, scrambles and converts the NRZ data into 8,9 (0,4,4) GCR format, precodes the data, and performs write precompensation.

The circuit consists of five major functional blocks; the data synchronizer, 8,9 ENDEC, NRZ scrambler/descrambler, NRZ interface, and write precompensation.

Data Synchronizer

The data synchronizer uses a fully integrated, fast acquisition, PLL to recover the code rate clock from the incoming read data. To achieve fast acquisition, the data synchronizer PLL uses two separate phase detectors to drive the loop. A decision-directed phase detector is used in the read mode and phase-frequency detector is used in the idle, servo, and write modes.

In the read mode the decision-directed timing recovery updates the PLL by comparing amplitudes of adjacent "one" samples or comparing the "zero" sample magnitude to ground for the entire sample period. A special (non IBM) algorithm is used to prevent "hang up" during the acquisition phase. The determination of whether a sample is a "one" or a "zero" is performed by a dedicated, dual mode, threshold comparator. This comparator's threshold levels are determined by the value, Lth, programmed in the Data Threshold Register. The fixed level threshold before the sync field count (SFC) has been achieved will be 1.4 times the threshold level after SFC since this is the ratio of the peak signal to the sampled "1" signal amplitude for PR4. The dual mode nature of this comparator allows the selection of either symmetric fixed or independent self adapting (+) and (-) thresholds by programming the adaptive level enable (ALE) bit in the WP/LT Register. Also at SFC, the gain of the phase detector is reduced by a factor of 6 or 10, selectable by the GS bit in the Damping Ratio Control Register. This gain shift increases the loop's noise immunity during data tracking by reducing its bandwidth.

The adaptive reference allows the specification of the threshold value to be a percentage of an averaged peak value. When adaptive mode is selected, the fixed thresholds are used until the sync field count (SFC) has been reached, then the adaptive levels are internally enabled. The time constant of a single pole filter that controls the rate of adaptation, is programmable by bits TC2-1 in the WP/LT Register.

In the write and idle modes the non-harmonic phase-frequency detector is continuously enabled, thus maintaining both phase and frequency lock to the time base generator's VCO output signal, FTBG. The polarity and width of the detector's output current pulses correspond to the direction and magnitude of the phase error.

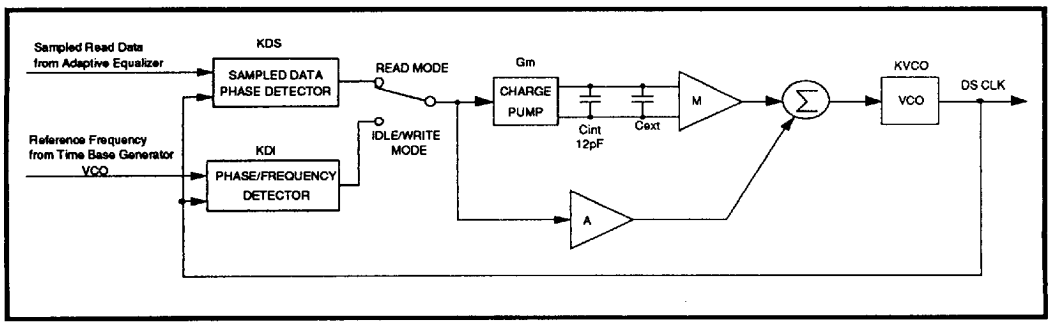


FIGURE 9: Data Synchronizer Phase Locked Loop

Data Synchronizer (continued)

The two phase detectors' outputs are muxed into a single differential charge pump which drives the loop filter directly. The loop filter requires an external capacitor. The loop damping ratio is programmed by bits 6-0 in the Damping Ratio Control Register. The programmed damping ratio is independent of data rate.

In write mode, the TBG output is used to clock the encoder, precoder, and write precompensation circuits. The output of the precompensation circuit is then fed to the write data flip-flop which generates the write data (WD, $\overline{WD}$) outputs.

ENDEC

The ENDEC implements an 8,9 (0,4,4) Group Coded Recording (GCR) algorithm. The code has a minimum of no zeros between ones and a maximum of four zeros between ones for the interleaved samples. During write operations the encoder portion of the ENDEC converts 8-bit parallel, scrambled or nonscrambled, data to 9-bit parallel code words that are then converted to serial format. In data read operation, after the code word boundary has been detected in the Viterbi qualified serial data stream, the data is converted to 9-bit parallel form and the decoder portion of the ENDEC converts the 9-bit code words to 8-bit NRZ format.

Sync Byte Detection

The SSI 32P4910A supports two types of sync byte detection, dual byte and single byte.

Dual Sync Byte Detection

The SSI 32P4910A implements a dual "or" type sync byte detection scheme to reduce the probability that a single bit errors will lead to the inability to synchronize. The two sync bytes are different and are spaced apart by one byte. The first sync byte is 1FH and the second is 69H. Sync byte detection is considered to have occurred if either of the two sync bytes is found but the sync byte detect output pin ($\overline{SBD}$) is transitioned at the position in time when the second sync byte (69) would have been detected. The data placed on the NRZ outputs when $\overline{SBD}$ goes low is always the second sync byte (69) regardless of which of the two was actually detected.

Single Sync Byte Detection

Since the SSI 32P4910A looks for either of the two sync bytes, the absence of the first sync byte is not an error. This allows for only a single byte to be written and still be able to achieve synchronization. It is recommended that only the 69H be written if single sync byte detection is desired so that when detection occurs, the data output on the NRZ pins at sync byte detect will match the sync byte written.

Single Sync Byte Detection When Semi Automatic Training Is Enabled

When the AUTOTR bit is set in the control operating register, the training /sync byte sequence is generated with an internal state machine. The internal state machine generates the 5-byte equalizer training pattern (93H) followed by the second sync byte (69H); the first sync byte (1FH) is not written by the internal state machine. To initiate the writing of the training pattern and sync byte in this mode, an FFH must be placed on the NRZ bus for 6 byte times prior to the user data. This mode may be desirable if controller state machine space is very limited.

Scrambler/Descrambler

The scrambler/descrambler circuit is provided to reduce fixed pattern effects on the channel's performance. It is enabled or disabled by bit 2 (SD) of the control operating register. In write mode, if enabled, the circuit scrambles the 8-bit internal NRZ data before passing it to the encoder. Only user data, i.e., the NRZ data following the second sync byte (69H), is scrambled. In data read mode, only the decoded NRZ data after the second sync byte (69H) is descrambled. The scrambler polynomial is $H(X) = 1 \oplus X7 \oplus X10$. The scrambler block diagram is shown below. The scrambler contributes no delay in either the encode or decode paths and therefore there is no difference in path delays whether or not the scrambler is enabled.

NRZ Interface

The NRZ interface circuit provides the ability to interface with either a nibble or byte-wide controller. The NRZ interface type is specified by the programming of bit 4 (NIB) of the control operating register. If byte wide mode is selected, the circuit does

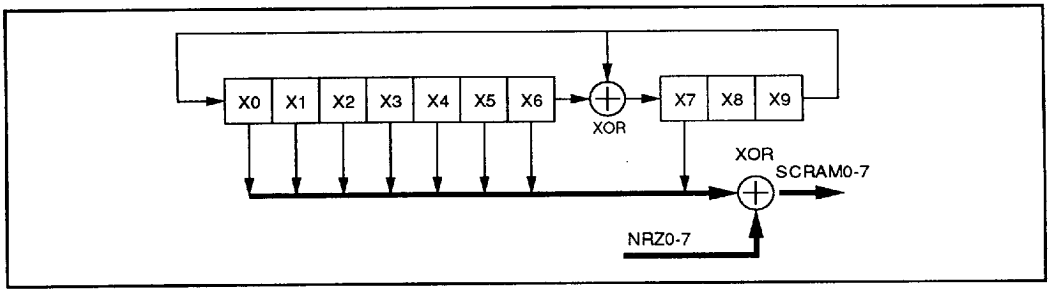


FIGURE 10: Scrambler Block Diagram

not reformat the data before passing it to and from the internal 8-bit bus. If nibble mode is selected, the NRZ interface circuit converts the 4 LSBs of the external 8-bit bus to the internal 8-bit bus. Only the selected NRZ interface is enabled and the unused bits can be left floating. Both the byte-wide and nibble interfaces define the most significant bit of the interface as the most significant bit of the data and the nibble interface defines the nibble clocked in or out as the most significant of the pair.

For both byte-wide and nibble operation, the NRZ write data is latched by the SSI 32P4910A on the rising edge of the WCLK input. The WCLK frequency must be appropriate for the data rate chosen or else overflow/underflow will occur. It is recommended that WCLK be connected to RCLK to prevent this from occurring. In byte-wide mode, as each NRZ byte is input to the SSI 32P4910A, its parity is checked against the controller supplied parity bit NRZP. If an error is detected, the PERR output pin goes high and remains high until WG/$\overline{WG}$ goes inactive.

In data read mode, the NRZ data will be presented to the controller near the falling edge of RCLK so that it can be latched by the controller on the rising edge of RCLK. When RG goes high, the selected NRZ interface will output low data until the sync byte has been detected. The first non-zero data presented will be the sync byte (69H). The NRZ interface is at a high impedance state when not in data read mode. In byte-wide mode, an even parity bit , NRZP, is generated for each output byte.

Write Precoder

The SSI 32P4910A implements a $1/(1 \oplus D^2)$ write precoder which is used to precode the serialized encoder data for PR4. The state of the precoder is preset to 0,0 upon exiting write mode. This guarantees that precoder will begin the next write in the 0,0 state. The state of the precoder is not guaranteed when the write data (WD/$\overline{WD}$) changes from sync field to encoded data. The result is that one of 2 different write data patterns or their inverses may be written for a particular write. All four of these patterns will decode properly upon read back. As a result of the fact that the write data toggle flip-flop is utilized as part of the precoder, the read/write amplifier connected to the SSI 32P4910A must not contain a T flip-flop. The precoder block diagram is shown below.

Write Precompensation

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognizes specific write data patterns and can add delays in the time position of write data bits to counteract the magnetic nonlinearity effect. The magnitude of the time shift, WPC, is programmable via the write precomp register and is made proportional to the time base generator's VCO period (i.e., data rate). The circuit performs write precompensation only on the second of two consecutive "ones" and only shifts in the late direction. If more than two consecutive "ones" are written, all but the first are precompensated in the late direction.

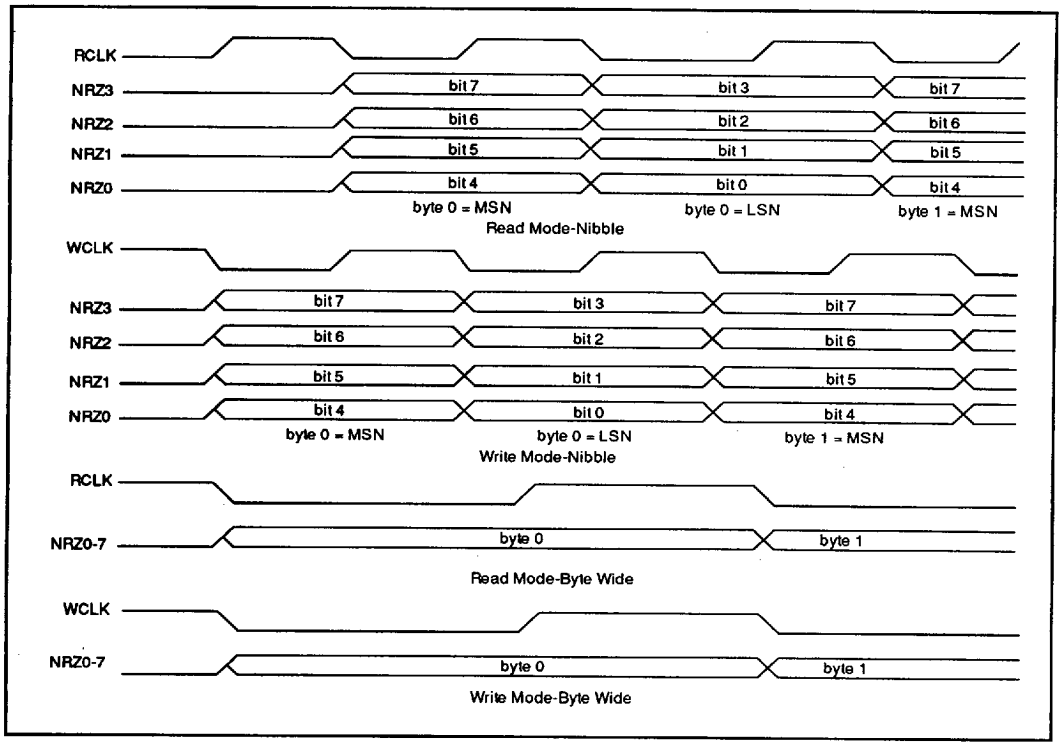


FIGURE 11: NRZ Timing

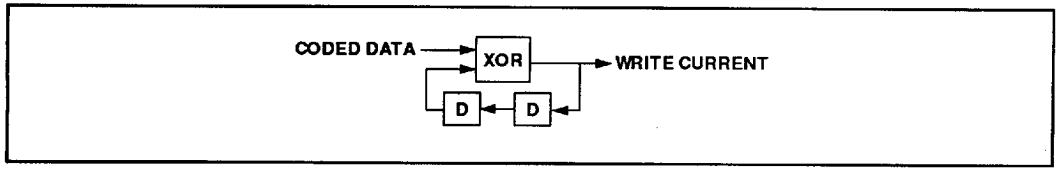


FIGURE 12: Precoder Block Diagram

FUNCTIONAL DESCRIPTION (continued)

SERVO DEMODULATOR CIRCUIT DESCRIPTION

Servo functionality is provided by two separate circuits: the servo demodulator circuit, and the previously described dual level pulse qualifier circuit. To support embedded servo applications, SSI 32P4910A provides a separate programmable registers for servo mode filter cutoff frequency, boost, and qualification threshold. The values programmed in these registers are selected upon entry into servo mode (SG = 1). Either the normal or the differentiated filter output can be routed to the servo demodulator by programming the Servo Mode Select (SMS) bit in the Data Rate Register. This bit also determines the polarity of the RDS/$\overline{\text{RDS}}$ output. In addition, the RDS/$\overline{\text{RDS}}$ pulse width and initial charge pump current is determined by the RDSPW bit in the Sample Loop Control Register and the SBCC bits in the Data Level Threshold Register respectively.

The servo demodulator circuit captures four separate servo bursts and provides an amplified and offset version of the voltages captured for each at the A, B, C, and D output pins respectively. The circuit uses a "Soft Landing" charge pump with programmable initial charge current to charge each of the internal 10 pF burst hold capacitors. This "soft landing"charge pump architecture minimizes the overshoot of the hold capacitor beyond the actual instantaneous peak voltage at the full wave rectifier output. Internal burst hold capacitors are provided to support low leakage burst capture and to reduce external component count. Burst capture control is provided by the STROBE and $\overline{\text{RESET}}$ input pins. In addition to the A, B, C, and D outputs pins, the circuit provides a maximum reference voltage at the MAXREF output pin. This reference voltage represents the maximum voltage that can be achieved at the A, B, C, and D output pins with a 1.4 Vp-p signal at the filter output and is typically used as the reference voltage for an external A/D converter.

Burst Capture

Burst capture is controlled by the signal applied to the STROBE input pin and an internal counter. The first pulse on the STROBE input pin causes the A burst hold capacitor to be charged by the charge pump. The capacitor charges for as long as the STROBE input is high or until the capacitor voltage reaches the peak voltage at the full wave rectifier output. On the falling edge of the STROBE signal, the internal counter is incremented. The next 3 STROBE pulses will charge the B, C, and D, hold capacitors respectively. After the falling edge of the fourth strobe, the counter is reset to zero and the burst capture can be repeated. The counter is also reset when the $\overline{\text{RESET}}$ input transitions low.

The voltage level on each hold capacitor is amplified by a factor of 3.33 and summed with a 0.27V DC reference to create the A, B, C, and D output signals. A 1.40 Vp-p differential voltage at the DP/DN pins will result in 1.40 • 0.6 • 3.33 = 2.80V peak burst amplitude (i.e., servo gain = 2.0). The MAXREF output pin is a nominal 3.2V and is internally divided by 12 to create the DC baseline of 0.27V.

Either the normal or differentiated filter output may be selected for full wave rectification for servo capture. If the Servo Mode Select (SMS) bit in the Data Rate Register is 0 then the normal filter outputs are used and if it is a 1, the differentiated filter outputs are used. If the differentiated output is selected, the polarity of the RDS/$\overline{\text{RDS}}$ pulse will be positive true otherwise RDS/$\overline{\text{RDS}}$ is negative true. The magnitude of the captured voltage on the burst hold capacitors is governed by setting of the 2-bit servo AGC DAC. The AGC voltage can be programmed from 1.1 to 1.40 Vp-pd.

All four of the internal hold capacitors are discharged when the $\overline{\text{RESET}}$ input is driven low. The $\overline{\text{RESET}}$ input overrides the STROBE signal. STROBE and $\overline{\text{RESET}}$ are not gated with SG.

The maximum charge pump current can be selected as 40, 80, 120 or 160 µA by setting the servo burst charge current (SBCC) bits in the Data Level Threshold register. The "Soft Landing" technique reduces the charge pump current as the error between the voltage on the hold capacitor and the full wave rectifier output becomes smaller. This reduces the possibility of overcharging the capacitor during the comparator's propagation delay period.

A small leakage current is applied to the capacitor being charged during each strobe period to make the captured voltage less sensitive to noise and strobe timing. The magnitude of this current is 1/450 of the charge current.

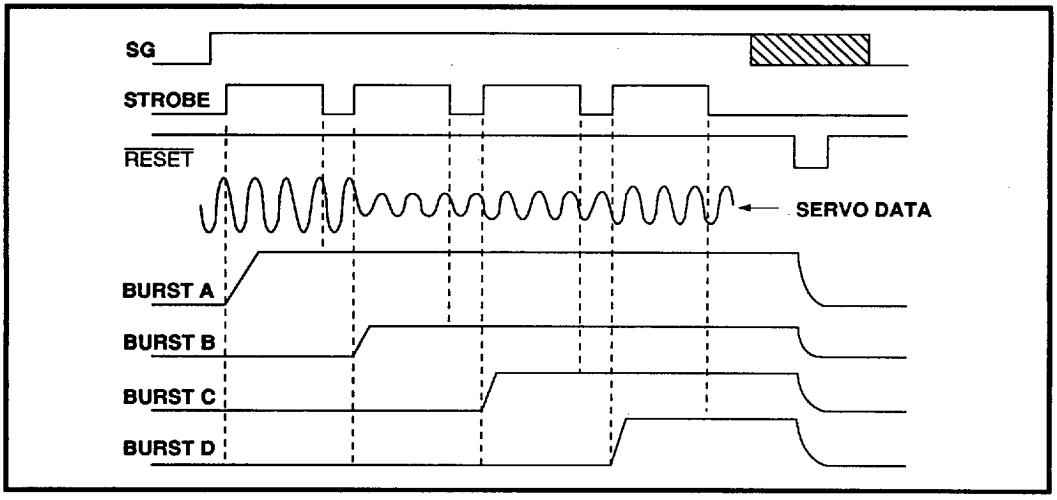


FIGURE 13: Servo Capture Timing Diagram

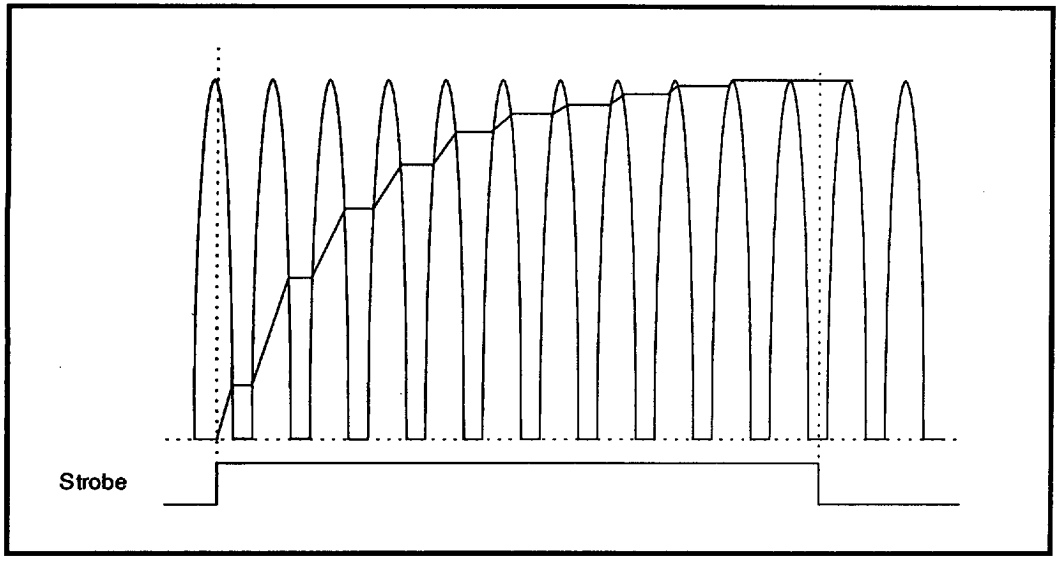


FIGURE 14: Servo Burst Aquisition (SG= $\overline{\text{RESET}}$ = 1)

FUNCTIONAL DESCRIPTION (continued)

SERVO TIMING OUTPUTS

The dual level qualifier that was previously described is used to generate the RDS/$\overline{\text{RDS}}$ and PPOL timing signals. The RDS/$\overline{\text{RDS}}$ output pin pulses low for each positive or negative servo peak that is qualified by the dual level qualifier. The pulse width of RDS/$\overline{\text{RDS}}$ may be selected as either 15 ns or 27 ns with the RDSPW bit in the Sample Loop Control Register. The PPOL output pin provides the pulse polarity information for the qualified peaks, where PPOL=1 for a positive peak and PPOL=0 for a negative peak. To reduce noise propagation, the RDS/$\overline{\text{RDS}}$ and PPOL outputs are only active in servo mode.

SERIAL PORT CIRCUIT DESCRIPTION

The serial port interface is used to program the SSI 32P4910A's seventeen internal registers. The serial port is enabled for data transfer when the Serial Data Enable (SDEN) pin is high ("1"). SDEN must be asserted high prior to any transmission and it should remain high until the completion of the transfer. At the end of each transfer SDEN should be brought low ("0").

When SDEN is high, the data presented to the Serial Data (SDATA) pin will be latched into the SSI 32P4910A on each rising edge of the Serial Clock (SCLK). Rising edges of SCLK should only occur when the desired bit of address or data is being presented on the serial data line. Serial data transmissions must occur in 16-bit packets. If more than 16 rising edges of SCLK are received during the time that SDEN is high, only the last 16 are considered valid. For all valid transmissions, the data is latched into the internal register on the falling edge of SDEN.

Each 16-bit transmission consists of a read/write control bit (must always set R/$\overline{\text{W}}$ = "0", i.e. write only) followed by 3 device select bits, 4 address bits and eight data bits. The device select and address bits select the internal register to be written to. The device select, address and data fields are input LSB first, MSB last, where LSB is defined as Bit 0. The three device select bits select the type of device on the SSI serial bus to be communicated with and must be set to S0 = 0 or 1 (depending on register to be selected), S1 = 1, and S2 = 0 when communicating with the SSI 32P4910A. The figure below shows the serial interface timing diagram.

DESCRIPTION OF OPERATING MODES

The fundamental operating modes of the SSI 32P4910A are controlled by the Servo Gate (SG), Read Gate (RG), and Write Gate (WG/$\overline{\text{WG}}$) input pins. The exclusive assertion of any these inputs causes the device to enter that mode. If none of these inputs is asserted, the device is in the idle mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG/$\overline{\text{WG}}$. The mode that is overriding takes effect immediately.

RG and SG are asynchronous inputs and may be initiated or terminated at any position on the disk. WG/$\overline{\text{WG}}$ is also an asynchronous input, but should not be terminated prior to the last output write data (WD/$\overline{\text{WD}}$) pulse.

Idle Mode Operation

If SG, RG, and WG/$\overline{\text{WG}}$ are not active, the SSI 32P4910A is in idle mode. When in idle mode, the time base generator and the Data Separator PLL are running and the Data Separator PLL is phase-frequency locked to the TBG VCO output. The AGC, continuous time filter, and pulse qualifiers are active but the outputs of the pulse qualifiers are disabled. The continuous time filter is using its programmed values for cutoff frequency and boost determined by the data mode registers. The AGC operation is the same as in the VCO preamble portion of a data read. Servo burst capture is operational in idle mode but the filter and AGC settings are for data reads and not for servo reads as would be the case if the device was in servo mode. The RDS/$\overline{\text{RDS}}$ and PPOL outputs are disabled in idle mode.

Servo Mode Operation

If SG is high, the device is in the servo mode. This mode is the same as idle except that the filter cutoff and boost settings are switched from those programmed for data read mode to those programmed for servo mode, the AGC is switched to servo mode, and the RDS/$\overline{\text{RDS}}$ and PPOL and outputs are enabled. The assertion of SG causes read mode, write mode, and the power down register settings for the front end to be overridden.

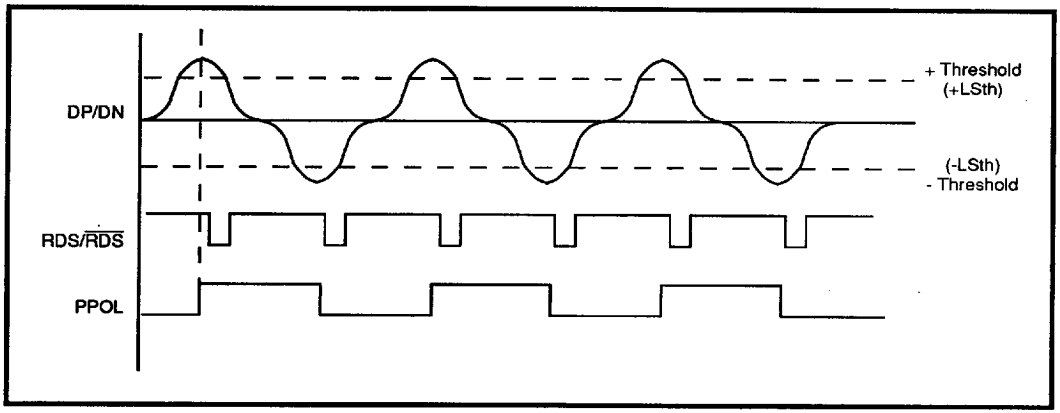


FIGURE 15: RDS/RDS and PPOL vs. DP/DN Relationship

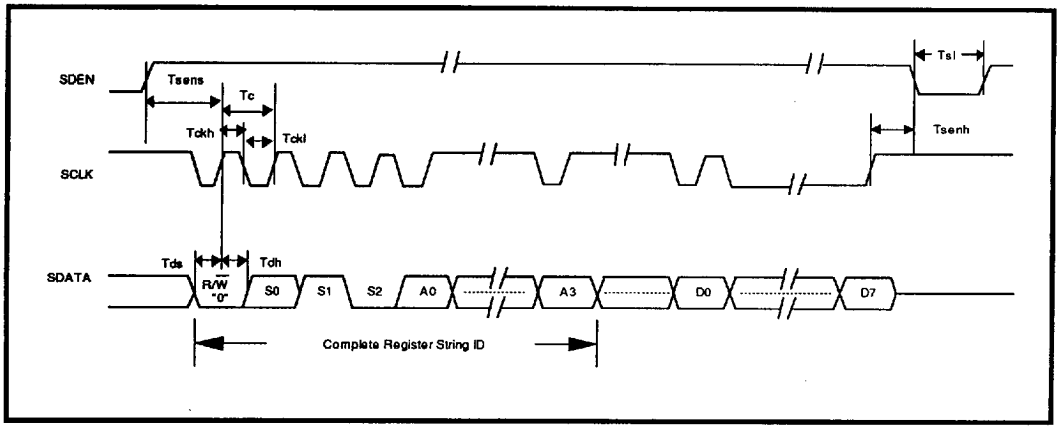


FIGURE 16: Serial Interface Timing

DESCRIPTION OF OPERATING MODES (continued)

Write Mode Operation

The SSI 32P4910A supports three different write modes; Normal write mode, direct write mode #1 and direct write mode #2. The direct write modes require that either the direct write bit , bit 0 of the control operating register, or the $\overline{DWR}$ pin be active. All three write modes require that the data separator be powered on. The active polarity of write gate can be selected by programming the WGP bit in the Control Operating Register. The $\overline{PDWN}$ input should be kept low until all registers are properly loaded to prevent an illegal write operation at power up.

Normal Write Mode

The SSI 32P4910A is in the normal write mode if WG/$\overline{WG}$ is active, $\overline{DWR}$ is high, and the direct write bit in the Control Operating Register is low. A minimum of one NRZ time period must elapse after RG goes low before WG/$\overline{WG}$ can be set active. The data separator PLL is phase-frequency locked to the TBG VCO output in this mode.

In normal write mode, the circuit first auto generates the VCO sync pattern, then scrambles the incoming NRZ data from the controller, encodes it into 8,9 GCR formatted data, precodes it, precompensates it, feeds it to a write data toggle flip-flop, and outputs it to the preamp for storage on the disk. When WG/$\overline{WG}$ goes inactive, the WD/$\overline{WD}$ outputs remain enabled but the active pull down current is reduced by a factor of 7 to reduce power consumption and the write data flip-flop is reset to guarantee that the WD/$\overline{WD}$ outputs represent a zero state.

In normal write operation, when the write gate (WG/$\overline{WG}$) goes active, the VCO sync field generation begins which causes a continuous "2T" pattern at the WD/$\overline{WD}$ outputs {(1,1,-1,-1,1,1,-1,-1...) in the write current domain}. The NRZ inputs must be low and must be held low for the duration of the VCO sync field generation. The minimum required sync field is equivalent to 8 byte times.

The SSI 32P4910A also allows the precoder to be preset when the first training byte arrives at the precoder. With Control Operating Mode Register #2 bit 3 (TME) and bit 0 (PCFDIS) set to 0, the SSI 32P4910A allows presetting of the precoder. Bit 2 (PFSPOL) of the Control Operating Mode Register #2 allows the precoder to be preset if PFSPOL is set to 1 and reset if set to 0.

Training and Sync Byte Generation

The SSI 32P4910A supports two modes of sync byte detection, single byte and dual "or" byte, and two modes of training and sync byte generation, manual and semi-automatic. The manual mode is generally recommended because it can be used for either dual or single sync byte detection and provides more flexibility in altering the number of training bytes to be written. The semi-automatic mode can only be used to generate an internally fixed number of training bytes and a single sync byte, but saves controller state machine space.

Manual Mode

In the manual mode, the device will continue to autogenerate the sync field pattern until a 93H is latched at the NRZ interface, and detected. The device encodes the 93H pattern and writes the result as the training pattern.

For the single sync byte detection mode, a recommended minimum of 5 bytes of 93H must be written to the NRZ interface to write the 5-byte equalizer training pattern. Next, the NRZ data must be changed to 69H for 1 byte time to write the single sync byte.

For the dual sync byte detection mode, a recommended minimum of 4 bytes of 93H must be written to the NRZ interface to write the minimum 4-byte equalizer training pattern. The NRZ data must then be changed to 1FH for one byte time to write the first sync byte. The NRZ data must then be changed to 93H for one byte time to write a training/propagation byte. Next, the NRZ data must be changed to 69H for one byte time to write the second sync byte.

DESCRIPTION OF OPERATING MODES (continued)

Semi-automatic Mode

In the semi-automatic mode, the device will continue to autogenerate the sync field pattern until a FFH is latched at the NRZ interface, and detected. The device then internally generates the encoded 93H pattern for 5 byte times and writes the result as the training pattern. It then internally generates the encoded 69H pattern for 1 byte time to write the single sync byte. To maintain proper controller synchronization, the FFH should be presented at the NRZ interface for a total of 6 byte times. Note that the semi-automatic mode can only be used to write single sync byte format and the training pattern length is fixed at 5. This mode is useful if controller state machine space is extremely limited.

User Data

The user data must be presented at the NRZ interface immediately following the last NRZ sync byte written. Finally, after the last byte of user data has been clocked in, the WG/$\overline{WG}$ must remain active for a minimum of 16 NRZ bit times in byte-wide mode to ensure that the device is flushed of data (The delay is 21 NRZ bit times in nibble mode). WG/$\overline{WG}$ can then go inactive. WD/$\overline{WD}$ stops toggling a maximum of 2 NRZ (RCLK) time periods after WG/$\overline{WG}$ goes inactive.

Direct Write Mode #1

In this direct write mode, the NRZ data from the byte-wide interface bypasses the scrambler, the 8,9 encoder and the precoder, but is precompensated before going to the write data flip-flop and then to the WD/$\overline{WD}$ output pins. The RCLK output is changed from 9 VCO clock periods to 8 VCO clock periods with a 3/8 duty cycle. The purpose of routing the signal to the precomp circuit is to generate a return to zero pulse every time a "1" occurs in the data so that the write data flip-flop is toggled. WCLK is not required to latch the byte-wide NRZ data into the NRZ interface since the data is latched by an internal version of RCLK, but the NRZ data must be valid no later than 12 ns after the rising edge of the RCLK output pin. Direct write mode #1 is selected by setting the DW bit (bit 0) in the Control Operating Register and is entered when the WG input is active. This mode is not valid when using the nibble NRZ interface. Note that direct write mode #2 will override direct write mode #1.

Direct Write Mode #2

In this direct write mode, the data presented at the DWI/$\overline{DWI}$ input pins directly toggles the write data flip-flop which drives the WD/$\overline{WD}$ output pins. No WCLK is required in this mode, and the WD/$\overline{WD}$ output is not resynchronized. Direct write mode #2 is selected by driving the $\overline{DWR}$ input low and is entered when the WG/$\overline{WG}$ input is active. Note that the direct write mode #2 will override direct write mode #1.

Data Read Mode Operation

Data read mode is initiated by setting the Read Gate (RG) input pin high. This action causes the data synchronizer to begin acquisition of the clock from the incoming VCO sync pattern. To achieve this, the data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the sample clock. This PLL is normally locked to the time base generator output, but when the Read Gate input (RG) goes high, the PLL's reference input is switched to the filtered incoming read signal.

Acquisition of DS VCO Sync

When the Read Gate input is asserted, the read sequence is initiated. At this time an internal counter begins counting the pulses that are qualified by the dual level pulse qualifier given the polarity changes of the incoming 1,1,-1,-1,1,1 read back pattern defined by the VCO sync field. When the count reaches 4, the internal read gate is asserted and the DS PLL input is switched from the TBG's VCO output to the sampled data input. This is also the point at which the DS PLL's phase detector is switched from the phase-frequency detector to the decision directed phase detector. The counter is also used to determine whether the selected sync field count, SFC, has been achieved. When the counter reaches the value specified by SFC, the data synchronizer PLL is assumed to be locked and settled (VCO lock). Also at SFC, the phase detector gain switch and the AGC mode switch occur. To allow for different preamble lengths, the SFC can be set to 64, 80, 96 or 128 from the Sample Loop Control Register. These values for the SFC may be thought of as the number of code clock periods in the sync field, but they actually represent twice the number of incoming polarity changes required.

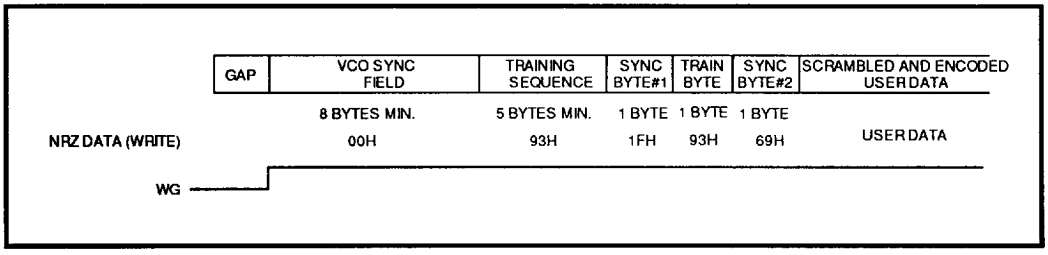


FIGURE 17: Hard Sector Write Sequence - Dual Sync

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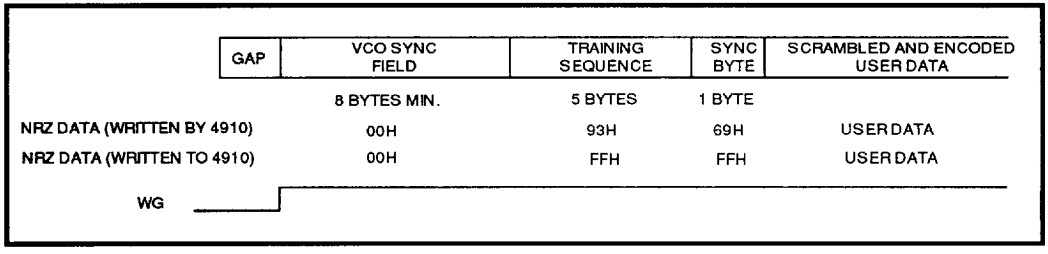

FIGURE 18: Hard Sector Semi-Auto Write Mode

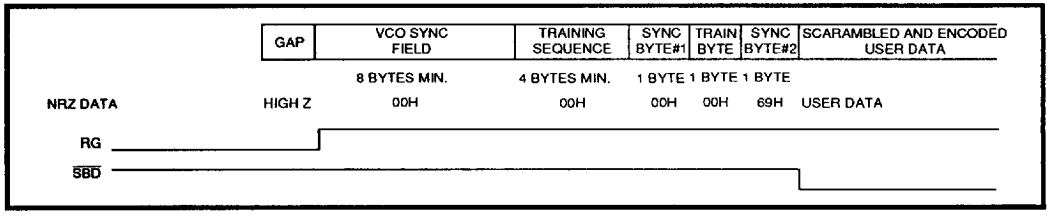

FIGURE 19: Read Sequence - Dual Sync Byte Mode

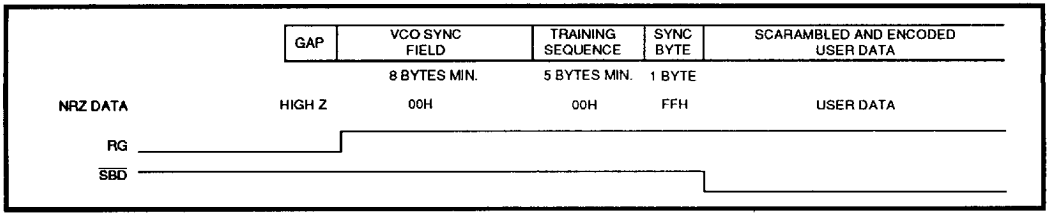

FIGURE 20: Semi-Auto Sector Read Mode

DESCRIPTION OF OPERATING MODES (continued)

VCO Lock, PD Gain, AGC Mode Switch, and Code Word Boundary Detector Enable

At SFC, one of two phase tracking methods will be chosen depending on the Enable Phase Detector Gain Switching (GS) bit in the Control Operating Mode Register. When the GS bit is high, the phase detector gain is reduced by a factor of 6 or 10 as dictated by the GS_10 bit after the SFC count is reached. When the GS bit is low, no phase detector gain switching takes place.

Also after SFC, the AGC feedback will be switched from the continuous time fullwave rectifier to sampled data feedback.

At SFC, the internal VCO lock signal activates the code word boundary detection circuitry to define the proper decode boundaries. Also, at count SFC, the RCLK generator source switches from the TBG's VCO output to the DS VCO clock signal which is phase locked to the incoming read data samples. The DS VCO is assumed locked to the incoming read samples at this point. At SFC a maximum of 1 RCLK time period may occur for the RCLK transition, however, no short duration glitches will occur. After the code word detection circuitry finds the proper code word boundary, the RCLK generator is again resynchronized to guarantee that the RCLK is in sync with the data. The RCLK output will not glitch and will not toggle during the RCLK generator resynchronization for up to 2 byte times maximum.

Also at the code word boundary detect, the internal 9-bit code words are allowed to pass to the ENDEC for decoding. This decoding will occur until read gate is deasserted.

Adaptive Equalizer Training Sequence

Training Sequence For Single Sync Byte Mode

As was previously discussed, in a single sync byte type write sequence, a minimum of 5 bytes of NRZ 93H and one byte of 69H must be written between the end of the VCO sync field and the beginning of the user data. The 5 bytes of 93H are 8,9 encoded and precoded during write mode to produce the adaptive equalizer training pattern. During read mode, the encoded 93H sequence (100110011 read data sequence) and the encoded 69H are used to adaptively train the inner two taps of the five tap transversal filter in a zero forcing manner. The error at the filter output is integrated to derive the tap weight multiplying coefficient, Km1. Both of these inner taps use the same Km1. It is anticipated that the continuous time filter will be used for coarse equalization and that transversal filter will be used adaptively for fine tuning. This will reduce Km's range and accuracy requirements. Since there are encoded user data patterns that will not produce an equalizer correction error, an equalization hold during data mode can be selected from the Sample Loop Control Register. If the equalizer is programmed to adapt only during the training sequence, the sync byte detect signal is used to hold the Km1 value. After the training pattern, if the loop is active during user data, the equalizer loop gain will be reduced by 7. The loop's integration time constant is made inversely proportional to the selected data rate.

The Km1 coefficient can be held at the present instantaneous value by asserting the EQHOLD input. If EQHOLD is asserted, the Km1 value will not be changed by either exiting read mode, subsequent training patterns, or by subsequent data patterns. When EQHOLD is deasserted, the equalizer will resume its normally programmed functionality. The Km1 value can be held with reasonable accuracy for up to 10 ms to make the number of code periods required for acquisition data rate independent.

Training Sequence For Dual Sync Byte Mode

The adaptive equalizer training used for the dual sync byte detection mode is the same as that used in the single sync byte mode except that the adaptation occurs over the 4 encoded 93H bytes, sync byte #1 (1FH), another 93H and sync byte #2 (69H). This occurs because the Sync Byte Detect ($\overline{SBD}$) is what disables the adaptation if adaptation is enabled only during the training sequence. The number of consecutive 93H training bytes may be reduced in dual sync byte mode because the sync byte #1 has been chosen to have the same training properties as the 93H training byte.

Sync Byte Detect and NRZ Output

The SSI 32P4910A implements a dual "or" type sync byte detection which offers increased sync byte detection capability while maintaining backward compatibility with the single sync byte format and detection. The two bytes of the dual sync byte are separated by a training byte to allow for Viterbi error propagation that may be caused by an error in the first sync byte. The training byte 93H was chosen to provide the adaptive equalizer an ideal training signal.

As the read data is 8,9 decoded, it is compared to one of two internally fixed sync bytes (1FH or 69H). If the 1FH byte is found, the $\overline{SBD}$ output will go low 18 code clocks (2 byte times) later and the 69H byte will be the first non-zero byte presented at the NRZ interface. If a match of the 69H byte is the first found, the sync byte detect ($\overline{SBD}$) pin goes low and the NRZ output data that until now was held low, is changed to 69H. The next byte presented on the NRZ outputs is the first byte of user data. $\overline{SBD}$ will remain low and NRZ data will continue to be presented at the NRZ interface until the read gate is deasserted at which point $\overline{SBD}$ goes high and the NRZ outputs go to a high impedance state.

Surface Defect Scan Mode

The SSI 32P4910A helps check for media defects using the surface defect scan mode. In order to use this mode the part must have the byte-wide interface enabled. In write mode, all zeros are presented (written) at the NRZ interface. When this pattern is to be read back, bit 7 (DSE bit) of the N counter register is enabled which enables the surface defect scan mode. The survival sequence register must also be turned off (BYPSR bit). In this mode, $\overline{SBD}$ will transition low at SFC. The NRZ7 pin is monitored. If no defect occurs, the NRZ7 pin will stay low. If a defect occurs, the NRZ7 pin will transition high on the falling edge of RCLK and stay high as long as the defect is present, transition back low on the next falling edge of RCLK when the defect is not present.

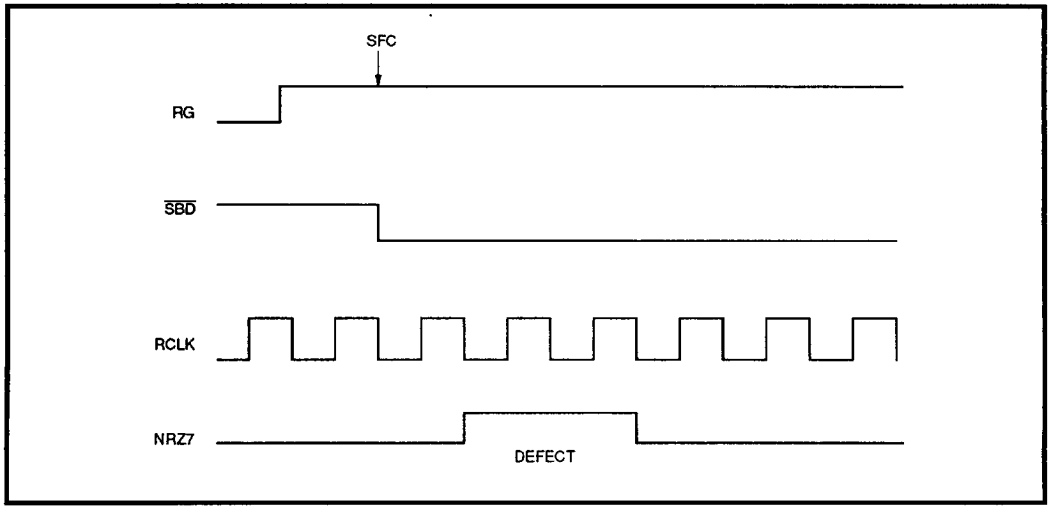

FIGURE 21: Surface Defect Scan Mode

FUNCTIONAL DESCRIPTION (continued)

POWER DOWN OPERATION

The power management modes of the SSI 32P4910A are determined by the states of the power down register bits and the $\overline{\text{PDWN}}$ and SG inputs. The individual sections of the chip can be powered down or up using the Power Down Register. A high level in a Power Down Register bit disables that section of the circuit. The power down information from the Power Down Register takes effect immediately after the SDEN pin goes low.

When the $\overline{\text{PDWN}}$ input is low, the chip goes into full power down mode regardless of the power down register settings or the state of the SG input.

When $\overline{\text{PDWN}}$ is high, SG will force the AGC, filter, and pulse qualifier circuits (front end) to be active by overriding the front end register bit. The back end power down register bits, which include the Data Separator and Time Base Generator are not affected by the SG input.

The serial port is active in all power down modes.

The time to restart from a full power down is dependent on the PLL loop filter and the data rate.

The truth table for the various modes of operation is shown below:

SG, $\overline{\text{PDWN}}$	1,1	1,0	0,1	0,0
Front End	ON	OFF	R	OFF
Data Separator	R	OFF	R	OFF
Time Base Generator	R	OFF	R	OFF
Serial Port	ON	ON	ON	ON

R = Controlled by register bit.

(Register bit =1 turns circuits OFF,
Register bit = 0 turns circuits ON)

REGISTER DESCRIPTION

SERIAL PORT REGISTER DEFINITIONS

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/W	
Power Down Register (PD)	0	0	0	0	0	1	0	0	04H
	Bits 7-6	TPC/ D1-0	Test point C/D/E control (TME = 0) TPC+/TPC- TPD+/TPD- TPE 0X = disabled disabled disabled 1X = DP/DN CP/CN disabled SG = 1 1X = disabled disabled disabled SG = 0 Test point C/D/E control (TME = 1) TPC+/TPC- TPD+/TPD- TPE (AGCSEL=0) TPE (AGCSEL=1) 00*= Servo mode calibration 01 = DP/DN CP/CN full write rectifier out low-z oneshot as input to qualifiers, etc. 10 = DP/DN CP/CN full wave rectifier out fastrec oneshot output mode from filter/offset canceller 11 = filter bypass filter bypass full wave rectifier out ultra fast decay control							
	Bits 5-4	ATOSEL	Output select for ATO test point 00 = MAXREF/2 01 = DAC output enabled DAC test mode 10 = Amplitude Asymmetry Monitor output (QASYM) selected 11 = Channel Equalization Monitor output (Q) selected						
	Bit 3	ACCPL	Internal AC coupling enable/disable (TME = 0) 0 = Internal AC coupling, AGC switched to sampled mode at SFC 1 = Internal AC coupling, AGC is always in continuous mode Internal AC coupling enable/disable (TME = 1) 0 = Internal AC coupling is enabled, AGC as per TME = 0 state 1 = Internal AC coupling is disabled						
	Bit 2	TB	Time Base Generator power down 0 = power up; 1 = power down						
	Bit 1	DS	Data Separator power down 0 = power up; 1 = power down						
	Bit 0	PD	AGC, Filter, Pulse Detector, and Servo power down 0 = power up; 1 = power down						

* Servo calibration mode enabled, strobing must occur for operation.

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SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/W	
Data Filter Cutoff Register (FC)	0	0	0	1	0	1	0	0	14H
	Bit 7	3 TAPEN	3 Tap equalizer enable						
			0 = Enable 5 tap equalizer (Normal operation) 1 = Enable only 3 tap equalizer (4901 mode)						
	Bits 6-0	FC6-0	Filter cutoff frequency setting in non-servo mode fc (MHz) = 0.301 • FC – 1.142 44 ≤ FC ≤ 117_{dec}						
Servo Filter Cutoff Register (FCS)	0	0	1	0	0	1	0	0	24H
	Bit 7	PDM	Servo Peak Detector mode 0 = Window qualifier 1 = Hysteresis qualifier						
	Bits 6-0	FCS6-0	Filter cutoff frequency setting in servo mode fc (MHz) = 0.277 • FCS +0.08 14 ≤ FCS ≤ 43_{dec}						
Data Filter Boost Register (FB)	0	0	1	1	0	1	0	0	34H
	Bit 7	LZTC	Non low-Z vs. low-Z time constant 0 = 15:1 1 = 5:1						
	Bits 6-0	FB6-0	Filter boost setting in data mode Boost (dB) = 20 • log[0.021848 • FB + 0.000046 • FB • FC +1] 0 ≤ FB ≤ 127_{dec}						
Servo Filter Boost Register (FBS)	0	1	0	0	0	1	0	0	44H
	Bits 7-6	FBS 1-0	Filter boost setting in servo mode 00 = 0 dB 01 = 2 dB 10 = 4 dB 11 = 6 dB						
	Bits 5-0	FGD5-0	Filter group delay Δ % in all modes Group delay Δ % = 0.9783 • (FGD 4-0) • -0.665, where FGD5 = 1 is positive, 0 is negative 0 ≤ FGD ≤ 31_{dec}						
Viterbi Detector Threshold Register (VDT)	0	1	0	1	0	1	0	0	54H
	Bit 7	BYPSR	Survival Sequence Register Bypass / Write Precode Bypass 0 = Bypass disabled (normal operation) 1 = Bypass enabled						
	Bits 6-0	VD6-0	Viterbi qualification threshold voltage Vth (mV) = 7.874 • VD 45 ≤ VD ≤ 127_{dec}						

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register ID String	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Data Level Threshold	0	1	1	0	0	1	0	0	64H
Register (LD)	Bits 7-6	SBCC1-0	Initial Servo Charge Pump current 00 = 40 µA 01 = 80 µA 10 = 120 µA 11 = 160 µA						
	Bits 5-0	LD5-0	Data level qualification threshold voltage If WP/LT register: ALE = 0 (fixed levels) Prior to SFC: Lth (mV) = 10.47 • LD after SFC: Lth (mV) = 7.44 • LD $16 \le LD \le 63_{dec}$ If WP/LT Register: ALE = 1 (adaptive levels) After SFC: Lth (%) = 1.574 • LD						
Servo Level Threshold	0	1	1	1	0	1	0	0	74H
Register (LDS)	Bits 7-6	SAGC LVL1-0	Servo mode AGC level control 00 = 1.40 Vp-pd 01 = 1.30 Vp-pd 10 = 1.20 Vp-pd 11 = 1.10 Vp-pd						
	Bits 5-0	LDS5-0	Servo level qualification threshold voltage LSth (mV) = 10.47 • LDS						
Control Test Mode	1	0	0	0	0	1	0	0	84H
Register (CT)	Bit 7	EFR	Sample clock source 0 = Sample clock is from the DS VCO, normal opera tion 1 = Sample clock is from the TBG output, a test mode						
	Bit 6	ECP	Factory Reserved Bit, must be set to 0 in application (enables charge pump)						
	Bits 5-3	TP3-1	Multiplexed test point selection						

TP3	TP2	TP1	Function	TPA+, TPA-	TPB+, TPB-
0	0	0	Test points off	high impedance	high impedance
0	0	1	Survival out/In	SSOUT A, B (sngl)	SSIN A+, A- (sngl)
0	1	0	Eq cont/phase det	equalizer control (diff)	phase detect out (diff)
0	1	1	Viterbi survival In	SSIN B+,B- (sngl)	SSIN A+, A- (sngl)
1	0	0	Equalizer outputs	Equalizer A (diff)	Equalizer B (diff)
1	0	1	EQ out/survival In	Equalizer A (diff)	SSIN A+, A- (sngl)
1	1	0	EQ out/survival out	Equalizer A, B (sngl)	SSOUT A, B (sngl)
1	1	1	EQ out/VCO/2	Equalizer A, B (sngl)	DS VCO/2 (diff) for RG = 1
			EQ out/TBG out	Equalizer A, B (sngl)	TBG out (diff) for RG = 0

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register Mode	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Control Test Mode Register (CT) (continued)	Bit 2	RCK2X/ VRDT	Enable double RCLK drive (TME = 0) at Byte wide NRZ interface 0 = RCLK drive at 1x 1 = RCLK drive at 2x Enable VRDT input (TME = 1) 0 = Viterbi survival outputs to the data decoder, normal use 1 = Digital input to the data decoder, used in testing only						
	Bit 1	DT	0 = Not in pump down test mode 1 = Digital input to the data decoder, for test only						
	Bit 0	TT/UT	Training Termination 0 = Terminate training when $\overline{SBD}$ goes low 1 = Terminate training 4 bytes after framing Enable TBG pump up (TME = 1) 0 = Not in pump up test mod 1 = Continuous pump up, for test use only FLTR1+ sources current; FLTR1- sinks current						
N Counter Register (N)	1	0	0	1	0	1	0	0	94H
	Bit 7	DSE	Defect scan enable 0 = Normal operation 1 = Defect scan mode enabled						
	Bits 6-0	N6-0	N counter $2 \leq N \leq 127$						
M Counter Register (M)	1	0	1	0	0	1	0	0	A4H
	Bits 7-0	M7-0	M counter $2 \leq M < 255$ FTBG = FREF • [(M+1) ÷ (N+1)]						
Data Rate Register (DR)	1	0	1	1	0	1	0	0	B4H
	Bit 7	SMS	Servo mode select 0 = Capture uses normal filter output and RDS is active low (normal operation) 1 = Capture uses differentiated filter output and RDS is active high						
	Bits 6-0	DR6-0	Fvco (MHz) = 9/8 data rate = 1.143 • DR + 4.986 for RR = 10 kΩ Fvco (MHz) = 9/8 data rate = 0.948 • DR + 1.831 for RR = 12.1 kΩ $37 \leq DR \leq 127$						

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register ID String	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Write Precomp / Level Threshold Time Constant Register (WPLT)	1	1	0	0	0	1	0	0	C4H
	Bits 7-6	TC2-1	Adaptive level qualification threshold time constant for decision directed phase detector. (Valid After SFC)						
	TC2		TC1		Time Constant				
	0		0		200 ns				
	0		1		400 ns				
	1		0		600 ns				
	1		1		800 ns				
	Bit 5	ALE	Enable adaptive level qualification in decision directed phase detector 0 = Fixed level qualification 1 = Adaptive mode						
	Bit 4	FREZQ	Freeze Channel quality factor and asymmetry factor at sync byte detect 0 = Update during read 1 = Freeze at $\overline{SBD}$						
	Bits 3-0	WPC3-0	Write precomp setting						

WPC3	WPC2	WPC1	WPC0	Write Precomp magnitude
0	0	0	0	no precomp
0	0	0	1	2.1% code period shift
0	0	1	0	4.2% code period shift
0	0	1	1	6.3% code period shift
0	1	0	0	8.4% code period shift
0	1	0	1	10.5% code period shift
0	1	1	0	12.6% code period shift
0	1	1	1	14.7% code period shift
1	0	0	0	16.8% code period shift
1	0	0	1	18.9% code period shift
1	0	1	0	21.0% code period shift
1	0	1	1	23.1% code period shift
1	1	0	0	25.0% code period shift
1	1	0	1	27.3% code period shift
1	1	1	0	29.4% code period shift
1	1	1	1	31.5% code period shift

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register ID String	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Control Operating	1	1	0	1	0	1	0	0	D4H
Register (CM1)	Bit 7	AUTOTR	Enables semi-automatic training and sync byte generation 0 = Disabled (normal operation) 1 = Enabled (single sync byte only)						
	Bit 6	AGCSEL	Selects AGC control mode 0 = Direct mode, i.e., external control signals must be provided 1 = Timed mode, i.e., control provided by one shot timing from SG & WG/$\overline{WG}$						
	Bit 5	WGP	Write gate polarity 0 = Active high, (normal operation) 1 = Active low						
	Bit 4	NIB	Enable Nibble interface 0 = Nibble interface disabled, i.e., byte-wide interface enabled 1 = Nibble (NRZ3-0) interface enabled						
	Bit 3	$\overline{BT}$	Bypass Time Base Generator 0 = Data synchronizer reference frequency is TBG output, (normal operation) 1 = Data synchronizer reference frequency is FREF input						
	Bit 2	SD	Disable Data Scrambler/Descrambler 0 = enabled, (normal operation); 1 = disabled						
	Bit 1	GS	DS Phase Detector gain switching 0 = enabled, (normal operation); 1 = disabled						
	Bit 0	DW	Enable direct write from byte-wide NRZ (bypasses scrambler & ENDEC) 0 = disabled, (normal operation); 1 = enabled						

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register ID String	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Sample Loop Control Register (SLC)	1	1	1	0	0	1	0	0	E4H
	Bit 7	RDSPW	RDS output pulse width 0 = 15 ns 1 = 27 ns						
	Bits 6-5	SFC1-0	Sync field count						
	SFC1	SFC0	Sync field count (code clocks)						
	0	0	64						
	0	1	80						
	1	0	96						
	1	1	128						
	Bit 4	AEGS	Adaptive Equalizer loop time constant shift 0 = Equalizer loop time constant same in preamble & data fields 1 = Equalizer loop time constant is increased to 7X in the data field relative to the preamble field, i.e., loop gain is reduced to 1/7						
	Bit 3	AED	Enable Adaptive Equalizer on data field 0 = Adaptive equalizer disabled after preamble field 1 = Adaptive equalizer in use after preamble field, if AEE bit = 1						
	Bit 2	AEE	Enable Adaptive Equalizer 0 = Adaptive equalizer disabled 1 = Adaptive equalizer enabled for use in preamble field, and after the preamble field if AED bit = 1						
	Bits 1-0	AGC1-0	AGC Charge Pump current in sampled AGC mode AGC charge/discharge current (μA) = 2.66 • AGC • DR/RR(kΩ) $37 \le DR \le 127$, RR = 10 kΩ e.g., for DR = 100 and AGC = 10 = 2_{dec} charge pump current = 53 μA						
Damping Ratio Control Register (DRC)	1	1	1	1	0	1	0	0	F4H
	Bit 7	GS_10	Data separator PLL gain shift factor 0 = 6 1 = 10						
	Bits 6-0	D6-0	Damping amplifier gain A = DRC • (0.8 / 127) Damping ratio = $\frac{A \cdot KVCO \cdot 0.25}{2\,\omega_n}$						

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register ID String	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Control Operating Mode	0	0	0	0	0	1	1	0	06H
Register #2 (CM2)	Bits 7-4	KM3-0	Equalizer outer tap coefficient km2 km2 = 0.0168 • KM (KM in 2's compliment) 0111 = +0.117 0110 = +0.101 0101 = +0.0840 0100 = +0.0672 0011 = +0.0504 0010 = +0.0336 0001 = +0.0168 0000 = 0 1111 = -0.0168 1110 = -0.0336 1101 = -0.0504 1100 = -0.0672 1011 = -0.0840 1010 = -0.1010 1001 = -0.1170 1000 = -0.1350						
	Bit 3	TME	Test Mode Enable 0 = TPC and TPD active when SG = 1 and bit 7 of Power Down Control Register is 1 1 = TPC and TPD as set by bits 6 and 7 of the Power Down Control Register						
	Bit 2	PFSPOL	Precoder Force State 0 = Precoder state set to 0 1 = Precoder state set to 1						
	Bits 1-0	QTC1-0	Qasym and Q Time Constant Control (TME = 1) Qasym — Q 00 =100 ns — 50 ns 01 =200 ns — 100 ns 10 =400 ns — 200 ns 11 =800 ns — 400 ns						
	Bit 0	PCFDIS	Precoder Force Disable (TME = 0) 0 = Precoder initialization enabled 1 = Precoder initialization disabled						

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	–	AGC/Filter analog circuit supply
VPF	–	Time Base Generator PLL ECL plus write pre-comp supply (connect to analog supply)
VPT	–	Time Base Generator PLL analog circuit supply
VPP	–	Data Separator PLL analog circuit supply
VPD	–	TTL Buffer I/O digital supply
VPC	–	Internal ECL, CMOS logic digital supply
VPS	–	Sampled data processor supply
VNA	–	AGC/filter analog circuit ground
VNF	–	Time Base Generator ECL ground (connect to analog ground)
VNT	–	Time Base Generator PLL analog circuit ground
VNP	–	Data separator PLL analog circuit ground
VND	–	TTL Buffer I/O digital ground
VNC	–	Internal ECL, CMOS logic digital ground
VNS	–	Sampled data processor ground

ANALOG INPUT PINS

VIA+, VIA-	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins

ANALOG OUTPUT PINS

TPA+, TPA-	O	TEST PINS: Emitter output test points. Various signals are multiplexed to these test points by the Test Point Control Register. The signals include the equalizer control voltage and output, various timing loop control signals and the Viterbi survival register outputs. The test points are provided to show how the signal is being processed. Internal "pull down" resistors to ground are provided. To save power when not in test mode, the control test register bits 3 - 5 must be set to "0".
TPB+, TPB-	O	TEST PINS: Emitter output test points similar to TPA+ and TPA-. The pins are used to look at the other phase of the interleaved signals.
TPC+, TPC-	O	TEST PINS: Bidirectional test points which provide emitter outputs similar to TPA+ and TPA- and provide differential input capability. The pins are used to look at the normal outputs of the continuous time filter or the AGC amplifier output. These pins can also be driven with DP/DN like signals for back end testing.
TPD+, TPD-	O	TEST PINS: Bidirectional test points provide which outputs emitter test points similar to TPA+ and TPA- and provide differential input capability. The pins are used to look at the differentiated outputs of the continuous time filter or the AGC amplifier output. These pins can also be driven with CP/CN like signals for back end testing.

ANALOG OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
TPE	O	TEST PIN: Emitter output test point similar to TPA+. Provides servo FWR out when enabled.
ATO	O	ANALOG TEST OUT: This test point output provides a monitor of one of three signals. They are the equalizer quality signal, the amplitude asymmetry signal, and the DAC outputs. The selected output is determined by the programming of the ATOSEL bits in the Power Down Register. If the DAC outputs are selected, the last DAC written to by the serial control register is the DAC monitored. Signal at ATO is referenced to MAXREF/2.
A, B, C, D	O	SERVO OUTPUTS: These outputs are the amplified and offset versions of the voltages captured on the servo hold capacitors. They are offset by an internally generated 0.27V baseline.
MAXREF	O	SERVO REFERENCE OUTPUT: +3.2V DC reference voltage that represents the maximum output voltage for the A, B, C, and D outputs. Can be used as the reference for an external A/D converter.

ANALOG CONTROL PINS

BYP	–	The data AGC integrating capacitor, C_{BYP}, is connected between BYP and VPA. This pin is used when not in servo read mode (SG = 0).
BYPS	–	The servo AGC integrating capacitor, C_{BYPS}, is connected between BYPS and VPA. This pin is used when in servo read mode (SG = 1).
FLTR1+, FLTR1-	–	TBG PLL LOOP FILTER: Differential connection points for the time base generator PLL loop filter components.
FLTR2+, FLTR2-	–	DS PLL LOOP FILTER: Differential connection points for the data separator PLL loop filter capacitor.
RR	–	CURRENT REFERENCE RESISTOR INPUT: An external 1%, 10 kΩ (for max data rate of 125 Mbit/s) or 12.1 kΩ (for max data rate of 100 Mbit/s) resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and the time base generator DACs.
VRX	–	FILTER REFERENCE RESISTOR INPUT: An external 1%, 12.1 kΩ resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter DACs.
VRC	–	AGC REFERENCE VOLTAGE: VRC is derived by a bandgap reference from VPA.
WRDEL	–	LOWZ ONE-SHOT ADJUST: The resistor connected between this pin and GND determines the length of the lowz period. Tlz = Rlz • 0.1 µs/kΩ.
AGCDEL	–	FAST RECOVERY ONE-SHOT ADJUST: The resistor connected between this pin and GND determines the length of the fast decay period. Tfd = Rfd • 0.1 µs/kΩ.
AGCRST	–	ULTRA FAST DECAY CURRENT ADJUST: The resistor connected between this pin and VPA determines the ultra fast decay current given by the equation I = (VPA - VBYP)/Rufd. This pin may be left open if ultra fast decay action is not required.

PIN DESCRIPTION (continued)

DIGITAL INPUT PINS

NAME	TYPE	DESCRIPTION
LOWZ	I	LOW-Z MODE INPUT: TTL compatible CMOS control pin which, when pulled high, the input impedance is reduced to allow rapid recovery of the input coupling capacitor. When pulled low, keeps the AGC amplifier and filter input impedance high. An open pin is a logic high.
FASTREC	I	FAST RECOVERY: TTL compatible CMOS control pin which, when pulled high, puts the AGC charge pump in the fast decay mode. An open pin is a logic high.
$\overline{\text{PDWN}}$	I	POWER DOWN CONTROL: CMOS compatible power control pin. When set to logic low, the entire chip is in sleep mode with all circuitry, except serial port, shut down. This pin must be set to logic high in normal operating mode. Selected circuitry can be shut down by the Power Down Register. The $\overline{\text{PDWN}}$ pin must be either driven to a valid CMOS high level or externally pulled up since it is not internally pulled up.
$\overline{\text{HOLD}}$	I	AGC HOLD CONTROL INPUT: TTL compatible CMOS control pin which, when pulled low, holds the AGC amplifier gain constant by turning off the AGC charge pump. The AGC loop is active when this pin is either at high or open.
EQHOLD	I	EQUALIZER HOLD CONTROL INPUT: TTL compatible control pin which, when pulled high causes the present adaptive equalizer tap weights to be held until the input is set low. An open pin is at logic high.
FREF	I	REFERENCE FREQUENCY INPUT: Reference frequency for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an ac coupled ECL signal. When bit 3 (BT) of the Control Operating Register is set, FREF replaces the VCO as the input to the data separator.
WCLK	I	WRITE CLOCK: TTL compatible CMOS input that latches in the data at the selected NRZ interface on the rising edge. Must be synchronous with the write data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. An open pin is at logic high.
RG	I	READ GATE: TTL compatible CMOS input that, when pulled high, selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input and enables the read mode/address detect sequences. A low level selects the time base generator output. An open pin is at logic high.
WG/$\overline{\text{WG}}$	I	WRITE GATE: TTL compatible CMOS input that, when pulled high, enables the write mode. The active state of WG/$\overline{\text{WG}}$ can be selected by the WGP bit in the control operating register. An open pin is at logic high.
SG	I	SERVO GATE: TTL compatible CMOS input that, when pulled high, enables the servo read mode. An open pin is at logic high.
VRDT	I	VITERBI READ DATA: A TTL or ac coupled PECL compatible input to the data separator back end, for testing purposes only. This pin is controlled by the VRDT bit in the Control Test Register.

DIGITAL INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{DWR}$	I	DIRECT WRITE MODE 2 ENABLE: Enables DWI, $\overline{DWI}$ inputs to the write data flip-flop when input is low. TTL compatible CMOS levels. Open pin is at logic high.
DWI, $\overline{DWI}$	I	DIRECT WRITE INPUTS: Inputs connect to the toggle input of the write data flip-flop when $\overline{DWR}$ is low. PECL input levels. Can be left open.
STROBE	I	SERVO STROBE INPUT: Active high enable for charging of an individual hold capacitor during a servo burst capture. The falling edge of STROBE will increment an internal counter that determines which of the four hold capacitors will be charged during the next strobe pulse. TTL compatible CMOS levels. Open pin is at logic high.
$\overline{RESET}$	I	RESET CONTROL INPUT: Active low reset for discharging of the four internal servo burst hold capacitors for channels A, B, C, and D. TTL compatible CMOS input levels. Open pin is at logic high.

DIGITAL BIDIRECTIONAL PINS

NRZ0-7	I/O	BYTE WIDE NRZ DATA PORT: TTL compatible CMOS bi-directional input / output. Input to the encoder when WG/$\overline{WG}$ is high. Output from the decoder when RG is high. The 4 LSBs are used in nibble mode. The 4 MSBs can be left open if not used.
NRZP	I/O	NRZ DATA PARITY BIT: Active when in byte-wide mode. TTL compatible CMOS bi-directional input/output. Generates even read parity when RG is high, and accepts even write parity when WG/$\overline{WG}$ is active. Can be left open if not used.

DIGITAL OUTPUT PINS

RCLK	O	READ REFERENCE CLOCK: A multiplexed clock source used by the controller. When RG is low, RCLK is synchronized to the time base generator output, F_{TBG}. When RG goes high, RCLK remains synchronized to F_{TBG} until the SFC is reached. At that time, RCLK is synchronized to the data separator VCO. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. Limited swing CMOS output levels.
$\overline{SBD}$	O	SYNC BYTE DETECT: Transitions low upon detection of sync byte. This transition is synchronous with the sync byte's placement on the NRZ lines. Once it transitions low, $\overline{SBD}$ remains low until RG goes low, at which point it returns high. CMOS output.
WD, $\overline{WD}$	O	WRITE DATA: Write data flip-flop output. The data is automatically re-synchronized (independent of the delay between RCLK and WCLK) to the reference clock F_{TBG}, except in direct write mode 2. Differential PECL output levels.
RDS/$\overline{RDS}$	O	SERVO READ DATA: Read data pulse output for servo read data. Active low limited swing CMOS output. Output active when SG is high, and high when SG is low. The RDS/$\overline{RDS}$ output becomes active high if the Servo Mode Select bit (SMS) in the Data Rate Register is set to 1.

DIGITAL OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
PPOL	O	SERVO READ DATA POLARITY: Read data pulse polarity output for servo read data. Active high limited swing CMOS output. Negative pulse = low, positive pulse = high. Output active when SG is high.
PERR	O	PARITY ERROR DETECT: Transitions high when a parity error is detected at the byte wide NRZ interface. CMOS output.

SERIAL PORT PINS

SCLK	–	SERIAL DATA CLOCK: Positive edge triggered clock input for the serial data. CMOS input levels.
SDATA	–	SERIAL DATA: Input pin for serial data; 8 register select bits first, followed by 8 data bits. The register select bits and data bits are entered LSB first, MSB last. CMOS input levels.
SDEN	–	SERIAL DATA ENABLE: A high level input enables data loading. The data is internally parallel latched when this input goes low. CMOS input levels.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
Positive 5.0V supply voltage (Vp)	-0.5 to 7V
Storage temperature	-65 to 150°C
Solder vapor bath	215°C, 90s, 2 times
Junction operating temperature	+135°C
Output pins	±10 mA
Analog pins	±10 mA
Voltage applied to other pins	-0.3V to Vp+0.3V

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 55°C for 80-lead PTQFP, 100-lead QFP & TQFP, 0°C < T (ambient) < 70°C for 100-lead PTQFP, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
ICC	Outputs and test point pins open Ta = 27°C		185		mA
PWR Power dissipation normal mode	Outputs and test point pins open, Ta = 27°C		925	1500	mW
PWR Data separator off	Power down register = 2d		530	760	mW
PWR Data separator off & TBG off	Power down register = 6d		460	685	mW
PWR Idle through serial port	Power down register = 7d		125	165	mW
Sleep mode	$\overline{\text{PDWN}}$ = low			5	mW

DIGITAL INPUTS

TTL CMOS Compatible Inputs

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Input low voltage	V_{IL}		-0.3		0.8	V
Input high voltage	V_{IH}		2.0		VPD + 0.3	V
Input low current	I_{IL}	V_{IL} = 0.4V	-400			µA
Input high current	I_{IH}	V_{IH} = 2.4V			100	µA

FREF and VRDT Inputs

Input low voltage	V_{IL}		-0.3		0.8	V
Input high voltage	V_{IH}		2.0		VPD + 0.3	V
Input low current	I_{ILF}	V_{IL} = 0.4V	-400			µA
Input high current	I_{IHF}	V_{IH} = 2.4V			500	µA

CMOS Inputs

Input low voltage	V_{ILC}	VPC = 5.0V			1.5	V
Input high voltage	V_{IHC}	VPC = 5.0V	3.5			V

Pseudo ECL Compatible Inputs

Input low voltage	V_{IL}		VPD - 2		V_{IH} - 0.25	V
Input high voltage	V_{IH}		VPD - 1.1		VPD - 0.4	V
Input current			-100		+100	µA

DIGITAL OUTPUTS

CMOS Outputs

Output low voltage	I_{OL} = +2 mA			0.45	V
Output high voltage	I_{OH} = -100 µA	0.7 • VPD			V

Digital Differential Outputs (WD, $\overline{WD}$)

Output low voltage	VOLD	I_{OL} = 2 mA	VPD - 1.9		VOHD - 0.3	V
Output high voltage	VOHD	I_{OH} = 2 mA	VPD - 1.4		VPD - 0.5	V
Output sink current				-3.5		mA
Differential voltage		| V(WD) - V(WD) |	0.6			Vp-pd

ELECTRICAL SPECIFICATIONS (continued)

Test Point Output Levels

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Test point output swing TPA+, TPA- TPB+, TPB-			0.8		Vp-pd
TPC+, TPC- TPD+,TPD- TPE	C_{LOAD} = 5 pF	1		VPA - 1.5	V
ATO Test point	$R_{LOAD} \geq 10\ k\Omega$ Relative to MAXREF/2	-0.6		1.2	V
Source impedance TPA+/ TPA- TPB+/ TPB- TPC+/TPC- TPD+/TPD- TPE, ATO			45		Ω
Output current TPC+/TPC- TPD+/TPD- TPE		-0.8		+3	mA
TPA+/ TPA- TPB+/ TPD-		-3		+1	mA
ATO		-2		+2	mA
Common voltage TPC+/TPC- TPD+/TPD- TPE			2.5		V
TPA+/ TPA- TPB+/ TPB-			VPA- 1.7 -2Vbe		V
ATO			MAXREF/2		V

SERIAL PORT TIMING
Refer to Figure 6

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Data clock period	Tc		80			ns
SCLK low time	Tckl	SCLK < 0.8V	30			ns
SCLK high time	Tckh	SCLK > 2.0V	30			ns
Enable to SCLK	Tsens		40			ns
SCLK to disable	Tsenh		40			ns
Data set-up time	Tds		15			ns
Data hold time	Tdh		15			ns
SDEN min. low time	Tsl		160			ns

ELECTRICAL SPECIFICATIONS (continued)

AGC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

AGC Amplifier

The input signals are AC coupled to VIA+ and VIA-. Integrating capacitor C_{BYP} = 1000 pF, is connected between BYP and VPA. Integrating capacitor C_{BYPS} = 1000 pF, is connected between BYPS and VPA. Unless otherwise specified, the output is measured differentially at TPC+ and TPC-, Fin = 5 MHz, the filter frequency fc = max and the filter boost = 0 dB. All specifications apply equally to servo and read mode prior to SFC.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input range	Filter Boost = 0 dB @ fc 5 MHz ≤ fc ≤ 34 MHz, Fin = fc	20		250	mVp-pd
Input range	Filter Boost = 11 dB @ fc 9 MHz ≤ fc ≤ 34 MHz, Fin = fc	20		200	mVp-pd
ON± voltage measured @ TPC±	VIA = 20 to 250 mVp-pd 1,1,-1,-1,— pattern DP/DN output selected 5 MHz < fc < 34 MHz, Fin = fc boost = 0 to 13 dB	1.19	1.40	1.61	Vp-pd
DP/DN voltage variation	20 mVp-pd < VIA < 250 mVp-pd			5.0	%
Gain range		3		64	V/V
Gain sensitivity	BYP or BYPS voltage change		38		dB/V
Differential input resistance	LOWZ = low, LZTC = low	5.8	7.6	9.4	kΩ
	LOWZ = low, LZTC = high	1.7	2.7	4.0	kΩ
	LOWZ = high, LZTC = x	200	550	1050	Ω
Single-ended input resistance	LOWZ = low, LZTC = low		6.5		kΩ
	LOWZ = high, LZTC = x		500		Ω
	LOWZ = low, LZTC = high		1.9		kΩ
Output offset change	From gain = 3 V/V to 64 V/V with DC cancellation off			200	mV
Input noise voltage	Fixed gain = 24 dB, Rs = 0Ω		15	30	nV/√Hz
CMRR	Fixed gain = 24 dB, Rs = 0Ω	35			dB
PSRR	Fixed gain = 24 dB, Rs = 0Ω	40			dB

AGC CONTROL SECTION

The input signals are DC coupled into TPC± with TPC± selected as inputs

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Decay current normal I_D	FASTREC = low, SG = low DR = Data Rate Register 37 ≤ DR ≤ 127 RR = 12.1 kΩ		-24.5		µA
Servo mode decay current normal	FASTREC = low, SG = high TPC+ = TPC-		-24.5		µA
Fast decay current I_{DFR}	FASTREC = high TPC+ = TPC-		8 • Id		A
Normal attack current I_{CH}	|TPC+ - TPC-| = 0.7875V FASTREC = low		-17 • Id		A
Fast attack current I_{CHF}	|TPC+ - TPC-| ≥ 1.09V FASTREC = low		-143 • Id		A
Fast recovery attack current I_{CHFR}	|TPC+ - TPC-| = 0.7875V FASTREC = high		-64 • Id		A
Sample data AGC peak charge and discharge currents	0 ≤ AGC ≤ 3 AGC = AGC1-0 DR = Data Rate Register 37 ≤ DR ≤127, RR(kΩ)		+/-2.66 • 10^{-6} • AGC • DR/RR		A
BYP pin leakage current	$\overline{HOLD}$ = low, V_{BYP} = VRC	-70		+50	nA
BYPS pin leakage current	$\overline{HOLD}$ = low, V_{BYPS} = VRC	-70		+50	nA
VRC reference voltage	-50 µA ≤ Io ≤ +500 µA	VPA - 2.56		VPA - 2.1	V

PULSE QUALIFIER CHARACTERISTICS

Unless otherwise specified, a 100 mVp-p sine wave at 15 MHz is AC coupled into VIA±. FC = 127, and FB = 0.

Dual Level Qualifier

See above for input conditions unless otherwise specified.

Data level threshold	L_{TH}	Prior to SFC L_{TH} (mV) = 10.47 • LD 16 ≤ LD ≤ 63	L_{TH} -11%	L_{TH}	L_{TH} +11%	V
Data level threshold	L_{TH}	After SFC ALE = 0 L_{TH} (mV) = 7.44 • LD ALE = 1 L_{TH} (%) = 1.574 • LD 16 ≤ LS ≤ 63	L_{TH} -11%	L_{TH}	L_{TH} +11%	V
Servo level threshold	LS_{TH}	LS_{TH} (mV) = 10.47 • LS 16 ≤ LS ≤ 63	LS_{TH} -11%	LS_{TH}	LS_{TH} +11%	V

Dual Level Qualifier (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
RDS/$\overline{\text{RDS}}$ pulse width high	RDSPW = 0	7.7	15	20	ns
voltage	RDSPW = 1	16.8	27	35	ns
PPOL to RDS/$\overline{\text{RDS}}$ delay time	PPOL Edge to RDS/$\overline{\text{RDS}}$ rise/fall, measured at 1.5V crossing	2.5		12	ns
PPOL, RDS/$\overline{\text{RDS}}$ Rise time	15 pF load, 0.8 to 2.4V			8	ns
PPOL, RDS/$\overline{\text{RDS}}$ Fall time	15 pF load, 2.4 to 0.8V			6	ns
Pulse pairing	Window and hysteresis LSth = 50%. Measured at the rising/falling edge of RDS/$\overline{\text{RDS}}$ Fin = 5 MHz, FCS = 30	-2.5		+2.5	ns

Viterbi Qualifier
See General for input conditions unless otherwise specified.

Viterbi threshold	V_{TH}	V_{TH} (mV) = 7.874 • VD 45 ≤ VD ≤ 127	V_{TH} - 10%	V_{TH}	V_{TH} +10%	V

Equalization Quality Factor
Unless otherwise specified, measured at ATO pin loaded with 5 pF. VIA± input signal has no asymmetry. Measured after training sequences. Continuous training pattern with zeros displaced by ±10% of ones magnitude of 500 mV.

Reference voltage	No pulse asymmetry ATOSEL1-0 = 00	Typ. -130 mV	Maxref/2	Typ. +130 mV	V
Q	Absolute deviation of zeros is multiplied by gain		600		mV
Drift			0.2		mV/µs

Amplitude Asymmetry Quality Factor
Unless otherwise specified, measured at ATO pin loaded with 5 pF. VIA± input signal has 10% amplitude asymmetry. Asymmetry (%) = $((V_{+1}-V_{-1})/(V_{+1}+V_{-1})) \cdot 100$, where V_{+1} = positive "1" sample value and V_{-1} = negative "1" sample value. This is measured with continuous training bytes, 93H, with distance between cancelled zeros and non-cancelled zeros at ±10% of one's magnitude of 500 mV or 100 mV.

Reference voltage	ATOSEL1-0 = 00	Typ. - 100 mV	Maxref/2	Typ. + 100 mV	V
Qasym at ATO			400		mV

ATO Buffer Characteristics
Unless otherwise specified, measured at ATO pin loaded with 5 pF. VIA± input signal has no asymmetry.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Reference voltage	ATOSEL1-0 = 00	Typ. - 100 mV	Maxref/2	Typ. + 100 mV	V
Swing	From reference voltage	±0.6			V
Source impedance			50		Ω
Drive capability	± refers to source/sink	+2/-2	+5/-3		mA

Internal AC Coupler Characteristics
Measured at TPC+/TPC- and TPD+/TPD- pins.

Offset Voltage	ACCPL = 0	-35		+35	mV
LOWZ Time Constant	LOWZ = 1, LZTC = X		0.3		µs
Non LOWZ Time Constant	LOWZ = 0, LZTC = 0		5		µs
	LOWZ = 0, LZTC = 1		1.5		µs

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ELECTRICAL SPECIFICATIONS (continued)

PROGRAMMABLE FILTER CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply. The input signals are AC coupled to VIA+ and VIA-. All specifications identical for identical data and servo register settings. Data uses C_{BYP} from BYP to VPA and servo uses C_{BYPS} from BYPS to VPA.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Filter cutoff range fcr	fc (MHz) = 0.301 • FC - 1.142 44 ≤ FC ≤ 117 fc (MHz) = 0.277 • FCS + 0.08 14 ≤ FCS ≤ 43 0 dB Boost		4-34		MHz
Filter Fc accuracy fca	44 ≤ FC ≤ 117	-15		+15	%
	14 ≤ FCS ≤ 43	-20		+20	%
OD gain to ON gain mismatch	Fin = 0.67 • fc 0 dB Boost mismatch = $\frac{\text{OD gain-ON gain}}{\text{ON gain}} \cdot 100\%$	-20		+20	%
Boost @ Fc	Boost (dB) = 20 • log [(0.021848 • FB) + 0.000046 • FC • FB + 1]		FB		dB
Boost accuracy	Boost = 13dB	-2.0		+2.0	dB
	Boost = 9 dB	-1.7		+1.7	dB
Filter output dynamic range ON±	THD = 2.5%, Fin = 0.67 • fc, CL = 15 pF	1.4			Vp-p
TGD Variation	fc = 34 MHz F = 0.3 fc to fc FB = 0	-500		+500	ps
	fc = 34 MHz F = 0.3 fc to f FB = 127	-700		+700	ps
	fc = 12 MHz to 34 MHz F = 0.3 fc to fc 0 ≤ FB ≤ 127	-3		+3	%
	fc = 4 MHz to 12 MHz F = 0.3 fc to fc 0 ≤ FB ≤ 127	-4		+4	%
	fc = 12 MHz to 34 MHz F = fc to 1.75 fc 0 ≤ FB ≤ 127	-3		+3	%
	fc = 4 MHz to 12 MHz F = fc to 1.75 fc 0 ≤ FB ≤ 127	-6		+6	%
ON+ - ON- output noise voltage, no boost	BW = 100 MHz, Rs = 50Ω fc = 34 MHz, boost = 0 dB AGC gain = 24 dB fixed		3.4		mV rms

PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
ON+ - ON- output noise voltage, max. boost	BW = 100 MHz, Rs = 50Ω fc = 34 MHz; FB = 127 AGC gain = 24 dB fixed		6.8		mV rms
Rx pin voltage VRX	Ta = 27°C		600		mV
	Ta = 127°C		800		mV
Rx resistance	1% fixed value		12.1		kΩ

TRANSVERSAL FILTER CHARACTERISTICS

Km1 Range		±0.15	±0.2		V/V
Km1 Gain drift	EQHOLD = 1, hold time ≤ 1 ms		0.015	0.05	V/V/ms
Km2 Range			+0.13125 -0.15		
Km2 Resolution			0.01875		
Km2 Accuracy			±20		%

Note: Km1 and the equalizer control voltage at TPA+ -TPA- is approximately related by
Km1 = 0.009 • Data Rate (Mbit/s) • (TPA + -TPA-)

TIME BASE GENERATOR CHARACTERISTICS
RR = 10.0 kΩ to gnd for 125 Mbit/s max. operation, and 12.1 kΩ for 100 Mbit/s max. operation

FREF input range	Control Operating Register BT bit = 0	6		25	MHz
	Control Operating Register BT bit = 1 and Control Test Register, EFR bit =1			141	MHz
FREF input pulse width	Control Operating Register BT bit = 0	10			ns
	Control Operating Register BT bit = 1 and Control Test Register, EFR bit =1	2			ns
FTBG frequency range		47		141	MHz
FTBG jitter	> 10K samples		30	200	ps_{RMS}
M counter range		2		255	
N counter range		2		127	
VCO center frequency FTBG	FLTR1+ - FLTR1- = 0V FTBG = [(1.143 • DR) + 4.986] MHz RR = 10.0 kΩ FTBG = [(0.948 • DR) + 1.831] MHz RR = 12.1 kΩ	0.80 • FTBG		1.20 • FTBG	MHz

TIME BASE GENERATOR CHARACTERISTICS (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VCO dynamic range		-2.0V ≤ FLTR1+ - FLTR1- ≤ +2.0V F_{TBG} = 94 MHz	±25			%
VCO control gain	KVCO	ωi = 2π • FTBG -2.0V ≤ FLTR1+ - FLTR1- ≤ 2.0V	0.12 • ωi	0.18 • ωi	0.24 • ωi	rad/(V-S)
Phase detector gain	KD	KD = (2.125 • DR) + 3.171 RR = 10 kΩ	0.72 • KD		1.22 • KD	µA/rad
		KD = 1.777 • DR + 3.335 RR = 12.1 kΩ	0.72 • KD		1.22 • KD	µA/rad
KVCO • KD product accuracy			-28		+28	%

DATA SEPARATOR CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

Read Mode - Byte Wide

Read clock rise time	T_{RRC}	0.8V to 2.4V CL ≤ 15 pF			10	ns
Read clock fall time	T_{FRC}	2.4V to 0.8V CL ≤ 15 pF			10	ns
RCLK pulse width	T_{RD}	Except during re-sync	4/9TORC -5		4/9TORC +5	ns
RCLK resync period at SFC and RG falling edge	T_{DC1}	Measured from rising edge to rising edge of RCLK	TORC		TORC+ 2TC	ns
RCLK re-sync period at code boundary detect	Tdc2	Measured from rising edge to rising edge of RCLK	TORC		2(TORC)	ns
NRZx out set-up and hold time	T_{NS}, T_{NH}		20			ns
$\overline{SBD}$ set-up time	T_{SBS}		20			ns

Write Mode - Byte Wide

Write clock rise time	T_{RWC}	0.8 to 2.0V CL ≤ 15 pF			10	ns
Write clock fall time	T_{FWC}	2.0 to 0.8V CL ≤ 15 pF			8	ns
NRZx set-up time	T_{SNRZ}		10			ns
NRZx hold time	T_{HNRZ}		3			ns
PERR propagation delay	T_{PERR}	Measured from the rising edge of WCLK to the transition of PERR			41	ns

DATA SEPARATOR CHARACTERISTICS (continued)

Write Data Output

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Write data output position accuracy	T_{WD}	Write precomp = 0, C_L < 15pF, T_{TBG} = 1/F_{TBG}	T_{TBG} - 0.5		T_{TBG} + 0.5	ns
Write data output rise time	T_{RWD}	20% to 80% points			4	ns
Write data output fall time	T_{RWD}	80% to 20% points			4	ns

Read Mode - Nibble

RCLK low time	R_{CL}	$C_L \leq 15$ pF	5			ns
RCLK high time	R_{CH}	$C_L \leq 15$ pF	5			ns
Read clock rise time	T_{RRC}	0.8V to 2.4V $C_L \leq 15$ pF			8	ns
Read clock fall time	T_{FRC}	2.4V to 0.8V $C_L \leq 15$ pF			6	ns
NRZx out set-up and hold time	T_{NS}, T_{NH}		5.6			ns
$\overline{SBD}$ set-up time	TDSL		7.5			ns

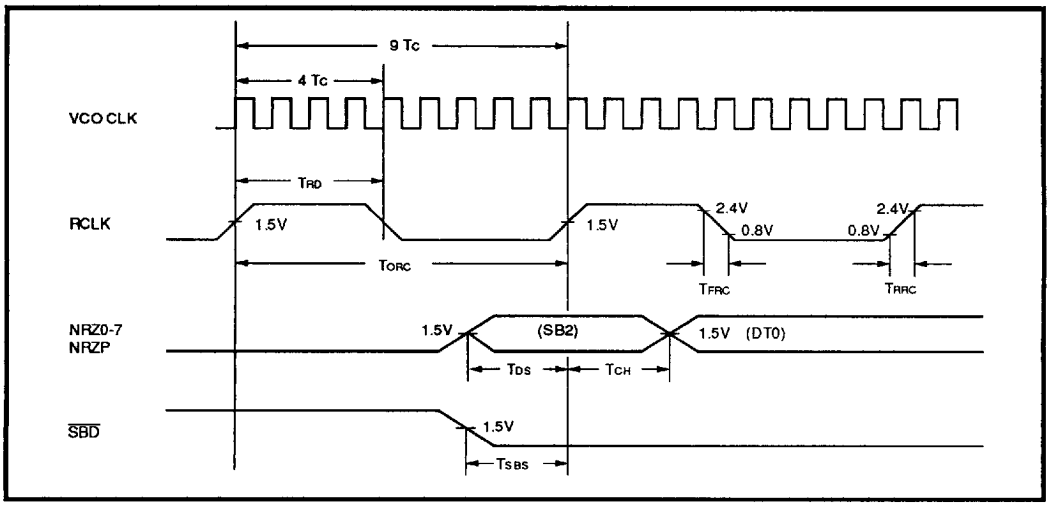


FIGURE 22: Byte Wide Read Timing

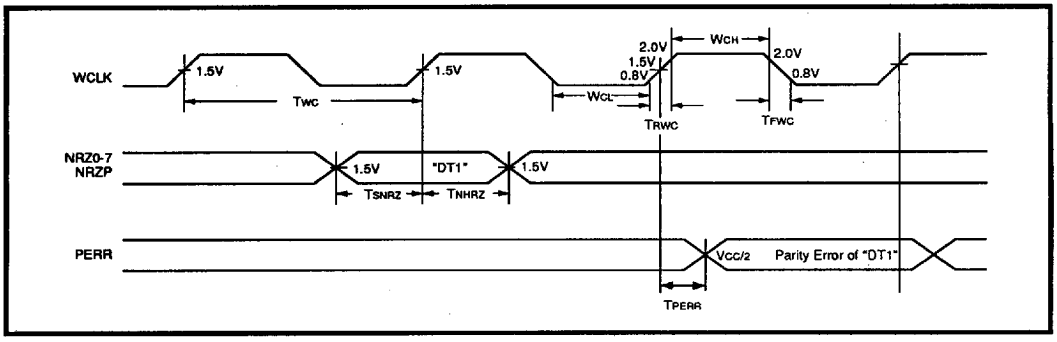


FIGURE 23: Write Mode NRZ Interface Timing (byte wide and nibble modes)

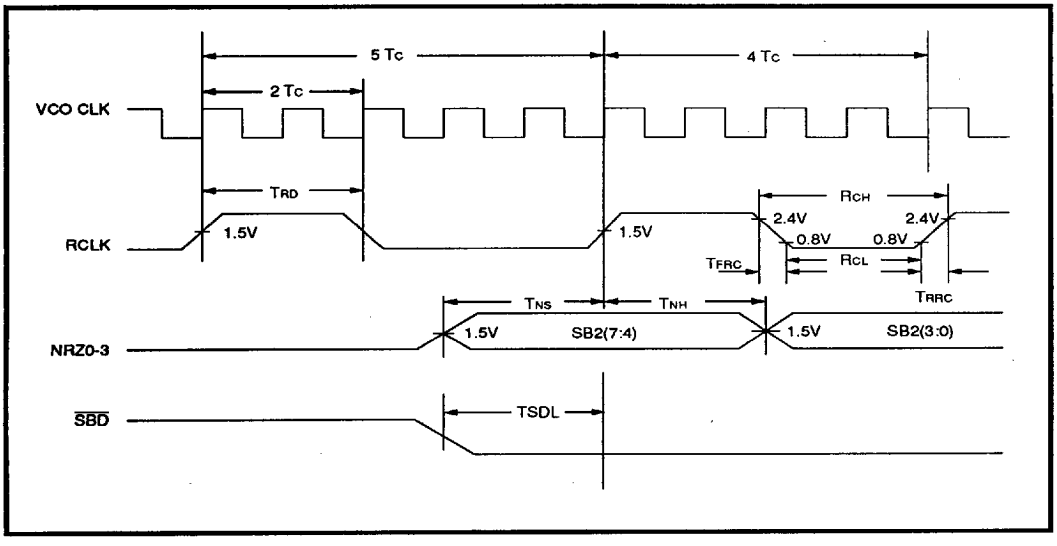


FIGURE 24: Nibble Read Timing

DATA SEPARATOR CHARACTERISTICS (continued)

Write Mode - Nibble

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
WCLK period	T_{WC}	$C_L \leq 15$ pF	24			ns
WCLK low time	WC_L	$C_L \leq 15$ pF	5			ns
WCLK high time	WC_H	$C_L \leq 15$ pF	5			ns
Write clock rise time	T_{RWC}	0.8 to 2.0V $C_L \leq 15$ pF			10	ns
Write clock fall time	T_{FWC}	2.0 to 0.8V $C_L \leq 15$ pF			8	ns
NRZx set-up time	T_{SNRZ}		8			ns
NRZx hold time	T_{HNRZ}		3			ns

Write Precompensation

Write precomp time shift as a percentage of T_{TBG}	TPC	TPC = 2.1 • WPC $0 \leq$ WPC ≤ 15	0.8 • TPC		1.2 • TPC	%

Data Synchronizer PLL

VCO center frequency	FVCO	FLTR2+ - FLTR2- = 0V FVCO = [(1.143 • DR) + 4.986] MHz RR = 10.0 kΩ FVCO = [(0.948 • DR) + 1.831] MHz RR = 12.1 kΩ	0.8 • FVCO		1.2 • FVCO	ns
VCO dynamic range in each direction		-2.0V $\leq$ FLTR2+ - FLTR2- $\leq$ +2.0V	±25			%
VCO control gain & M, M • KVCO		$\omega i = 2\pi$ • FVCO M = 4.32 • (DR/127) RR = 10.0 kΩ M = 3.60 • (DR/127) RR = 12.1 kΩ -0.25V $\leq$ FLTR2+ - FLTR2- $\leq$ +0.25V	0.11 • ωi • M		0.29 • ωi • M	rad/(V-S)
Charge Pump Transconductance		Gm = 350 µA/V during synchronization	0.6 • Gm		1.4 • Gm	A/V
Idle Mode Phase Detector Gain	KDI	KDI = 0.15 • Gm • M RR = 10.0 kΩ KDI = 0.18 • Gm • M RR = 12.1 kΩ		KDI		µA/rad
Gm • M • KVCO product accuracy			-28		+28	%
A • KVCO Product accuracy		A = 0.8 • (DRC/127)	-30		+30	%

ELECTRICAL SPECIFICATIONS (continued)

SERVO CHARACTERISTICS

Unless otherwise specified input is 15 MHz sine wave into DP/DN inputs, TPC/D1-0 = "01". SMS = "0". STROBE and RESET durations are 1.0 µs and SBCC = "10".

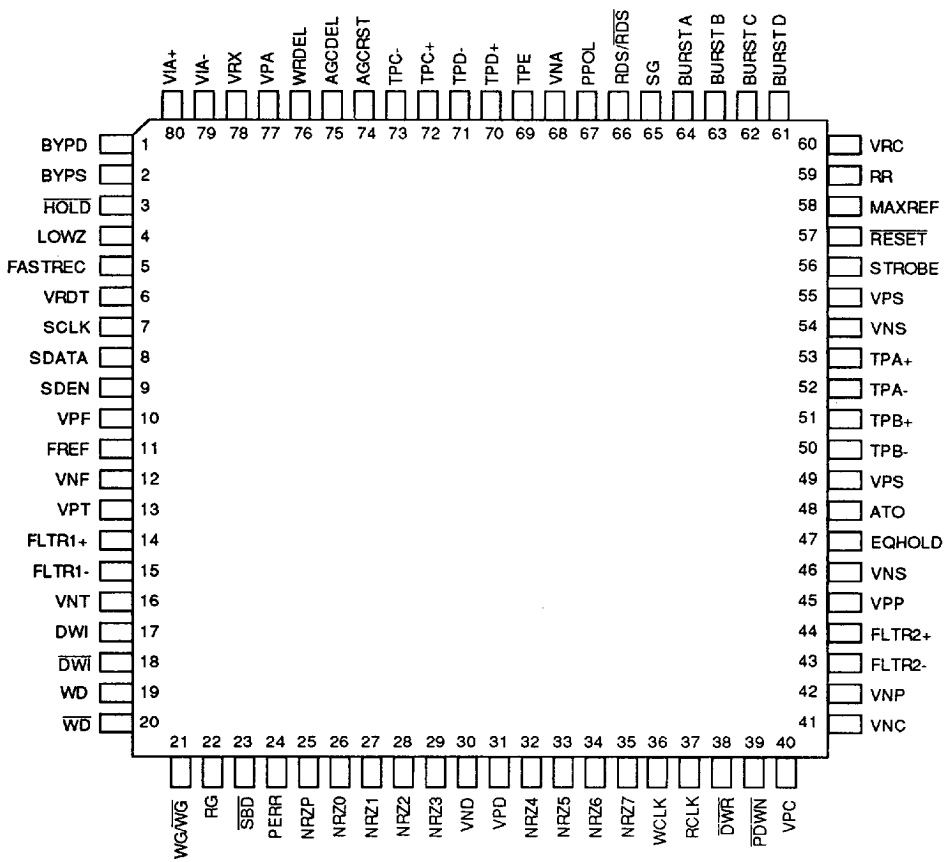
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MAXREF output voltage	I_{SOURCE} = 0 mA	3.06	3.22	3.42	V
MAXREF load regulation	$I_{SOURCE} \leq$ 1.5 mA			40	mV
A, B, C, D output resistance	I_{SOURCE}/I_{SINK} = 0.1 mA			50	Ω
A, B, C, D output low voltage	I_{SINK} = 0.1 mA $\overline{RESET}$ = low	170	270	370	mV
A, B, C, D output swing	DP/DN = 1.4 Vp-p	2.56	2.8	3.01	V
A, B, C, D gain	0.3V ≤ DP - DN ≤ 1.4V	1.85	2.0	2.15	V/Vp-pd
	0V ≤ DP - DN ≤ 0.3V	0		2.15	V/Vp-pd
Hold droop	$\overline{STROBE}$ = low $\overline{RESET}$ = high			0.5	mV/µs
Channel to channel mismatch	DP - DN = 1.4 Vp-p			120	mV
Burst acquisition time to 95% from reset time	DP - DN = 1.4 Vp-p			0.5	µs
Burst reset to 5%	DP - DN = 1.40 Vp-p $\overline{RESET}$ = low			0.5	µs
Reset to strobe delay	From rising $\overline{RESET}$ to rising STROBE	20			ns
Minimum time between STROBE pulses		20			ns

MODE CONTROL

WG/$\overline{WG}$	RG	DEVICE MODE	DESCRIPTION
0/1	0	Idle mode	DS VCO locked to FTBG. NRZ7-0 tri-stated.
0/1	1	Data read mode	DS PLL acquisition, adaptive equalizer training, code word boundary search and detect, decode, sync byte detect, and NRZ data output. DS VCO switched from FTBG to RD after preamble detect. RCLK gen. input switched from FTBG to DS VCO. RCLK re-synchronized to RD at code word boundary detect. NRZ7-0 active.
1/0	0	Data write mode	Write mode preamble insertion and data write. DS VCO locked to FTBG. RCLK synchronized to FTBG. WD and $\overline{WD}$ active. NRZ7-0 = inputs.
1/0	1	Read override	RG overrides WG/$\overline{WG}$ which causes any write in progress to cease and data read mode to be entered.

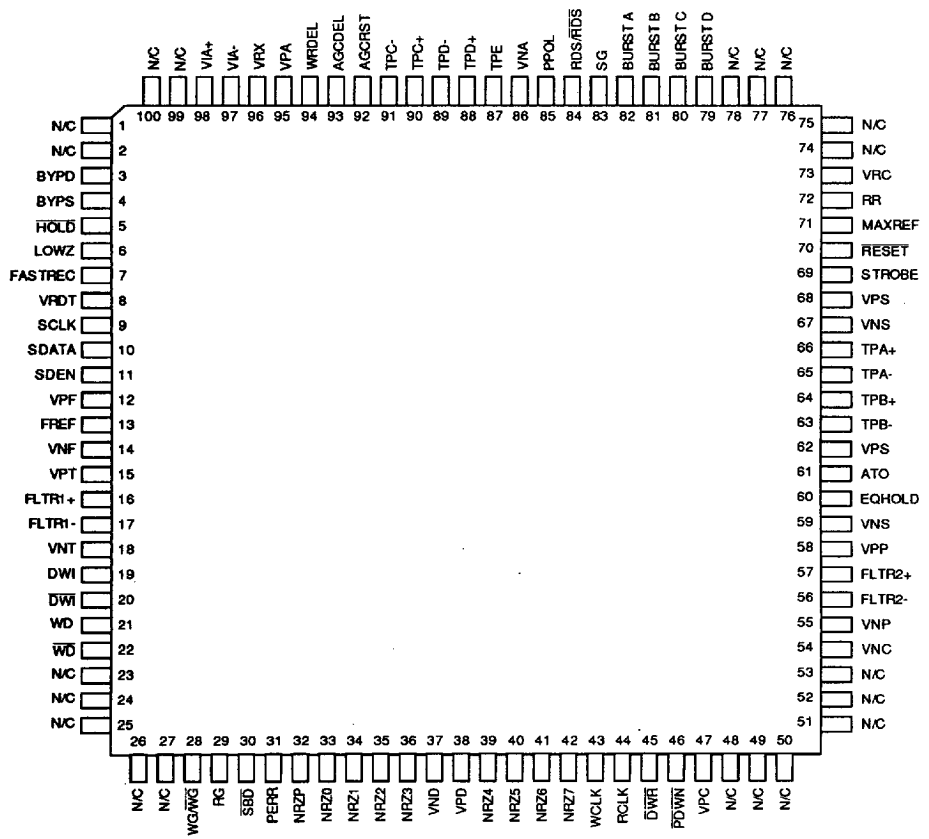
PACKAGE PIN DESIGNATIONS

(Top View)



80-Lead PTQFP

PACKAGE PIN DESIGNATIONS
(Top View)

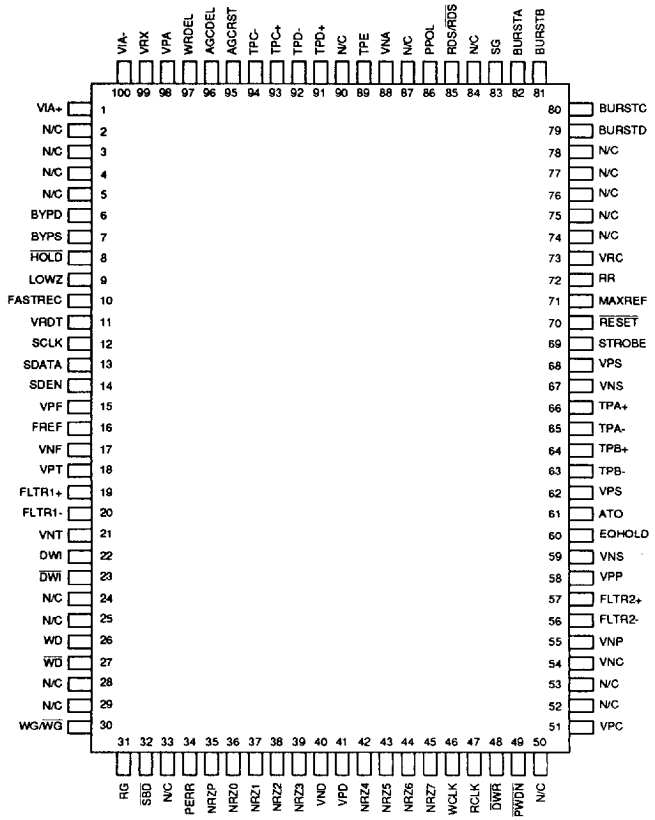


100-Lead TQFP, PTQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-Lead QFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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