Preliminary COM'L

PALCE630H-15/25

EE CMOS High Performance Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **AMD's Programmable Array Logic (PAL®) architecture**
- **Electrically-erasable CMOS technology providing half power (90 mA I_{CC}) at high speed**
  -15 = 15 ns t_{PD}
  -25 = 25 ns t_{PD}
- **Sixteen macrocells with configurable I/O architecture**
- **Registered or combinatorial operation**
- **Registers programmable as D, T, J-K, or S-R**
- **Asynchronous clocking via product term or bank register clocking from external pins**
- **Register preload for testability**
- **Power-up reset for initialization**
- **Space-saving 24-pin SKINNYDIP® and 28-pin PLCC packages**
- **Fully tested for 100% programming yield and high reliability**
- **Easy design with PALASM® software**

GENERAL DESCRIPTION

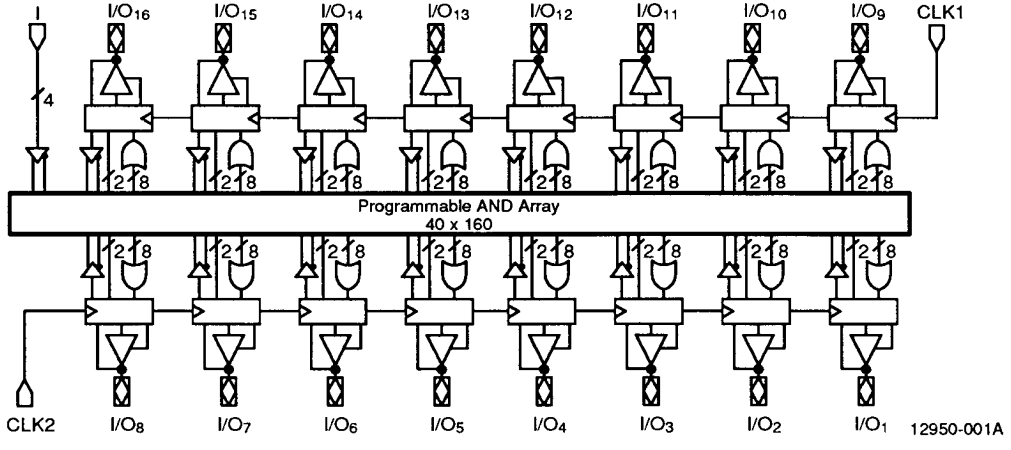
The PALCE630 is a general purpose PAL device and is functionally and fuse map equivalent to the EP610. It can accommodate logic functions with up to 20 inputs and 16 outputs. There are 16 I/O macrocells that can be individually configured to the user's specifications. The macrocells can be configured as either registered or combinatorial. The registers can be configured as D, T, J-K, or S-R flip-flops.

The PALCE630 uses the familiar sum-of-products logic with programmable-AND and fixed-OR structure. Eight product terms are brought to each macrocell to provide logic implementations.

The PALCE630 is manufactured using advanced CMOS EE technology providing high density and low power consumption. Moreover, it is a high-speed device having a worst-case t_{PD} of 15 ns. Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages are offered.

This device can be erased and reprogrammed at least 100 times. Data retention is guaranteed for 20 years. Once a device is programmed the security bit can be used to provide protection from copying a proprietary design.

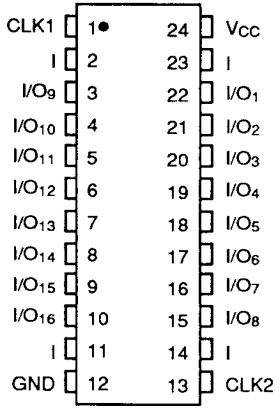
BLOCK DIAGRAM



Publication # 12950 Rev. B Amendment /0
Issue Date: March 1990

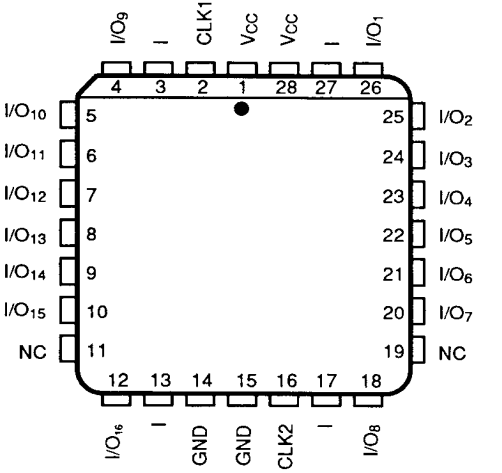
CONNECTION DIAGRAMS
Top View

SKINNYDIP



12950-002A

PLCC



12950-003A

Note:
Pin 1 is marked for orientation

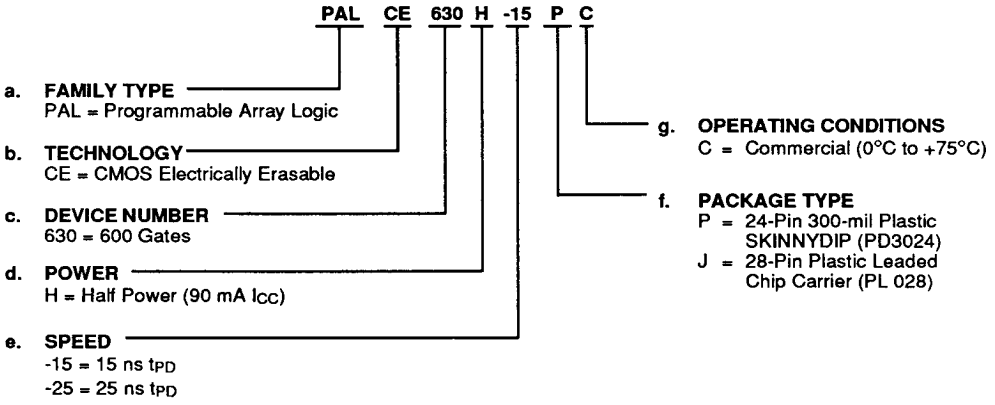
PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Device Number
d. Power
e. Speed
f. Package Type
g. Operating Conditions



Valid Combinations	
PALCE630H-15	PC, JC
PALCE630H-25	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

The PALCE630 is a general purpose programmable logic device. It has 16 independently-configurable macrocells. Each macrocell can be configured as either combinatorial or registered. The registers can be D, T, J-K, or S-R type flip-flops. The device has 4 dedicated input pins and 2 clock pins. Each clock pin controls 8 of the 16 macrocells.

The programming matrix implements a programmable AND logic array which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input polarity. Unused input pins should be tied to V_{CC} or ground.

The array uses AMD's electrically erasable technology. An unprogrammed bit is disconnected and a programmed bit is connected. Product terms with all bits unprogrammed assume the logical-HIGH state and product terms with both the TRUE and Complement bits programmed assume the logical-LOW state.

The programmable functions in the PALCE630 are automatically configured from the user's design specifications, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to the programmer, configures the design according to the user's desired function.

Macrocell Configurations

The PALCE630 macrocell can be configured as either combinatorial or registered I/O. Both the combinatorial and registered configurations have output polarity control. The register can be configured as a D, T, J-K, or S-R type flip-flop. Figure 1 shows the possible configurations.

Each macrocell can select as its clock either the corresponding clock pin or the CLK/OE product term. If the clock pin is selected, the output enable is controlled by the CLK/OE product term. If the CLK/OE product term is selected, the output is always enabled.

Combinatorial I/O

All 8 product terms are available to the OR gate. The output-enable function is performed by the CLK/OE product term.

Registered Configurations

There are 4 flip-flop types available: D, T, J-K and S-R.

The registers can be configured as synchronous or asynchronous. In the synchronous configuration, the clock is controlled by the clock input pin. The output enable is controlled by the product term function. In the asynchronous configuration, the clock input is controlled by the product term. The output is always enabled.

D Flip-Flop

All 8 product terms are available to the OR gate. The D input polarity is controlled by an exclusive-OR gate. For the D flip-flop, the output level is the D-input level at the rising edge of the clock.

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

T Flip-Flop

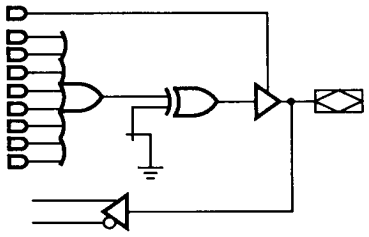
All 8 inputs are available to the OR gate. The T-input polarity is controlled by an exclusive-OR gate. For the T register, the output level toggles when the T input is HIGH and remains the same when the T input is LOW.

T	Q^n	Q^{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

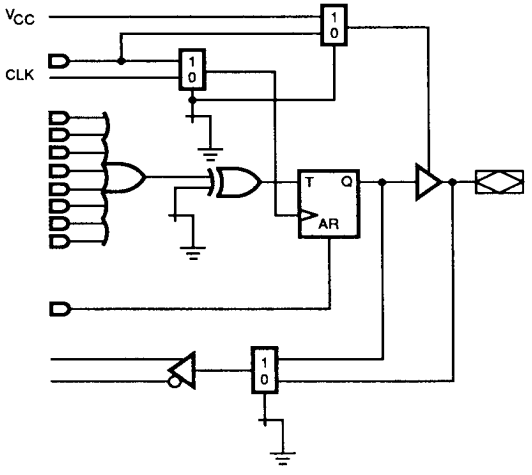
J-K Flip-Flop

The 8 product terms are divided between the J and K inputs. N product terms go to the J input and 8-N product terms go to the K input, where N can range from 0 to 8. Both the J and K inputs to the flip-flop have polarity control via exclusive-OR gates. The J-K flip-flop rules are shown below.

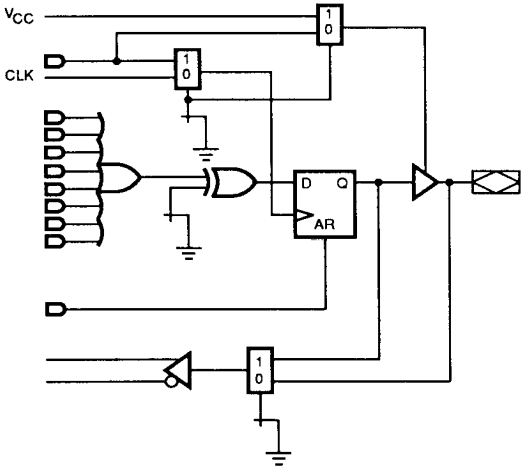
J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



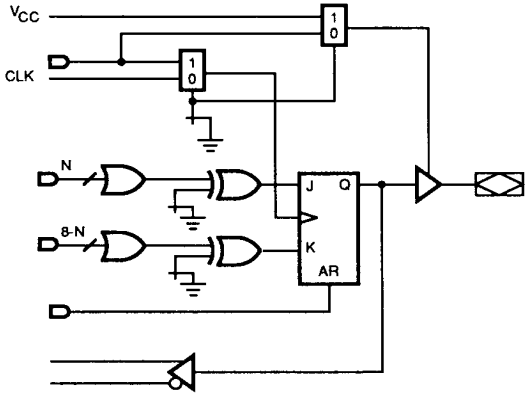
Combinatorial



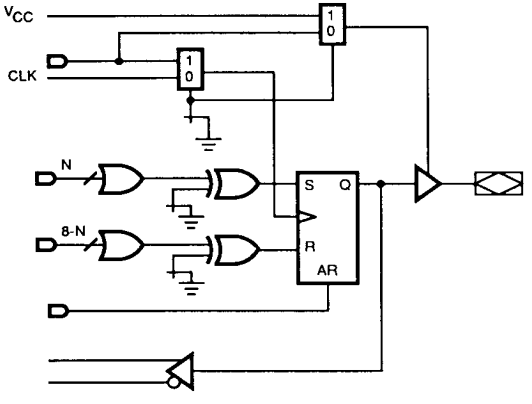
T Register



D Register



J-K Register



S-R Register

12950-004A

Figure 1. Macrocell Configurations

S-R Flip-Flop

The 8 product terms are divided between the S and R inputs. N product terms go to the S input and 8-N product terms go to the R input, where N can range from 0 to 8. Both the S and R inputs to the flip-flop have polarity control via exclusive-OR gates. The S-R flip-flop rules are shown below.

S	R	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Not Allowed	

Asynchronous Reset

All flip-flops have an asynchronous-reset product-term input. When the product term is true, the flip-flop will reset to a logic LOW, regardless of the clock and data inputs.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE630 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW. If combinatorial is selected, the output will be a function of the logic. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE630 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE630 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, preload is disabled and the array is unreadable.

Technology

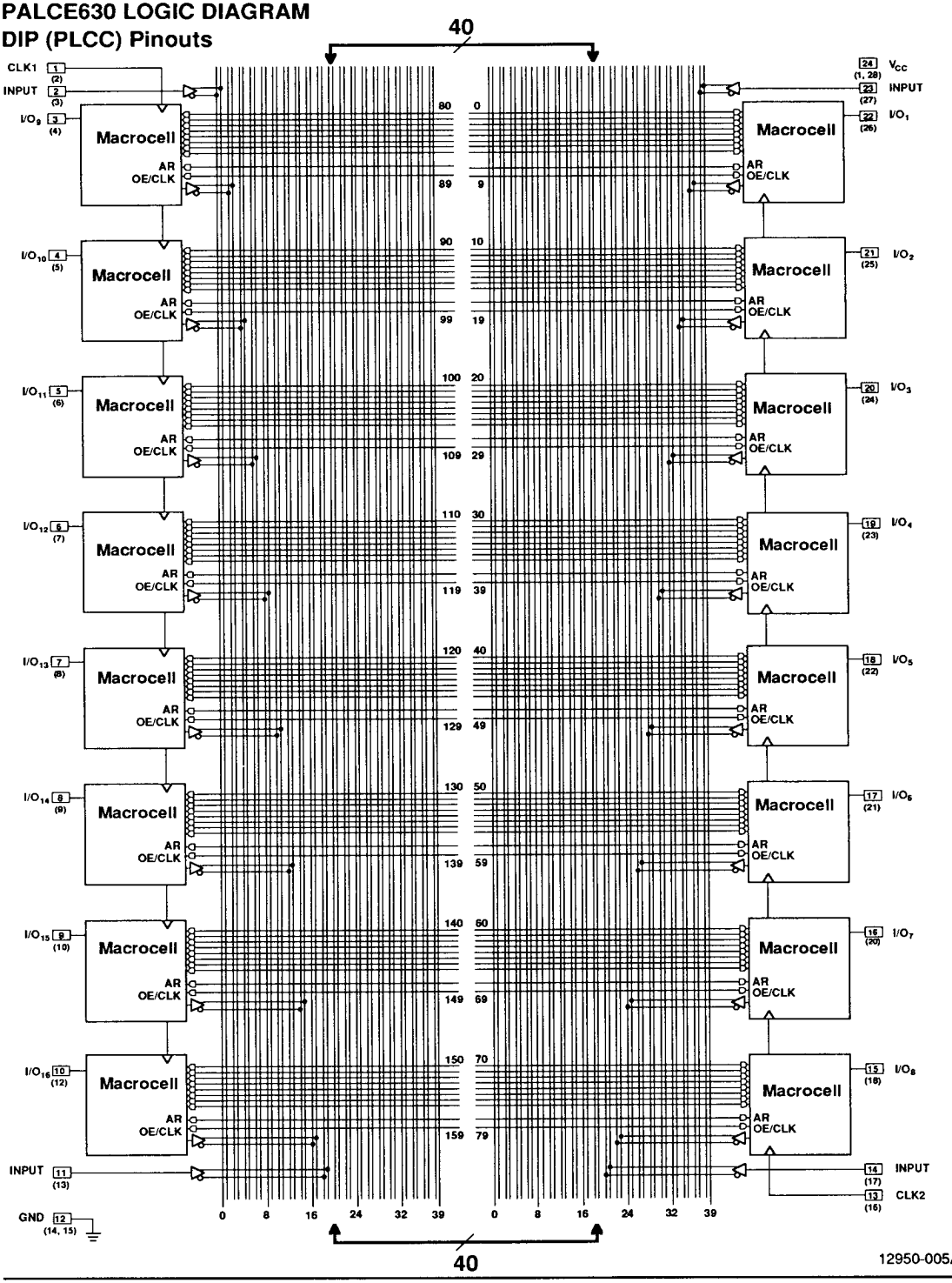
The PALCE630 is manufactured using AMD's advanced Electrically Erasable CMOS process. This technology uses an E^2 cell to replace the fuse link in bipolar parts, and allows AMD to offer lower-power parts of high complexity. In addition, since the E^2 cells can be erased and reprogrammed, these devices can be 100% factory tested before being shipped to the customer.

Programming and Erasing

The PALCE630 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PALCE630 may be erased to reset a previously configured device back to its virgin state. Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

PALCE630 LOGIC DIAGRAM
DIP (PLCC) Pinouts



12950-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
		V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min., I_{OH} = –2.0 mA	3.84		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–150	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

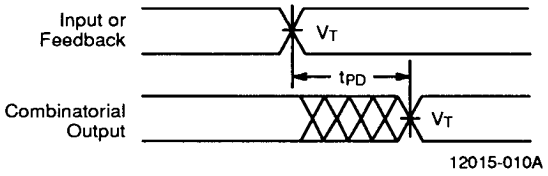
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				8		12	ns
t_{CF}	Clock to Feedback (Note 3)				6		10	ns
t_{WL}	Clock Width	LOW		6		10		ns
t_{WH}		HIGH		6		10		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	50		37		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	55		40		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83		50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns
t_{SA}	Setup Time from Input or Feedback to Clock (Note 5)			5		8		ns
t_{HA}	Hold Time (Note 5)			5		12		ns
t_{COA}	Clock to Output (Note 5)				15		27	ns
t_{CFA}	Clock to Feedback (Notes 3 and 5)				14		26	ns
t_{WLA}	Clock Width	LOW (Note 5)		8		10		ns
t_{WHA}		HIGH (Note 5)		8		10		ns
f_{MAXA}	Maximum Frequency (Notes 4 and 5)	External Feedback	$1/(t_{SA} + t_{COA})$	50		28.6		MHz
		Internal Feedback	$1/(t_{SA} + t_{CFA})$	53		29		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	63		41.6		MHz

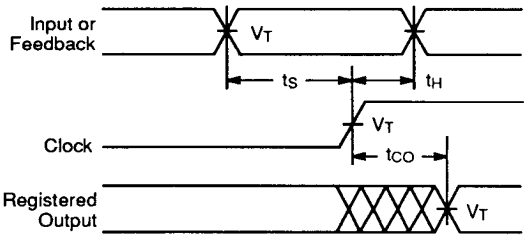
Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. These parameters are measured using the asynchronous product-term clock.

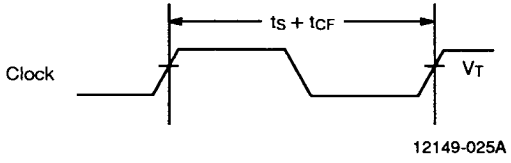
SWITCHING WAVEFORMS



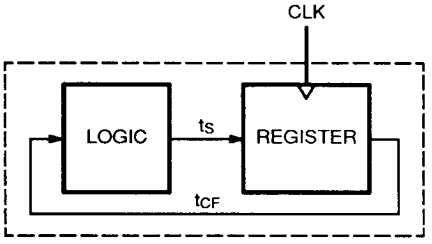
Combinatorial Output

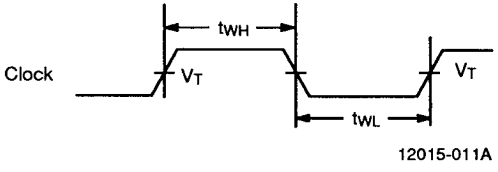


Registered Output

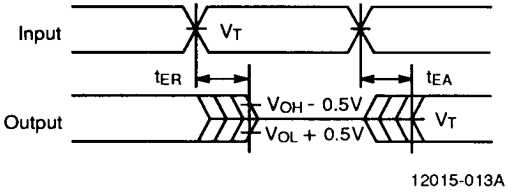


Clock to Feedback (f_{MAX} Internal)
See Path at Right





Clock Width

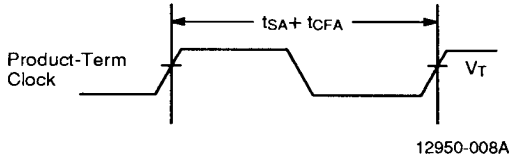


Input to Output Disable/Enable

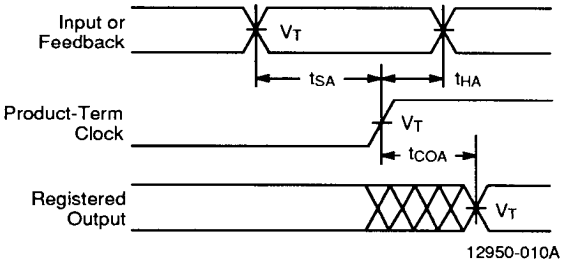
Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

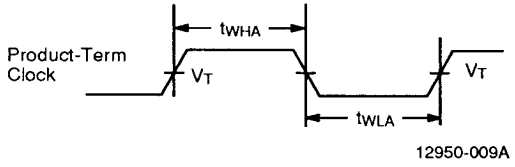
SWITCHING WAVEFORMS (Continued)



Clock to Feedback Using Product-Term Clock



Registered Output Using Product-Term Clock

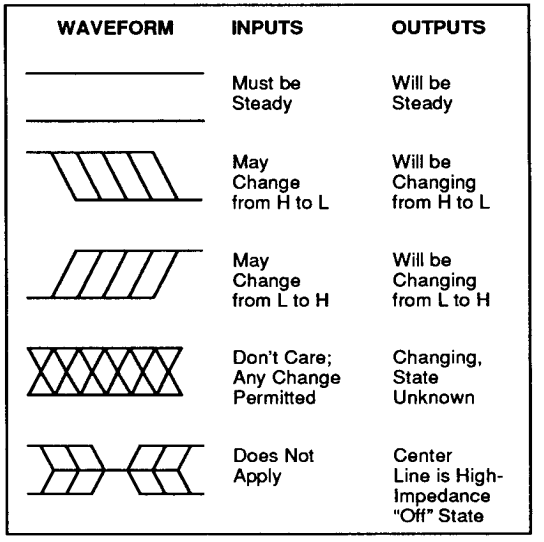


Clock Width Using Product-Term Clock

Notes:

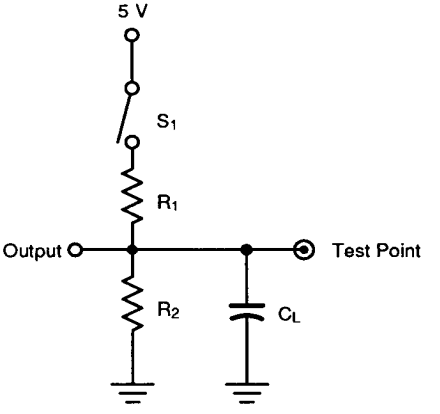
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



12950-012A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	35 pF	340 Ω	855 Ω	1.5 V
t_{EA}	Z → H : Open Z → L : Closed	35 pF	340 Ω	855 Ω	1.5 V
t_{ER}	H → Z : Open L → Z : Closed	5 pF	340 Ω	855 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

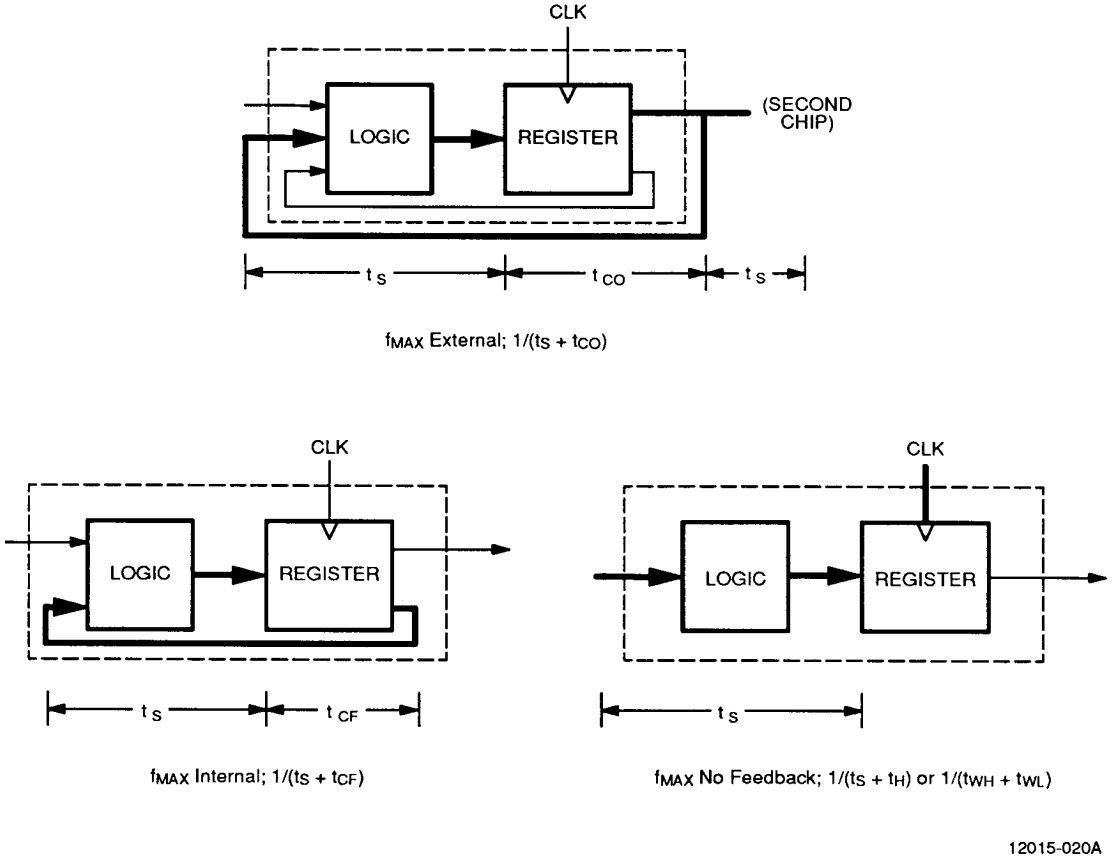
f_{MAX} Parameters

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs ($t_S + t_{CF}$). This f_{MAX} is designated "f_{MAX} internal".

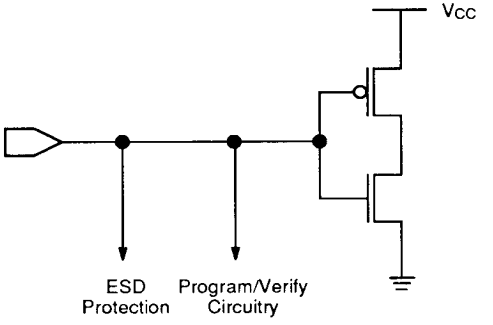
The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period designates the period for the third f_{MAX}, designated "f_{MAX} no feedback".



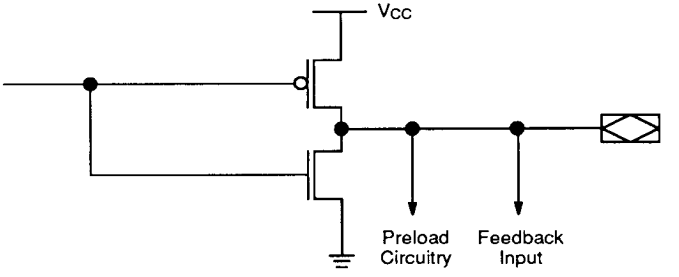
ENDURANCE

Symbol	Parameter Description	Test Conditions	Min.	Unit
t_{DR}	Pattern Data Retention Time	Max. Storage Temperature	10	Years
		Max. Operating Temperature	20	Years
N	Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



Output

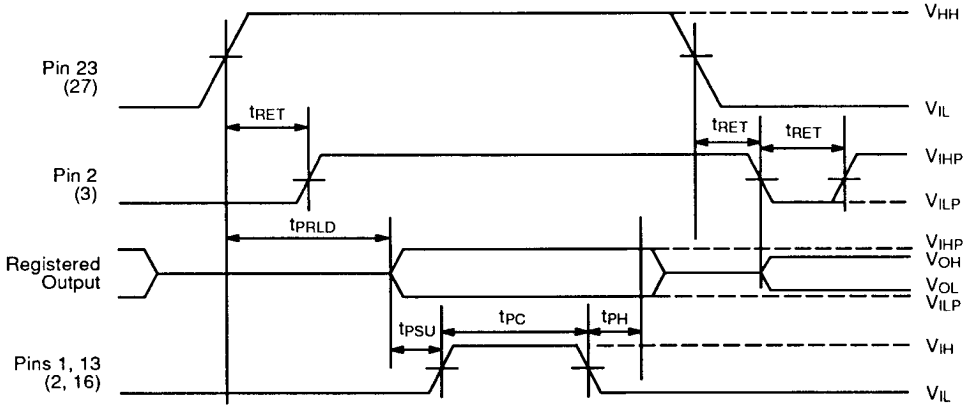
12950-011A

OUTPUT REGISTER PRELOAD

The preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows. PLCC pin numbers are indicated in parentheses.

1. Set pin 23 (27) to V_{HH}.
2. Set pin 2 (3) to V_{IHP}.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Connect combinatorial output pins to ground.
4. Clock pins 1 and 13 (2 and 16).
5. Remove V_{ILP}/V_{IHP} from all registered outputs.
6. Lower pin 23 (27) to V_{IL}/V_{IH}.
7. Verify V_{OL}/V_{OH} at all registered output pins.
8. Toggle pin 2 (3).
9. Enable per programmed pattern.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-Level Input Voltage	8.5	9.0	9.5	V
V_{ILP}	Low-Level Input Voltage	0	0	0.5	V
V_{IHP}	High-Level Input Voltage	2.4	5.0	5.25	V
V_{CCH}	Power Supply During Preload	4.75	5.0	5.25	V
t_{RET}	Pin 2 (3) Delay Time	200			ns
t_{PRLD}	Preload Input Data Delay	300			ns
t_{PSU}	Preload Data Setup Time	100			ns
t_{PC}	Preload Clock Width	1000	1000		ns
t_{PH}	Preload Data Hold Time	100			ns



12950-006B

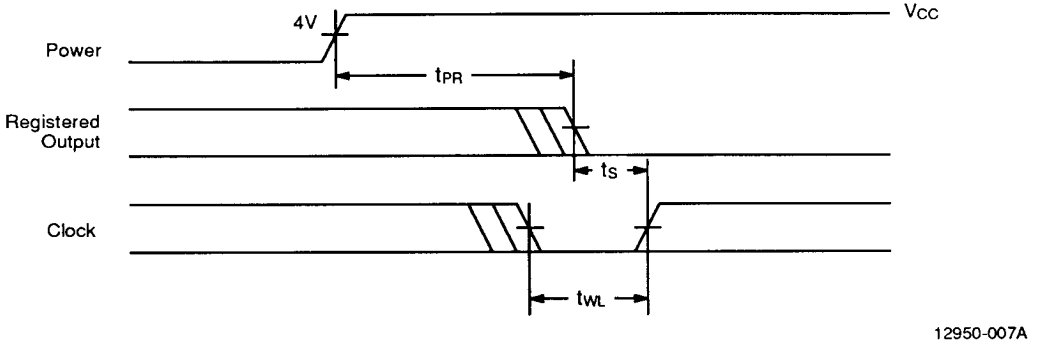
Output Register Preload Waveform

Power-Up Reset

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



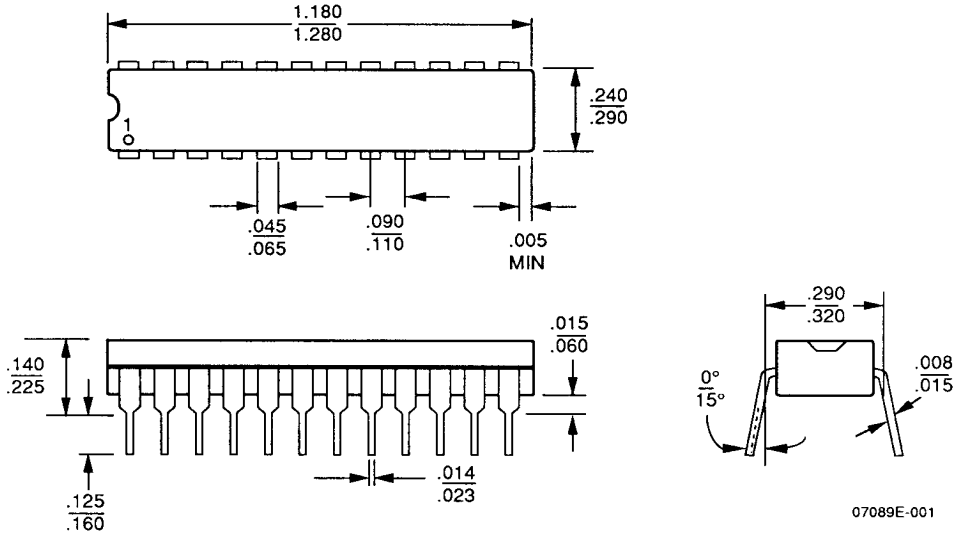
Power-Up Reset Waveform

APPROVED PROGRAMMERS/DEVELOPMENT SYSTEMS (subject to change)

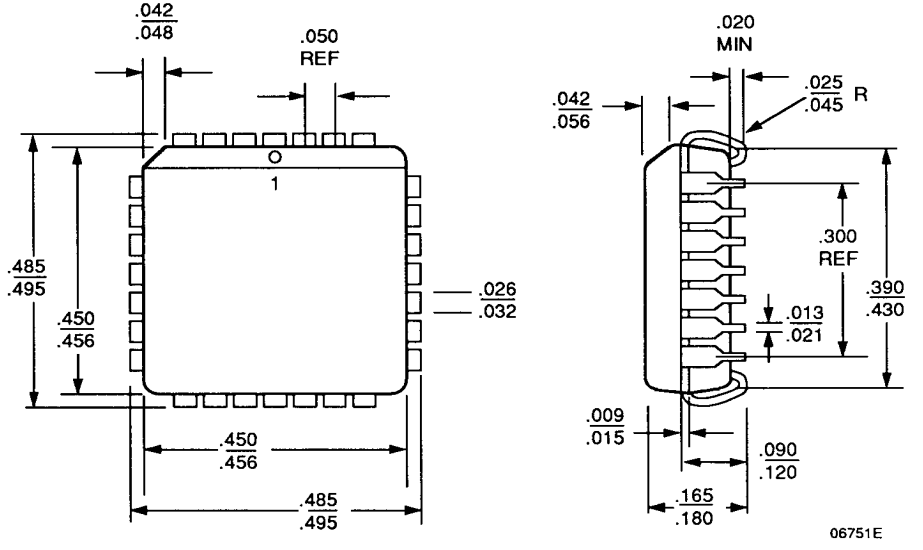
MANUFACTURER	PROGRAMMER CONFIGURATION
Advanced Micro Devices 901 Thompson Place, MS 1028 Sunnyvale, CA 94088-3453 (800) 222-9323 or (408) 732-2400	LabPro™ Rev. 1.2
Adams MacDonald 800 Airport Road Monterey, CA 93940 (408) 373-3607	Contact Manufacturer
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	UniSite™ 40 Rev. 3.0 Family/Pinout Code 80–59
Digelec Inc. 22736 Vanowen Canoga Park, CA 91307 (800) 367-8750 or (818) 887-3755	Contact Manufacturer
Kontron Electronics Inc. 630 Clyde Ave. Mountain View, CA 94039-7230 (800) 227-8834 or (415) 965-7020	Contact Manufacturer
Logical Devices Inc. 1201 E. Northwest 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	Contact Manufacturer
Microprоss Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47.90.40	Contact Manufacturer
Stag Microsystems Inc. 1600 Wyatt Drive, Suite 3 Santa Clara, CA 95054 (408) 988-1118	Contact Manufacturer
Varix Corporation 1210 E. Campbell Road, Suite 100 Richardson, TX 75081 (214) 437-0777	Contact Manufacturer
MANUFACTURER	**SOFTWARE DEVELOPMENT SYSTEM**
Advanced Micro Devices 901 Thompson Place, MS 1028 Sunnyvale, CA 94088-3453 (800) 222-9323 or (408) 732-2400	PALASM 90 or later
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	ABEL™ Software, Rev. 3.1 or later
Logical Devices 1201 E. Northwest 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software, Rev. 3.0 or later

CUPL is a trademark of Logical Devices.
GAL is a registered tradmark of Lattice Semiconductor Corp.
LabPro is a trademark of Advanced Micro Devices.
LogicPak, UniSite and ABEL are trademarks of Data I/O Corporation.

PHYSICAL DIMENSIONS
PD 3024
24-Pin Plastic SKINNYDIP



PL 028
28-Pin Plastic Leaded Chip Carrier



Sales Offices

North American

ALABAMA		(205) 882-9122
ARIZONA		(602) 242-4400
CALIFORNIA,		
Culver City		(213) 645-1524
Newport Beach		(714) 752-6262
Roseville		(916) 786-6700
San Diego		(619) 560-7030
San Jose		(408) 452-0500
Woodland Hills		(818) 992-4155
CANADA, Ontario,		
Kanata		(613) 592-0060
Willowdale		(416) 224-5193
COLORADO		(303) 741-2900
CONNECTICUT		(203) 264-7800
FLORIDA,		
Clearwater		(813) 530-9971
Ft. Lauderdale		(305) 776-2001
Orlando (Casselberry)		(407) 830-8100
GEORGIA		(404) 449-7920
ILLINOIS,		
Chicago (Itasca)		(312) 773-4422
Naperville		(312) 505-9517
KANSAS		(913) 451-3115
MARYLAND		(301) 796-9310
MASSACHUSETTS		(617) 273-3970
MICHIGAN		(313) 347-1522
MINNESOTA		(612) 938-0001
NEW JERSEY,		
Cherry Hill		(609) 662-2900
Parsippany		(201) 299-0002
NEW YORK,		
Liverpool		(315) 457-5400
Poughkeepsie		(914) 471-8180
Rochester		(716) 272-9020
NORTH CAROLINA		(919) 878-8111
OHIO,		
Columbus (Westerville)		(614) 891-6455
OREGON		(503) 245-0080
PENNSYLVANIA		(215) 398-8006
SOUTH CAROLINA		(803) 772-6760
TEXAS,		
Austin		(512) 346-7830
Dallas		(214) 934-9099
Houston		(713) 785-9001
UTAH		(801) 264-2900

International

BELGIUM, Bruxelles	TEL	(02) 771-91-42
	FAX	(02) 762-37-12
	TLX	846-61028
FRANCE, Paris	TEL	(1) 49-75-10-10
	FAX	(1) 49-75-10-13
	TLX	263282F
WEST GERMANY,		
Hannover area	TEL	(0511) 736085
	FAX	(0511) 721254
	TLX	922850
München	TEL	(089) 4114-0
	FAX	(089) 406490
	TLX	523883
Stuttgart	TEL	(0711) 62 33 77
	FAX	(0711) 625187
	TLX	721882
HONG KONG,	TEL	852-5-8654525
Wanchai	FAX	852-5-8654335
	TLX	67955AMDAPHX
ITALY, Milan	TEL	(02) 3390541
		(02) 3533241
	FAX	(02) 3498000
	TLX	843-315286
JAPAN,		
Kanagawa	TEL	462-47-2911
	FAX	462-47-1729
Tokyo	TEL	(03) 346-7550
	FAX	(03) 342-5196
	TLX	J24064AMDTKOJ
Osaka	TEL	06-243-3250
	FAX	06-243-3253

International (Continued)

KOREA, Seoul	TEL	822-784-0030
	FAX	822-784-8014
LATIN AMERICA,		
Ft. Lauderdale	TEL	(305) 484-8600
	FAX	(305) 485-9736
	TLX	5109554261 AMDFTL
NORWAY, Hovik	TEL	(03) 010156
	FAX	(02) 591959
	TLX	79079HBCN
SINGAPORE	TEL	65-3481188
	FAX	65-3480161
	TLX	55650 AMDMMI
SWEDEN,		
Stockholm	TEL	(08) 733 03 50
(Sundbyberg)	FAX	(08) 733 22 85
	TLX	11602
TAIWAN	TEL	886-2-7213393
	FAX	886-2-7723422
	TLX	886-2-7122066
UNITED KINGDOM,		
Manchester area	TEL	(0925) 828008
(Warrington)	FAX	(0925) 827693
	TLX	851-628524
London area	TEL	(0483) 740440
(Woking)	FAX	(0483) 756196
	TLX	851-859103

North American Representatives

CANADA		
Burnaby, B.C.		
DAVETEK MARKETING		(604) 430-3680
Calgary, Alberta		
DAVETEK MARKETING		(403) 291-4984
Kanata, Ontario		
VITEL ELECTRONICS		(613) 592-0060
Mississauga, Ontario		
VITEL ELECTRONICS		(416) 676-9720
Lachine, Quebec		
VITEL ELECTRONICS		(514) 636-5951
IDAHO		
INTERMOUNTAIN TECH MKTG, INC		(208) 888-6071
ILLINOIS		
HEARTLAND TECH MKTG, INC		(312) 577-9222
INDIANA		
Huntington - ELECTRONIC MARKETING CONSULTANTS, INC		(317) 921-3450
Indianapolis - ELECTRONIC MARKETING CONSULTANTS, INC		(317) 921-3450
IOWA		
LORENZ SALES		(319) 377-4666
KANSAS		
Merriam – LORENZ SALES		(913) 384-6556
Wichita – LORENZ SALES		(316) 721-0500
KENTUCKY		
ELECTRONIC MARKETING CONSULTANTS, INC		(317) 921-3452
MICHIGAN		
Birmingham - MIKE RAICK ASSOCIATES		(313) 644-5040
Holland – COM-TEK SALES, INC		(616) 392-7100
Novi – COM-TEK SALES, INC		(313) 344-1409
MISSOURI		
LORENZ SALES		(314) 997-4558
NEBRASKA		
LORENZ SALES		(402) 475-4660
NEW MEXICO		
THORSON DESERT STATES		(505) 293-8555
NEW YORK		
East Syracuse – NYCOM, INC		(315) 437-8343
Woodbury – COMPONENT CONSULTANTS, INC		(516) 364-8020
OHIO		
Centerville – DOLFUSS ROOT & CO		(513) 433-6776
Columbus – DOLFUSS ROOT & CO		(614) 885-4844
Strongsville – DOLFUSS ROOT & CO		(216) 238-0300
PENNSYLVANIA		
DOLFUSS ROOT & CO		(412) 221-4420
PUERTO RICO		
COMP REP ASSOC, INC		(809) 746-6550
UTAH, R^2 MARKETING		(801) 595-0631
WASHINGTON		
ELECTRA TECHNICAL SALES		(206) 821-7442
WISCONSIN		
HEARTLAND TECH MKTG, INC		(414) 792-0920

Advanced Micro Devices, Inc. 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088, USA
Tel: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450
APPLICATIONS HOTLINE TOLL FREE: (800) 222-9323 • (408) 749-5703

2/2/90
WCP-20M-3/90-0 Printed in USA