Features

- **16-bit Fixed-point Digital Signal Processing (DSP) Core**
- **Low-power Consumption:**
  - **ATC35/ATL35 - 2 mW/MIPS at 3.3V**
  - **ATC25/ATL25 - 1 mW/MIPS at 2.5V**
  - **ATC20/ATL20 - 0.6 mW/MIPS at 1.8V**
- **High Performance:**
  - **ATC35/ATL35 - 52 MIPS, 104 MHz at 3.0V/85°C (worst case)**
  - **ATC25/ATL25 - 70 MIPS, 140 MHz at 2.25V/85°C (worst case)**
  - **ATC20/ATL20 - 65 MIPS, 130 MHz at 1.6V/85°C (worst case)**
- **Small Die Size:**
  - **ATC35/ATL35 - 2.5 mm^2**
  - **ATC25/ATL25 - 1.3 mm^2**
  - **ATC20/ATL20 - 1.3 mm^2**
- **Slow Mode and Stop Mode allow Further Power Reduction**
- **Wide Range of Operating Voltage: 1.8V - 3.6V**
- **High Level of Modularity:**
  - **Expandable Data and Program RAM and/or ROM**
  - **User-definable Registers**
- **64K x 16-bit Data Address Space, 64K x 16-bit Program Address Space**
- **Three Parallel Execution Units**
- **Wait States are Supported to Link with Slow External Devices**
- **Advanced Windows-based Development Tools: Macro Assembler, Linker, C Compiler, Debugger (emulator, simulator)**
- **Optional 'On-core Emulator' Allows the On-core Debugger, Embedded in the ASIC, to be Run**
- **JTAG Serial Interface for On-chip Debug (optional)**

Description

Atmel's embedded OakDSPCore® is a 16-bit general-purpose low-power, low-voltage and high-speed digital signal processor (DSP). It is designed for mid-to-high-end telecommunications and consumer electronics applications, where low power and portability are major requirements. Among the applications supported are digital cellular telephones, fast modems, advanced facsimile machines and hard disk drives.

OakDSPCore is available as a DSP core in Atmel's standard cell library, to be utilized as an engine for DSP-based ASICs. It is specified with several levels of modularity in RAM, ROM and I/O blocks, allowing efficient DSP-based ASIC development.

OakDSPCore is aimed at achieving the best cost-performance factor for a given (small) silicon area. As a key element of a system-on-chip, it takes into account such requirements as program size, data memory size, glue logic, power management, etc.

The OakDSPCore consists of three main execution units operating in parallel: the Computation/Bit Manipulation Unit (CBU), the Data Address Arithmetic Unit (DAAU) and the Program Control Unit (PCU). The core also contains ROM and RAM addressing units, and Program Control Logic (PCL). All other peripheral blocks, which are application specific, are defined as a part of the user-specific logic, implemented around the DSP core on the same silicon die.

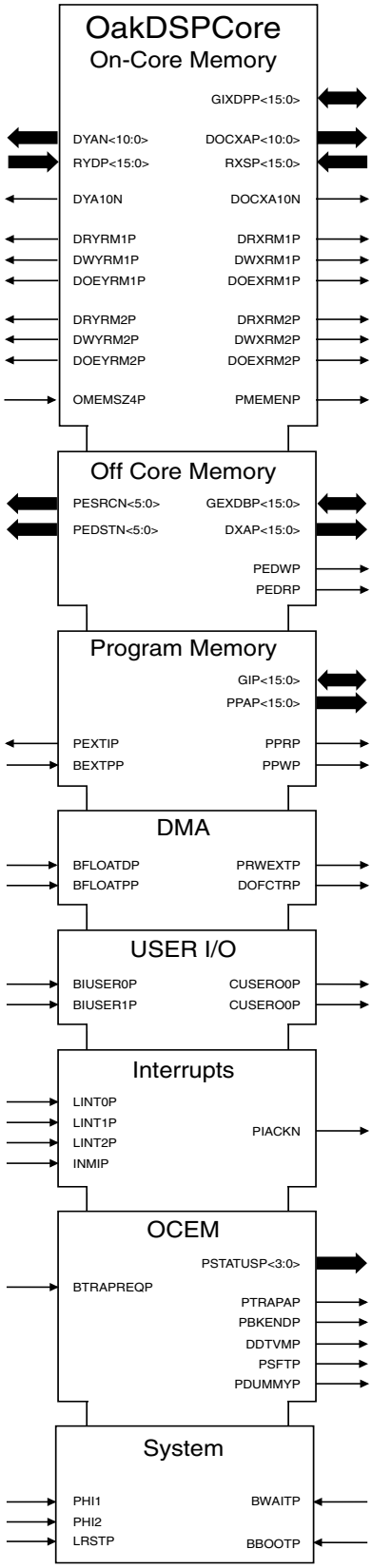
OakDSPCore has an enhanced set of DSP and general microprocessor functions to meet the application requirements. The OakDSPCore programming model and instruction set are aimed at straightforward generation of efficient and compact code.

Embedded Digital Signal Processing Core

OakDSPCore®

Rev. 0876E–03/00

Figure 1. Symbol



Signal Description

Table 1. On-core Memory

Signal Name	Width	Description
Input Signals		
RYDP <15:0>	16	YRAM data bus
OMEMSZ4P	1	Memory size 4K
RXSP <15:0>	16	XRAM data bus
Input/Output Signals		
GIXDBP <15:0>	16	Internal data bus
Output Signals		
DYAN <10:0>	11	On-core YRAM address
DYA10N	1	On-core YRAM address - bit 10
DRYRM1P	1	On-core YRAM read (lower 1K)
DWYRM1P	1	On-core YRAM write (lower 1K)
DOEYRM1P	1	On-core YRAM output enable (lower 1K)
DRYRM2P	1	On-core YRAM read (upper 1K)
DWYRM2P	1	On-core YRAM write (upper 1K)
DOEYRM2P	1	On-core YRAM output enable (upper 1K)
DOCXAP <10:0>	11	On-core XRAM address
DOCXA10N	1	On-core XRAM address - bit 10
DRXRM1P	1	On-core XRAM read (lower 1K)
DWXRM1P	1	On-core XRAM write (lower 1K)
DOEXRM1P	1	On-core XRAM output enable (lower 1K)
DRXRM2P	1	On-core XRAM read (upper 1K)
DWXRM2P	1	On-core XRAM write (upper 1K)
DOEXRM2P	1	On-core XRAM output enable (upper 1K)
PMEMENP	1	Data memory enable

Table 2. Off-core Memory

Signal Name	Width	Description
Input/Output Signals		
GEXDBP <15:0>	16	External data bus
Output Signals		
PESRCN <5:0>	6	Source bus
PEDSTN <5:0>	6	Destination bus
DXAP <15:0>	16	Off-core XRAM address
PEDWP	1	Data write
PEDRP	1	Data read

Table 3. Program Memory

Signal Name	Width	Description
Input Signals		
BEXTPP	1	External program indication
Input/Output Signals		
GIP <15:0>	16	Instruction data
Output Signals		
PEXTIP	1	MOVP instruction indication
PPAP <15:0>	16	Program address
PPRP	1	Program read
PPWP	1	Program write

Table 4. Direct Memory Access (DMA)

Signal Name	Width	Description
Input Signals		
BFLOATDP	1	Float DXAP bus control
BFLOATPP	1	Float PPAP bus control
Output Signals		
PRWEXTP	1	Read or write to/from external registers
DOFCTRP	1	Off core data transaction

Table 5. User I/O

Signal Name	Width	Description
Input Signals		
BIUSER0P	1	User input 0
BIUSER1P	1	User input 1

Table 5. User I/O (Continued)

Signal Name	Width	Description
Output Signals		
CUSERO0P	1	User output 0
CUSERO1P	1	User output 1

Table 6. Interrupts

Signal Name	Width	Description
Input Signals		
LINT0P	1	Interrupt 0
LINT1P	1	Interrupt 1
LINT2P	1	Interrupt 2
LNMIP	1	Non-maskable Interrupt
Output Signals		
PIACKN	1	Interrupt acknowledge

Table 7. On-Chip Emulation Module (OCEM)

Signal Name	Width	Description
Input Signals		
BTRAPREQP	1	TRAP interrupt
Output Signals		
PSTATUSP <3:0>	4	Internal status (used by the OCEM module)
PTRAPAP	1	Trap active indication
PBKENDP	1	Block repeat end
DDTVMP	1	Data value match
PSFTP	1	Software trap indication
PDUMMYP	1	Dummy fetch (used by the OCEM module)

Table 8. System

Signal Name	Width	Description
Input Signals		
PHI1	1	Phase1 Clock
PHI2	1	Phase2 Clock
LRSTP	1	Reset
BWAITP	1	Wait state indication
BBOOTP	1	BOOT indication

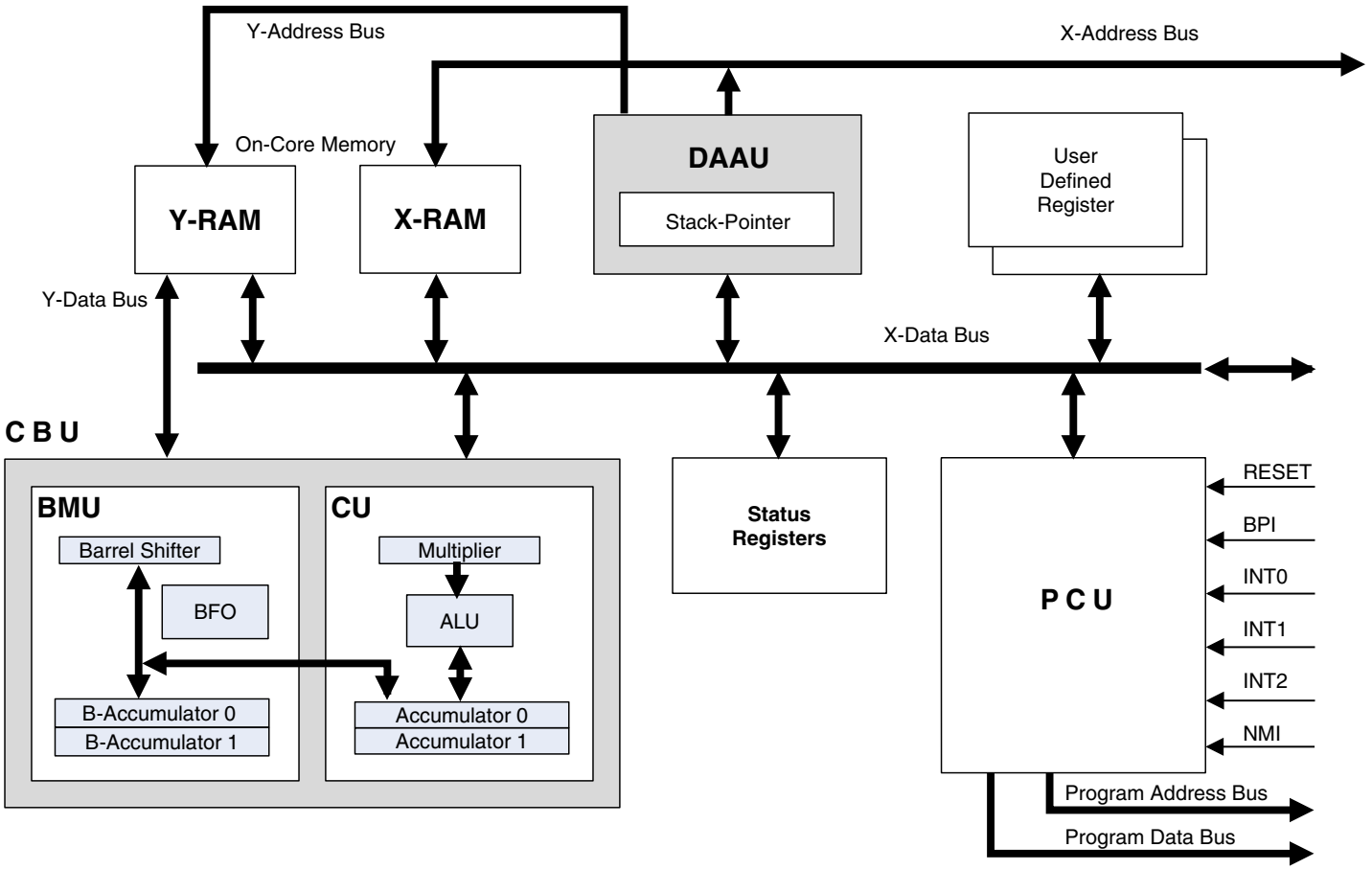
OakDSPCore Architecture

The OakDSPCore consists of three main execution units operating in parallel:

- The Computation/Bit Manipulation Unit (CBU)
- The Data Address Arithmetic Unit (DAAU)
- The Program Control Unit (PCU)

The OakDSPCore also supports four user-definable registers, enabling future expansion of the core residing in off-core glue logic. The user defined registers are part of the core register set, meaning that they can be accessed by most OAK instructions.

Figure 2. OakDSPCore Block Diagram



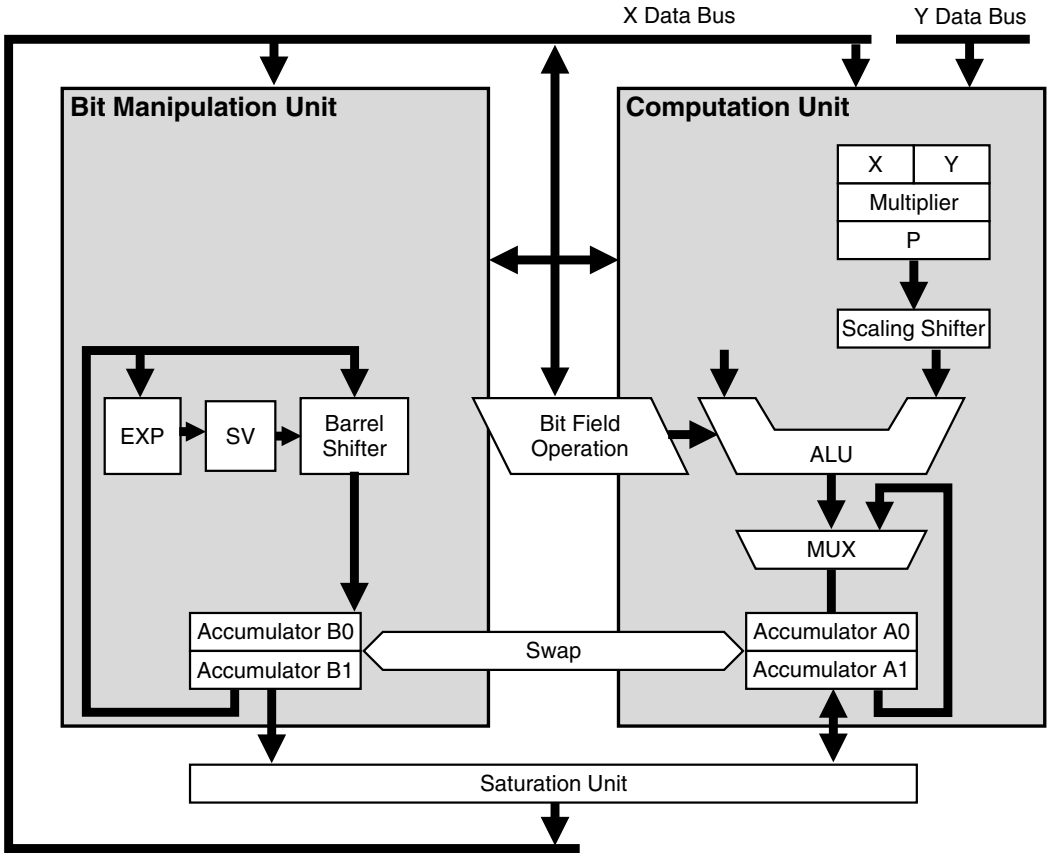
Note: X- and Y-RAM sizes depend on the customer's need. The variable size minimizes overhead area.

Computation/Bit Manipulation Unit

The Computation/Bit Manipulation Unit (CBU) contains three main elements:

- The Computation Unit (CU)
- The Bit Manipulation Unit (BMU).
- The Saturation Unit, which is shared by the CU and the BMU units.

Figure 3. Computation and Bit Manipulation Unit Block Diagram



The CU consists of a 16- by 16-bit parallel 2s complement multiplier, supporting single and double precision multiplication, a 36-bit Arithmetical and Logical Unit (ALU) and two 36-bit A-accumulators with access to the two additional B-accumulators of the BMU. The OakDSPCore can perform a single-cycle Multiply-Accumulate (MAC) instruction, and has support for double precision multiplication. A single-cycle division step is supported.

The Arithmetic Logic Unit (ALU) performs all arithmetic and logical operations on data operands. It is a 36-bit, single-cycle, non-pipelined unit. A maximum or minimum operation is available.

The BMU consists of a full 36-bit barrel shifter, a Bit-Field Operation (BFO) unit, a special hardware (EXP) for exponent calculation, and two 36-bit B-accumulators with access to the two A-accumulators of the CU. Extension nibbles of the B-accumulators offer protection against 32-bit overflows. The Shift Value (SV) register is a 16-bit register used for shifting operation and exponent calculation.

Context switching (swapping) between the two sets of accumulators is supported.

Saturation arithmetic is provided to selectively limit overflow from the high portion of an accumulator to the extension bits. When necessary the saturation logic substitutes a limited data value having maximum magnitude and the same sign as the source accumulator.

Data Address Arithmetic Unit

The Data Address Arithmetic Unit (DAAU) performs all address storage and effective address calculations necessary to address data operands in data and program memories. It also supports the software stack pointer. This unit operates in parallel with other core resources to minimize address generation overhead. The DAAU contains six 16-bit address registers for indirect addressing, two 16-bit configuration registers for modulo and increment or decrement step control, and a base register for supporting index addressing. In addition, it contains a 16-bit stack pointer register and four alternative bank registers that are supported by an individual bank exchange. A 16-bit minimum and maximum pointer latching register also is contained.

The DAAU can generate two 16-bit addresses every instruction cycle. These can be post-modified by two modifiers: linear and modulo modifier. The address modifiers allow the creation of data structures in memory for circular buffers, delay lines, FIFOs, another pointer to the software stack, etc.

Program Control Unit

The Program Control Unit (PCU) performs instruction fetch, instruction decoding, exception handling, hardware loop control, wait state support and on-chip emulation support. In addition, it controls the internal program memory protection.

The PCU contains the Repeat and Block-Repeat unit, and two 16-bit directly accessible registers: the Program Counter and the Loop Counter of the block-repeat unit.

Instruction Set

The OAK instruction set is balanced between DSP and control functions, thus permitting both DSP and high-speed control activities.

There are a total of 89 instructions. All have been carefully designed to produce compact code. The OakDSPCore has an internal four-stage pipeline which continually performs concurrent instruction fetch, decode fetch, operand fetch and instruction execution. This allows instruction execution to overlap, thus the effective execution time for most instructions is one cycle. Of particular significance are the repeat and block repeat (four nested levels) capabilities.

This instruction set optimizes the OakDSPCore for algorithms such as Viterbi decoding, adaptive filtering, and cellular phone applications.

On-Chip Emulation

The OakDSPCore has the capability to be combined with an On-Chip Emulation Module (OCEM). The OCEM provides hardware emulation and program flow trace buffering. Hardware emulation allows breakpoints due to a pre-defined condition such as program or data address match, single stepping, etc.

Program flow buffer records, during run time, those instruction addresses that cause a non-continuity in the program flow. These addresses are kept in a FIFO within the OCEM block and used afterwards to re-construct the complete program flow graph.

Development Tools

Development tools are a critical element in core-based ASIC design as they affect the design cycle and the time-to-market. For ease of development of DSP-based applications, the OakDSPCore is supplied with a comprehensive set of hardware and software tools, and a development platform for rapid prototyping. These feature a familiar design technology, full-speed and real-time emulation/simulation, easy of use and interactivity.

Hardware Development Tools

The OakDSPCore hardware tools include the ODKit standalone board, ODKit Accelerator, and the Combo Debug Interface (CDI). The ODKit/CDI is a unified line of development tools which provides the user the ability to develop and debug an application-specific Oak-based system in the same software environment.

The ODKit also has a reduced version called the Accelerator. The Accelerator provides the user the ability of very fast turn-key development of firmware (and application specific software) as well as a hardware acceleration engine for heavy simulations. The Accelerator doesn't provide a prototyping ability. The stand-alone ODKit provides the user an ability of fast prototyping of application specific hardware. So three different products are established in the product line: the Accelerator, the stand-alone ODKit and the CDI. The last two devices use an ISA Extender card for the PC host link, while the Accelerator must be plugged into an ISA bus connector of the host PC.

The ODKit is designed for prototyping during COMBO (Oak based ASIC) development stage, whereas the CDI is designed for COMBO debug and/or re-targeting stages. Both devices support a stand-alone (demo mode) operation. Both the stand-alone ODkit and ODkit accelerator card include an Oak development chip, program and data memory, boot logic, EPROM socket, dual-ported monitor

MAILBOX memory, and CODEC with audio input and output connectors.

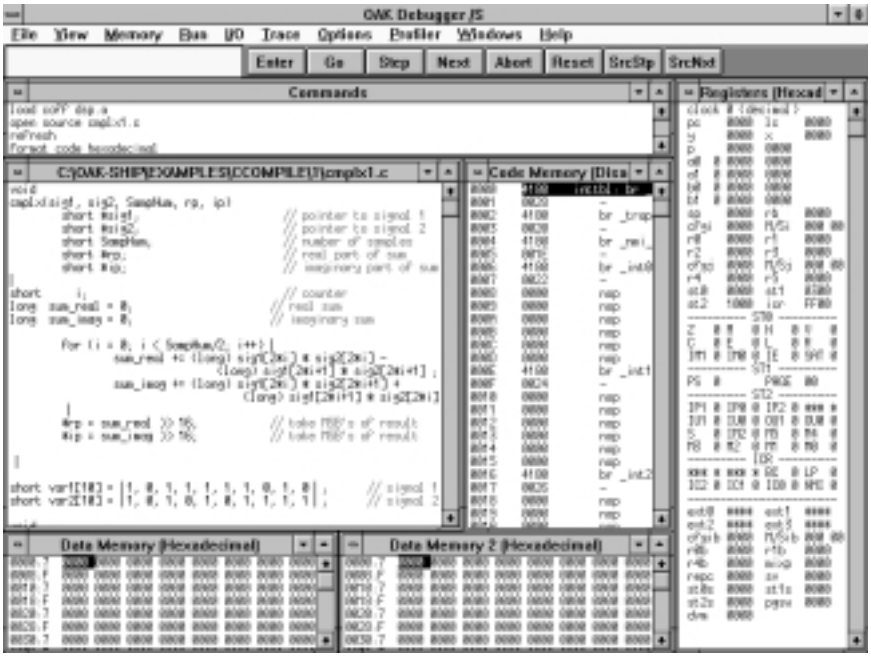
The CDI contains the PC ISA host interface, dual-ported monitor MAILBOX memory, program memory, EPROM socket, boot logic, C-bus interface and target connector interface. It does not include the Oak development chip or Oak socket like the Odkit boards. The CDI would be used for hardware verification/debug of an Oak based ASIC or ASSP that has a different package than the Oak development chip.

Software Development Tools

The OakDSPCore command line software tools include a COFF macro assembler and linker, and ANSI C compiler. The GUI based tools include the COFF symbolic debugger and ASSYST simulator. The ASSYST simulator is used to simulate external hardware in simulation mode before actual target hardware is available.

The debugger can operate in either emulation or simulation modes on a PC, depending upon whether Oak-based target hardware is attached. The debugger supports source level debugging in assembly, C/C++, or mixed assembly and C/C++ modes. It also includes a disassembler, an inline assembler, and an application profiler. In simulation mode the application profiler indicates memory usage, program flow, instruction usage, real time consumption and more. The software tools are available for Windows 3.1, Windows® 95, and Windows NT® operating systems. As a UNIX/Motif compatible application, it can run on Sun SPARC workstations in simulation mode only.

Figure 4. Windows User Interface of the OAK Development Kit



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