

LH53H1100

PRELIMINARY
CMOS 1M (128K × 8) Mask Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 35 ns (MAX.)
- Power consumption:
Operating: 660 mW (MAX.)
Standby: 440 mW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
32-pin, 600-mil DIP
32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53H1100 is a high speed mask programmable ROM organized as 131,072 × 8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

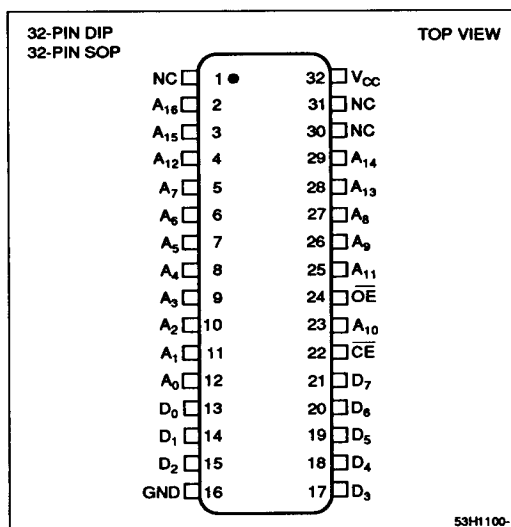
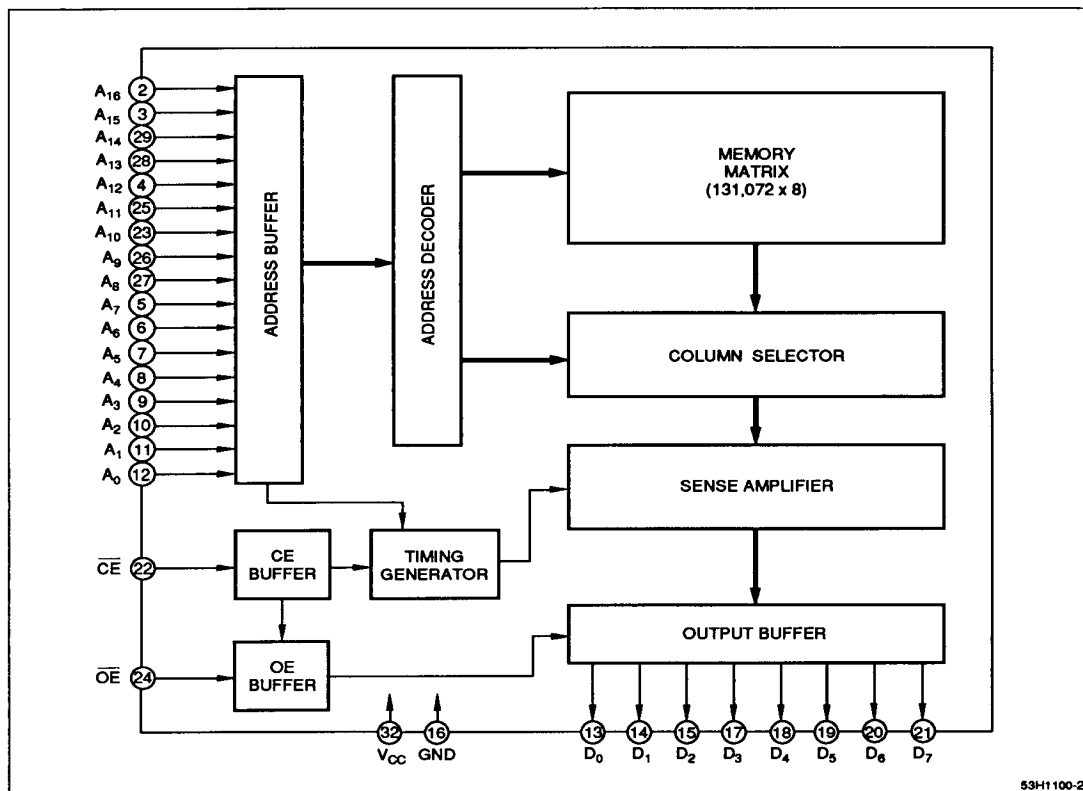


Figure 1. Pin Connections for DIP and SOP Packages



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Figure 2. LH53H1100 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₅	Address input
D ₀ - D ₇	Data output
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V _{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	D ₀ - D ₇	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby (I _{SB})	1
L	H	Non selected	High-Z	Operating (I _{CC})	
L	L	Selected	DOUT	Operating (I _{CC})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V	
Output voltage	V _{OUT}	-0.3 to V _{CC} +0.3	V	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		-0.3		0.8	V	
Input "High" voltage	V _{IH}		2.2		V _{CC} +0.3	V	
Output "Low" voltage	V _{OL}	I _{OL} = 3.2 mA			0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -1.0 mA	2.4			V	
Input leakage current	I _{LI}	V _{IN} = 0 V or V _{CC}			10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V or V _{CC}			10	μA	1
Operating current	I _{CC1}	t _{RC} = 35 ns			120	mA	2
	I _{CC2}	t _{RC} = 35 ns			110		3
Standby current	I _{SB}	$\overline{CE}$ = V _{IH}			80	mA	

NOTES:

1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	35			ns	
Address access time	t_{AA}			35	ns	
Chip enable time	t_{ACE}			35	ns	
Output enable time	t_{OE}			15	ns	
Output hold time	t_{OH}	0			ns	
CE to output in High-Z	t_{CHZ}			15	ns	1
OE to output in High-Z	t_{OHZ}			15	ns	

NOTE:

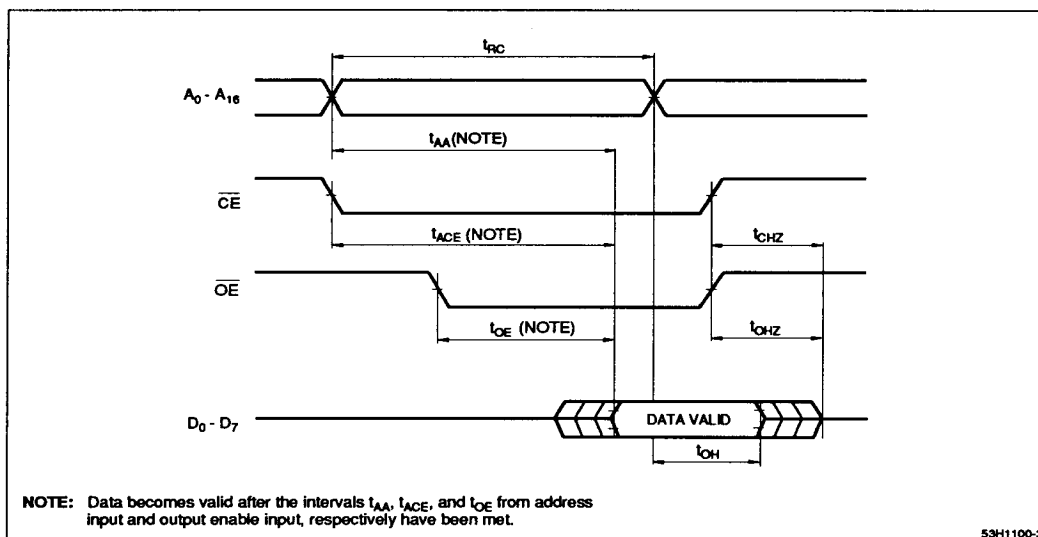
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0 V to 3.0 V
Input rise/fall time	5 ns
Input reference level	1.5 V
Output load condition	1TTL + 30 pF

CAPACITANCE ($V_{CC} = 5\text{ V} \pm 10\%$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



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Figure 3. Timing Diagram**CAUTION**

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION

