

HB56A240 Series

2,097,152-Word x 40-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A240B/SB is a 2M x 40 dynamic RAM module, mounted 20 pieces of 4 Mbit DRAM (HM514400AS) sealed in SOJ package. An outline of the HB56A240B/SB is a 72-pin single in-line package. Therefore, the HB56A240B/SB makes high density mounting possible without surface mount technology. The HB56A240B/SB provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ but only on the one side of its module board.

■ FEATURES

- 72-pin Single In-line Package
Lead Pitch1.27mm
- Single 5V ($\pm 5\%$) Supply
- High Speed
Access Time60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
Operation6038 mW/5513 mW/4988 mW/
4463 mW (max)
Standby210 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles(16 ms)
- 2 Variations of Refresh
RAS Only Refresh
CAS Before RAS Refresh
- TTL Compatible

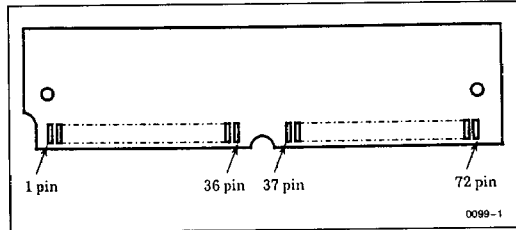
■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56A240B-6A	60 ns	72-pin SIP Socket Type	Gold
HB56A240B-7A	70 ns		
HB56A240B-8A	80 ns		
HB56A240B-10A	100 ns		
HB56A240SB-6A	60 ns	72-pin SIP Socket Type	Solder
HB56A240SB-7A	70 ns		
HB56A240SB-8A	80 ns		
HB56A240SB-10A	100 ns		

■ PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₉	Address Input
A ₀ -A ₈	Refresh Address Input
DQ ₀ -DQ ₃₉	Data-in/Data-out
CAS ₀ , CAS ₁	Column Address Strobe
RAS ₀ , RAS ₀	Row Address Strobe
WE	Read/Write Enable
OE	Output Enable
V _{DD}	Power Supply (+ 5V)
V _{SS}	Ground
PD1-PD4	Presence Detect Pin
NC	No Connection

■ PINOUT



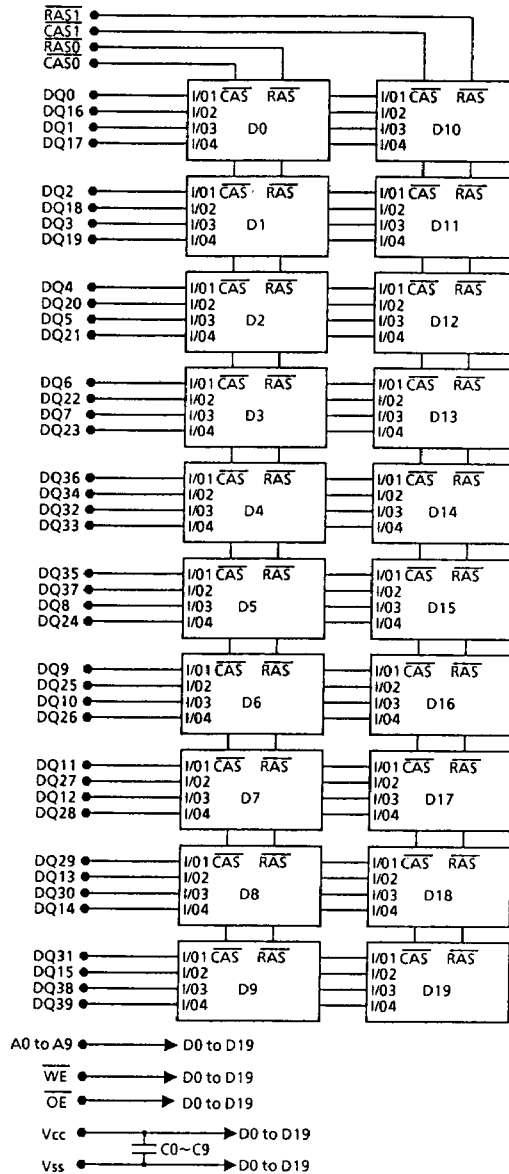
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	OE	37	DQ ₃₃	55	DQ ₁₁
2	DQ ₀	20	DQ ₄	38	DQ ₃₅	56	DQ ₂₇
3	DQ ₁₆	21	DQ ₂₀	39	V _{SS}	57	DQ ₁₂
4	DQ ₁	22	DQ ₅	40	NC	58	DQ ₂₈
5	DQ ₁₇	23	DQ ₂₁	41	CAS ₀	59	V _{DD}
6	DQ ₂	24	DQ ₆	42	CAS ₁	60	DQ ₂₉
7	DQ ₁₈	25	DQ ₂₂	43	NC	61	DQ ₁₃
8	DQ ₃	26	DQ ₇	44	RAS ₀	62	DQ ₃₀
9	DQ ₁₉	27	DQ ₂₃	45	RAS ₁	63	DQ ₁₄
10	V _{DD}	28	A ₇	46	DQ ₃₇	64	DQ ₃₁
11	NC	29	DQ ₃₆	47	WE	65	DQ ₁₅
12	A ₀	30	V _{DD}	48	GND	66	DQ ₃₈
13	A ₁	31	A ₈	49	DQ ₈	67	PD1
14	A ₂	32	A ₉	50	DQ ₂₄	68	PD2
15	A ₃	33	NC	51	DQ ₉	69	PD3
16	A ₄	34	NC	52	DQ ₂₅	70	PD4
17	A ₅	35	DQ ₃₄	53	DQ ₁₀	71	DQ ₃₉
18	A ₆	36	DS ₃₆	54	DQ ₂₆	72	V _{SS}

■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56A240B/SB			
		-6A	-7A	-8A	-10A
67	PD1	NC	NC	NC	NC
68	PD2	NC	NC	NC	NC
69	PD3	NC	V _{SS}	NC	V _{SS}
70	PD4	NC	NC	V _{SS}	V _{SS}



■ BLOCK DIAGRAM

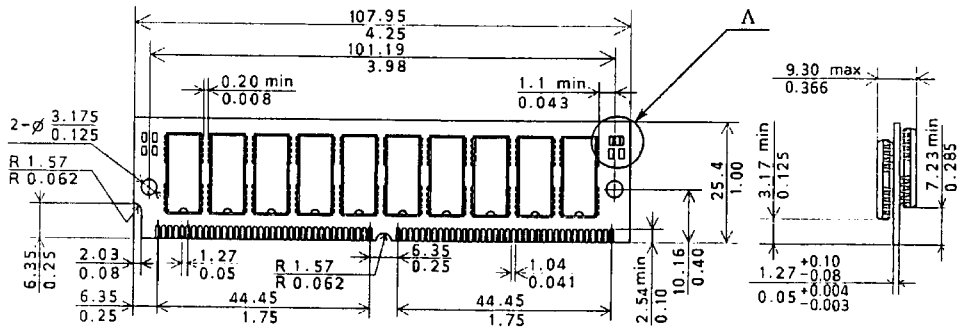


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* D0 to D9: HM514400AS



■ PHYSICAL OUTLINE

Unit: $\frac{\text{mm}}{\text{inch}}$ 

0099-4

Detail A

60ns	70ns	80ns	100ns

0099-5

Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A240B-XXA	Gold
HB56A240SB-XXA	Solder

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	10	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS} .• DC Electrical Characteristics ($T_A = 0$ to +70°C, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$)

Parameter	Symbol	HB56A240B/SB								Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I _{CC1}	—	1150	—	1050	—	950	—	850	mA	t _{RC} = Min	1, 2
Standby Current	I _{CC2}	—	40	—	40	—	40	—	40	mA	TTL Interface RAS, CAS = V _{IH} D _{out} = High-Z	
		—	20	—	20	—	20	—	20	mA	CMOS Interface RAS, CAS ≥ V _{CC} − 0.2V D _{out} = High-Z	
RAS Only Refresh Current	I _{CC3}	—	1150	—	1050	—	950	—	850	mA	t _{RC} = Min	2
Standby Current	I _{CC5}	—	100	—	100	—	100	—	100	mA	RAS = V _{IH} CAS = V _{IL} D _{out} = Enable	1
CAS Before RAS Refresh Current	I _{CC6}	—	1150	—	1050	—	950	—	850	mA	t _{RC} = Min	
Fast Page Mode Current	I _{CC7}	—	1150	—	1050	—	950	—	850	mA	t _{PC} = Min	1, 3
Input Leakage Current	I _{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V _{in} ≤ 7V	
Output Leakage Current	I _{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V _{out} ≤ 7V D _{out} = Disable	
Output High Voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	I _{out} = − 5 mA	
Output Low Voltage	V _{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I _{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.2. Address can be changed less than three times while $\overline{RAS} = V_{IL}$.3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

• **Capacitance** ($T_A = 25^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address A_0 – A_9)	C_{I1}	—	140	pF	1
Input Capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I2}	—	160	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I4}	—	90	pF	1
Input/Output Capacitance (DQ_0 to DQ_{39})	$C_{I/O1}$	—	25	pF	1

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable D_{out} .

• **AC Characteristics** ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$)^{1, 14, 15, 16}

Read, Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	180	—	ns	
RAS Precharge Time	t _{RP}	40	—	50	—	60	—	70	—	ns	
RAS Pulse Width	t _{RAS}	60	10000	70	10000	80	10000	100	100000	ns	
CAS Pulse Width	t _{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	20	—	ns	
RAS to CAS Delay Time	t _{RCD}	20	45	20	50	20	60	25	75	ns	8
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	20	55	ns	9
RAS Hold Time	t _{RSH}	15	—	20	—	20	—	25	—	ns	
CAS Hold Time	t _{CSH}	60	—	70	—	80	—	100	—	ns	
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	10	—	ns	
OE to D _{in} Delay Time	t _{ODD}	15	—	20	—	20	—	25	—	ns	
OE Delay Time from D _{in}	t _{DZO}	0	—	0	—	0	—	0	—	ns	
CAS Setup Time from D _{in}	t _{DZC}	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
Refresh Period	t _{REF}	—	16	—	16	—	16	—	16	ms	

• **Read Cycle**

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from RAS	t _{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 17
Access Time from CAS	t _{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t _{AA}	—	30	—	35	—	40	—	45	ns	3, 4, 13, 16
Access Time from OE	t _{OAC}	—	15	—	20	—	20	—	25	ns	
Read Command Setup Time	t _{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to CAS	t _{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to RAS	t _{RRH}	0	—	0	—	0	—	0	—	ns	
Column Address to RAS Lead Time	t _{RAL}	30	—	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t _{OFF1}	0	15	0	20	0	20	0	20	ns	6
Output Buffer Turn-off Time to OE	t _{OFF2}	0	15	0	20	0	20	0	20	ns	6
CAS to D _{in} Delay Time	t _{CDD}	15	—	20	—	20	—	25	—	ns	



• Write Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	20	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t _{RWC}	150	—	180	—	200	—	245	—	ns	
RAS to WE Delay Time	t _{RWD}	80	—	95	—	105	—	135	—	ns	10
CAS to WE Delay Time	t _{CWD}	35	—	45	—	45	—	60	—	ns	10
Column Address to WE Delay Time	t _{AWD}	50	—	60	—	65	—	80	—	ns	10
OE Hold Time from WE	t _{OEH}	15	—	20	—	20	—	25	—	ns	

• Refresh Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh Cycle)	t _{CSR}	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh Cycle)	t _{CHR}	10	—	10	—	10	—	10	—	ns	
RAS Precharge to CAS Hold Time	t _{RPC}	10	—	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	t _{RASC}	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	—	35	—	40	—	45	—	50	ns	13, 17
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	—	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t _{PCM}	80	—	95	—	100	—	110	—	ns	

• Test Mode Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{\text{WE}}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{\text{WE}}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	ns	

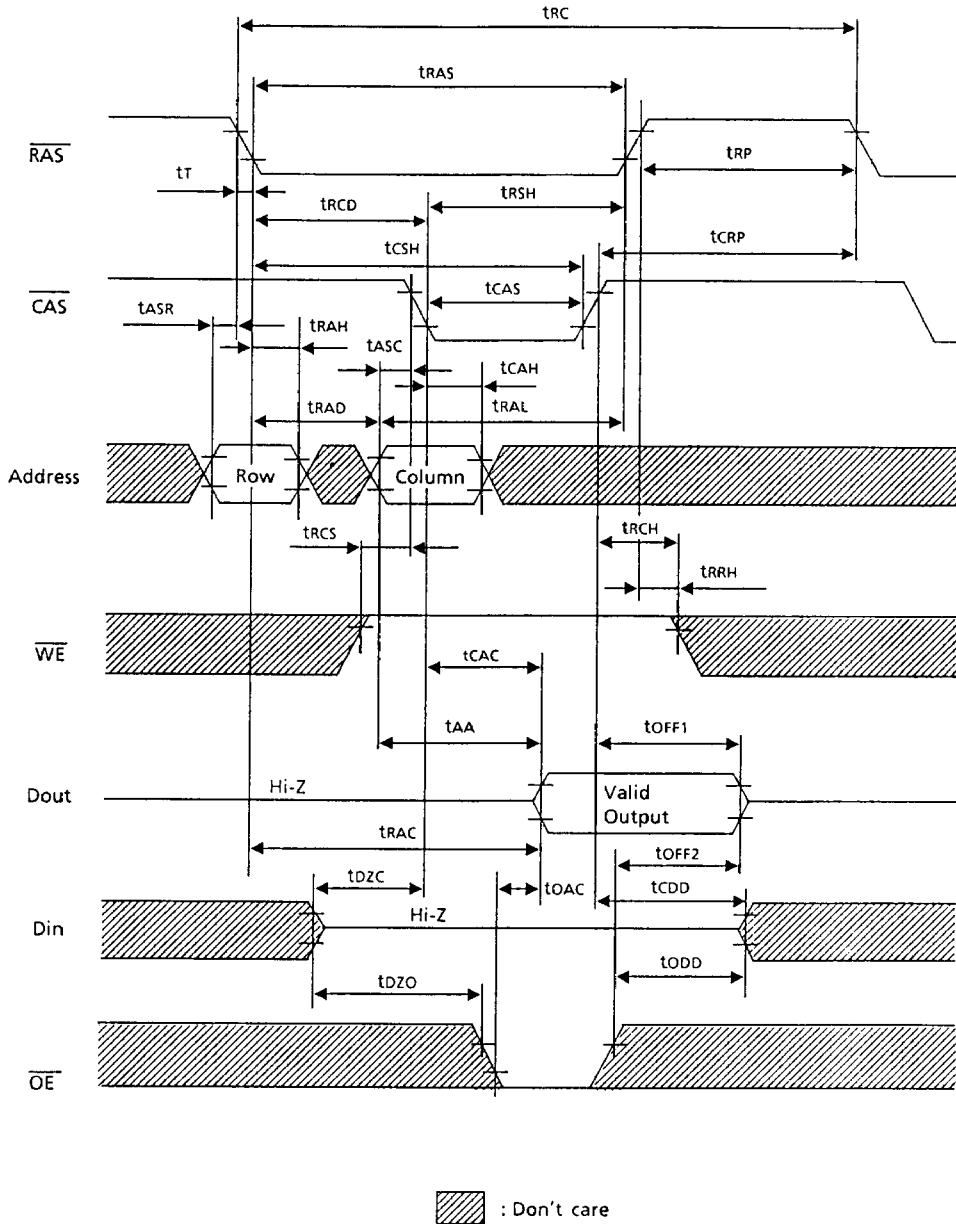
Notes: 1. AC measurements assume $t_T = 5$ ns.

- Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2 TTL load and 100 pF.
- Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.
- Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
- $t_{\text{OFF}}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
- t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of condition is satisfied, the condition of the data out (at access time) is indeterminate.
- These parameters are referenced to $\overline{\text{CAS}}$ leading in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
- t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycle.
- Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
- An initial pulse of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle is required.
- In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
- Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits ... CA0. This test mode operation can be performed by $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is low level. Data output pin is I/O₃ and data input pin is I/O₂. In order to end this test mode operation, perform a $\overline{\text{RAS}}$ only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
- In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.



■ TIMING WAVEFORMS

• Read Cycle

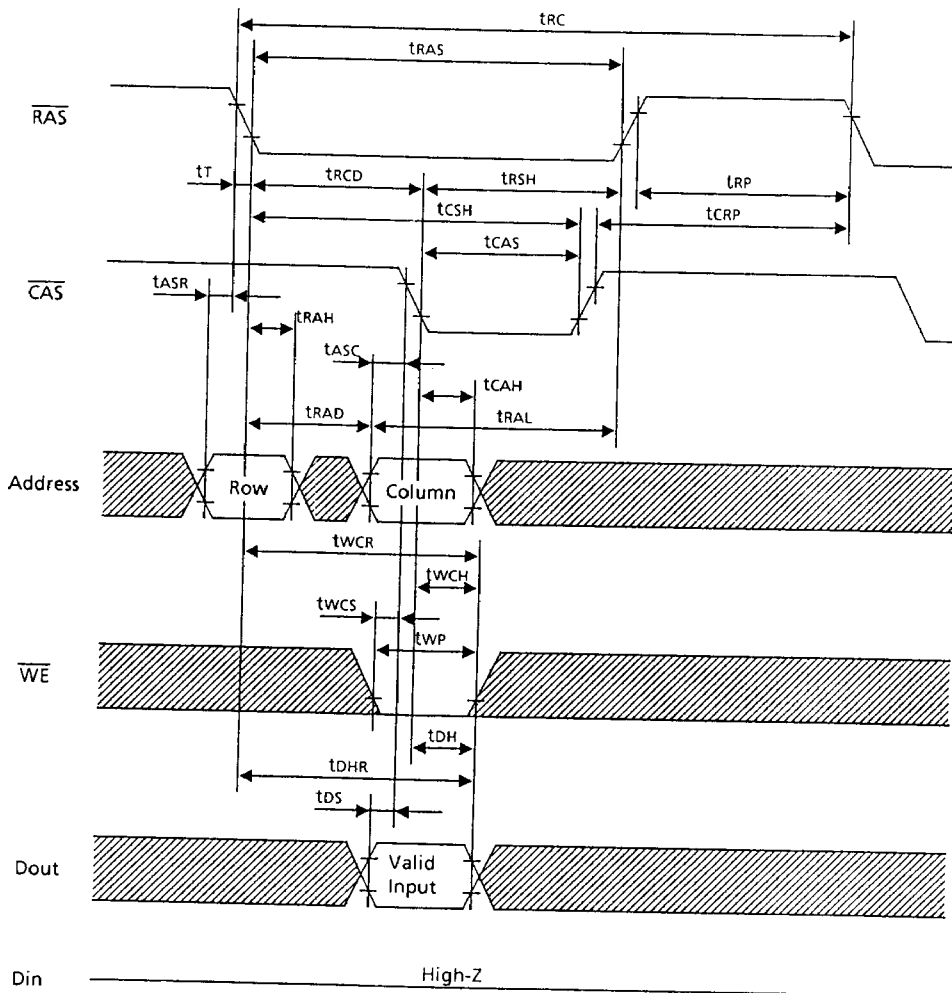


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• Early Write Cycle

HB56A240 Series



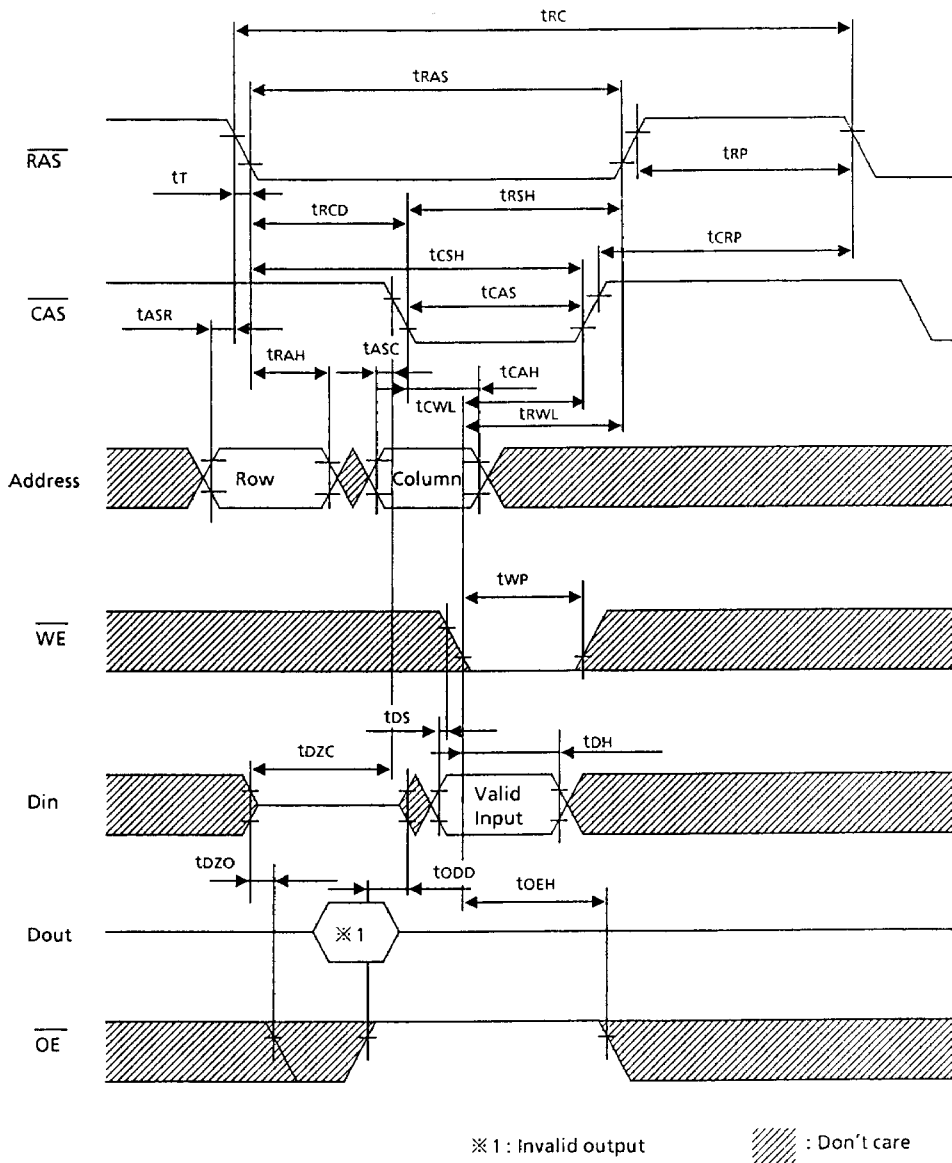
▨ : Don't care

$\overline{OE}$: Don't care

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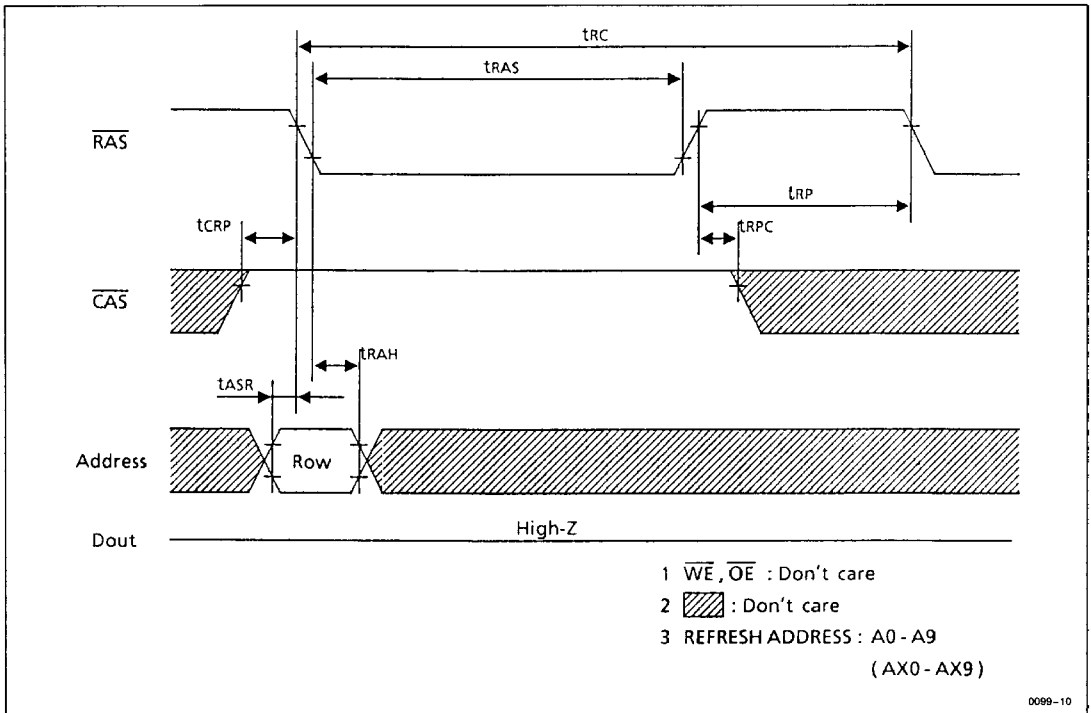
• Delayed Write Cycles



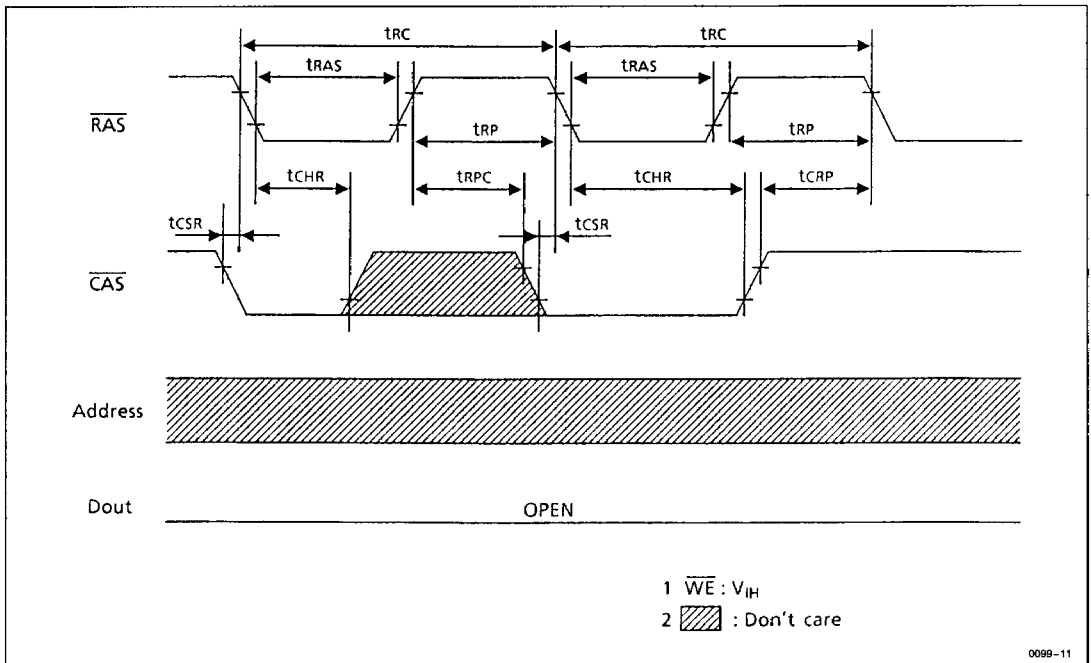
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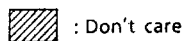


• RAS Only Refresh Cycle



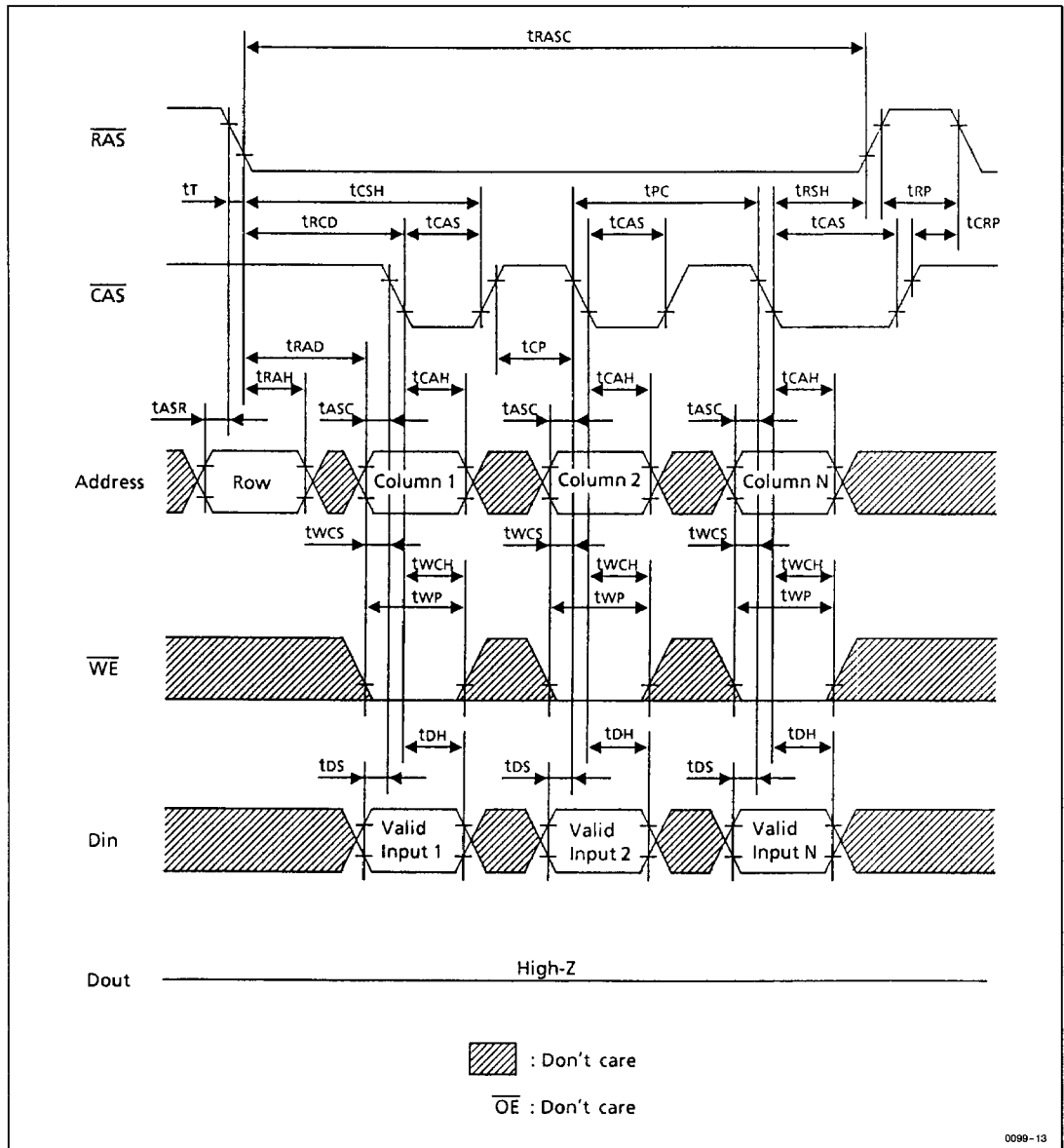
• CAS Before RAS Refresh Cycle





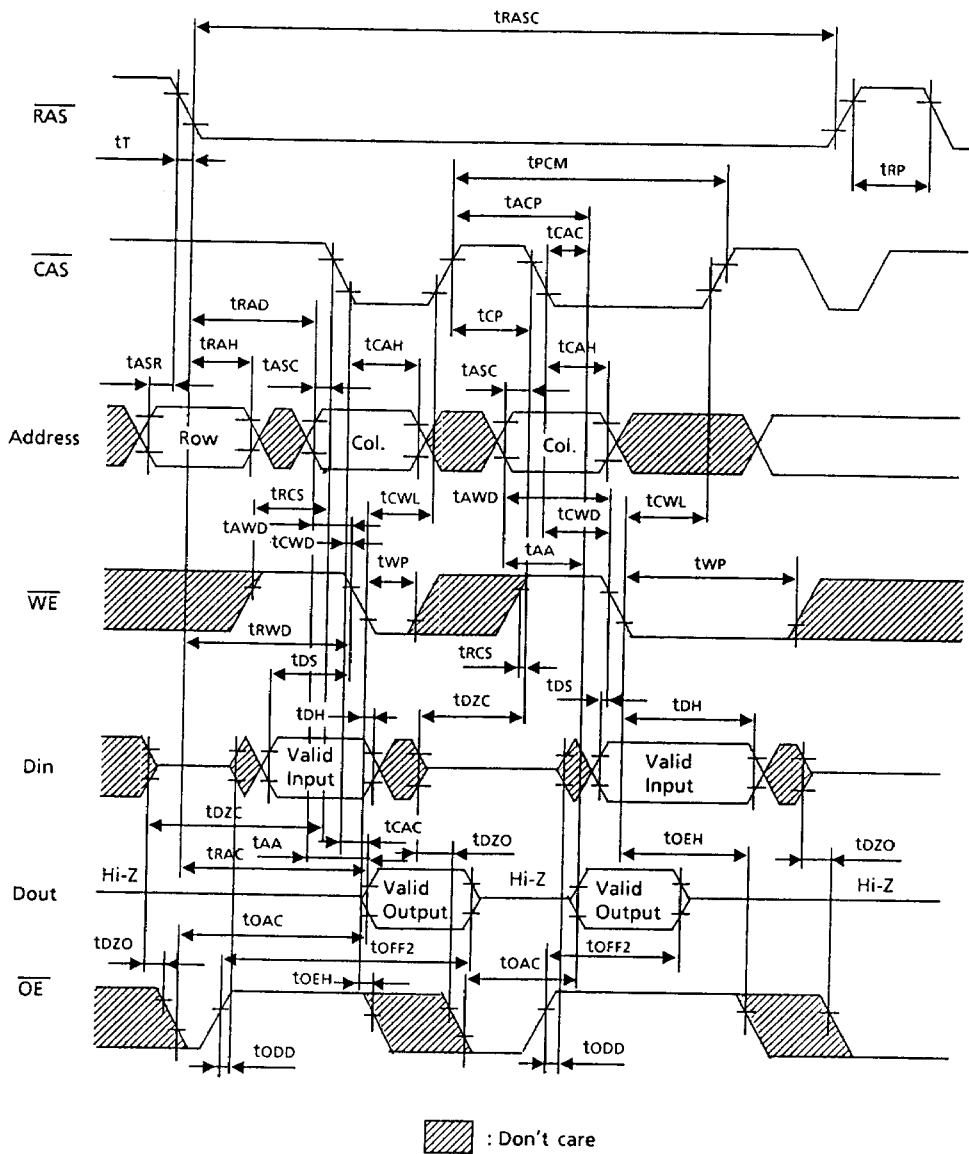
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• Fast Page Mode Early Write Cycle





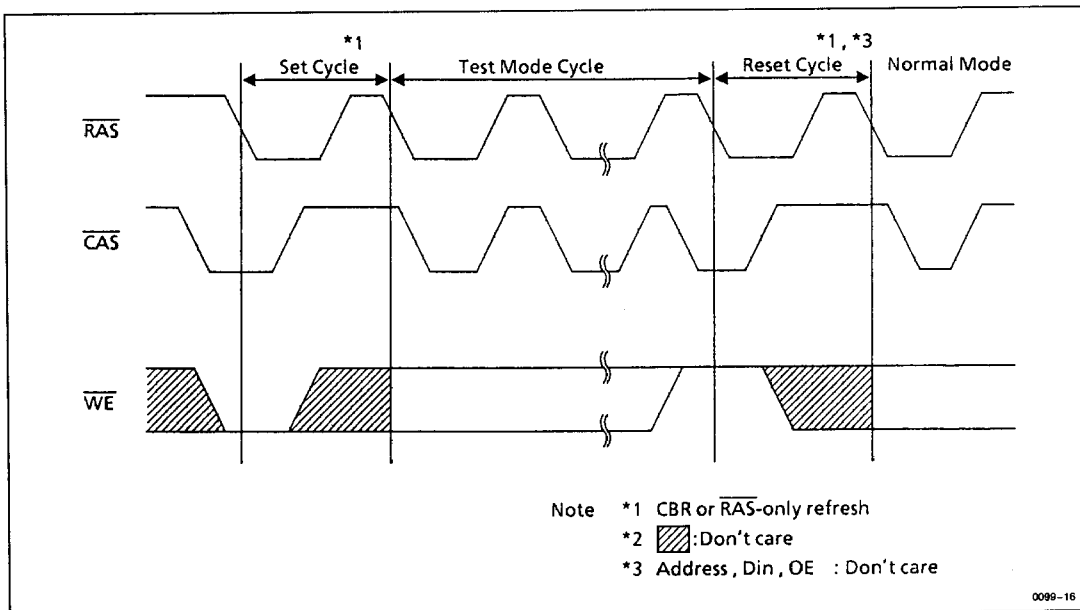
• Fast Page Mode Read-Modify-Write Cycle



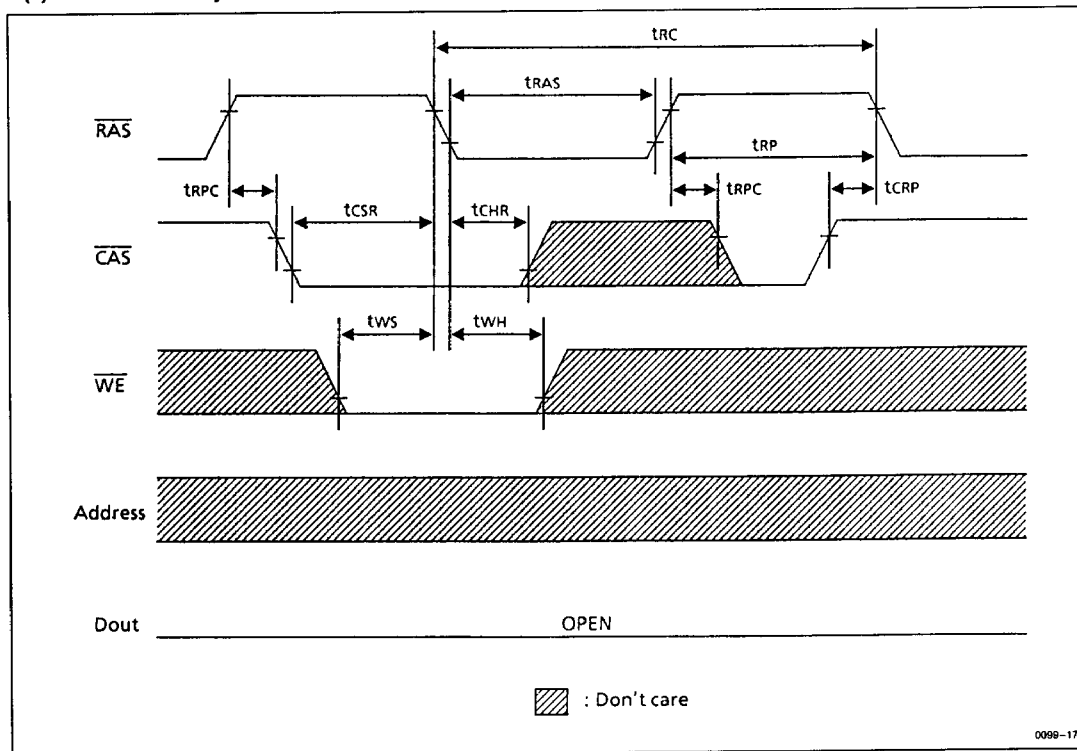
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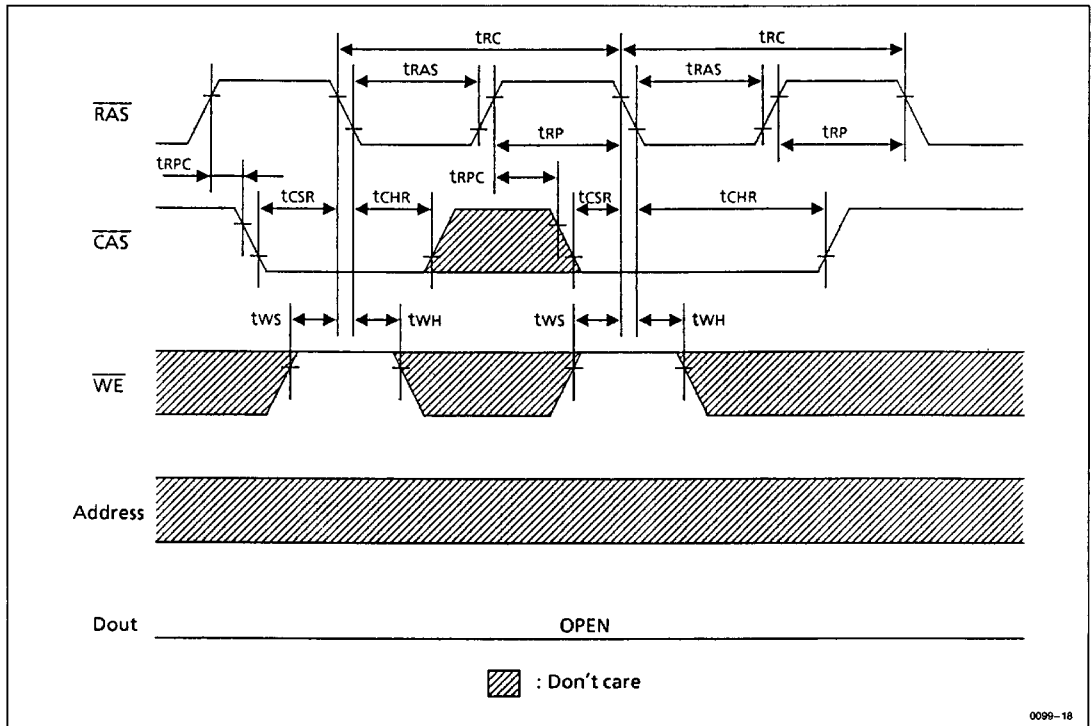
• TEST MODE CYCLE



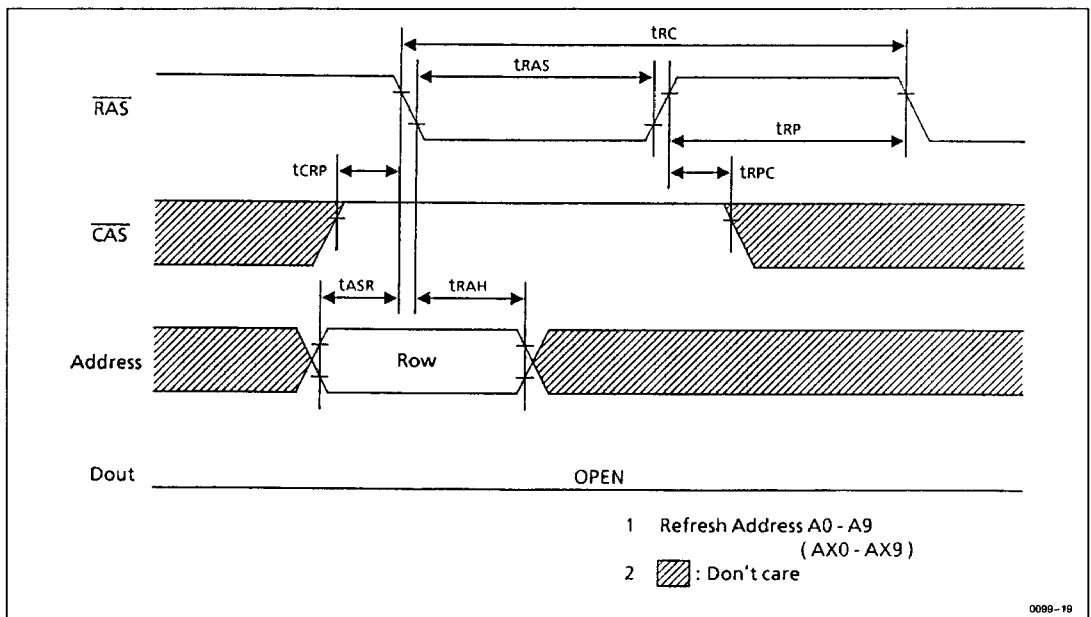
• (1) Test Mode Set Cycle



• (2) Test Mode Reset Cycle
CAS Before RAS Refresh Cycle



RAS Only Refresh Cycle

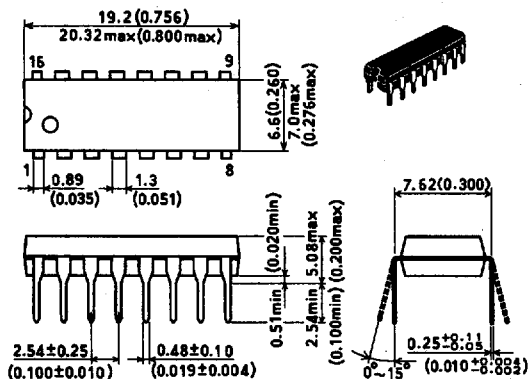


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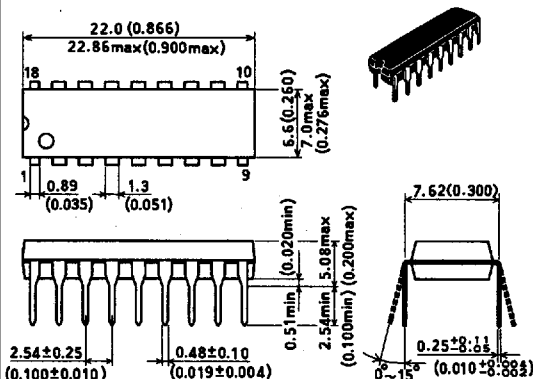
Unit: mm (inch) Scale 3/2

• Dual-in-line Plastic

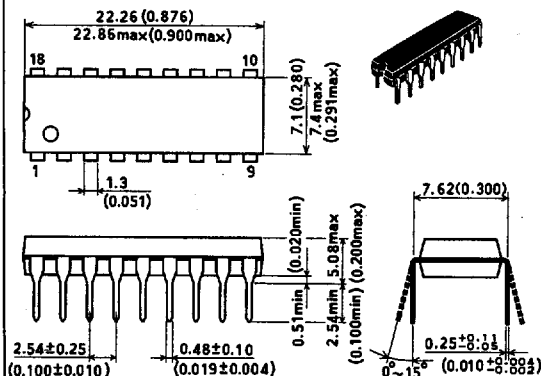
• DP-16B



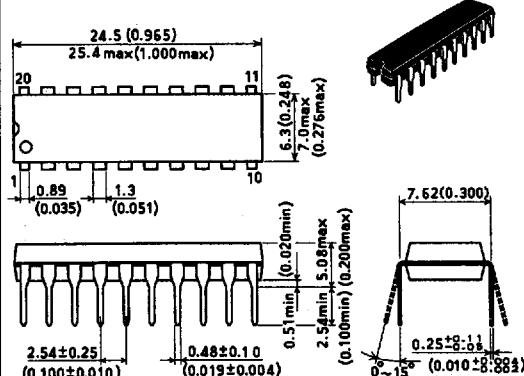
• DP-18B



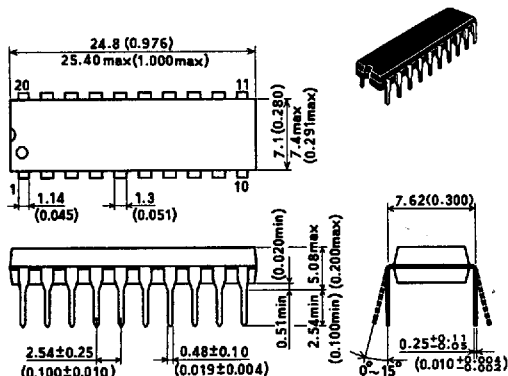
• DP-18C



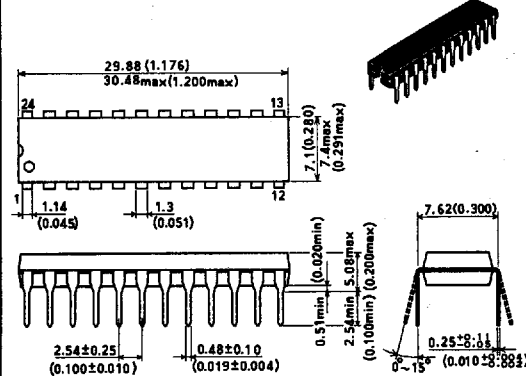
• DP-20N



• DP-20NA



• DP-20NC

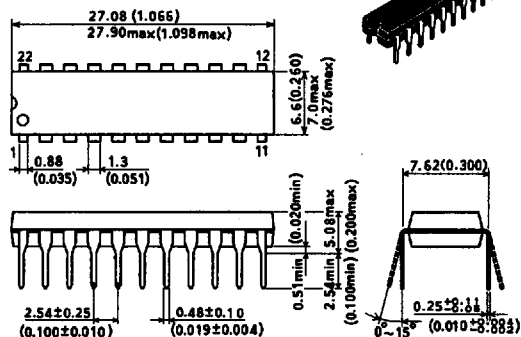


• Dual-In-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

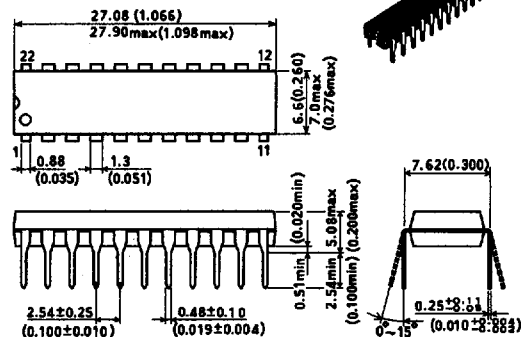
Unit: mm (inch) Scale 3/2

• DP-22N

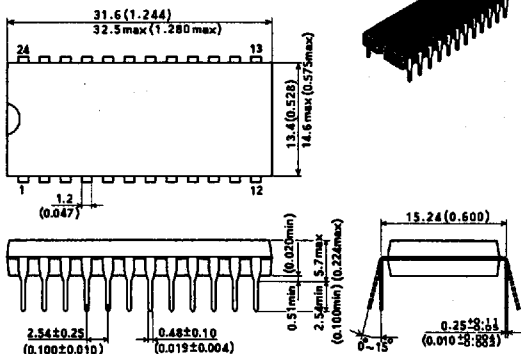


• DP-22NB

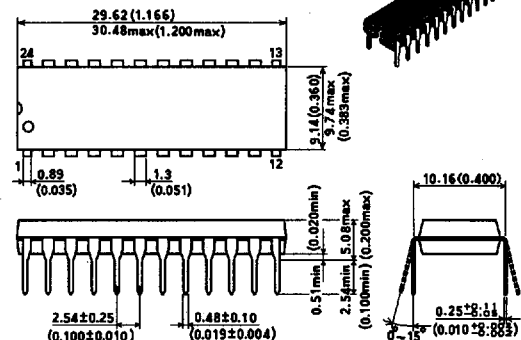
T-90-20



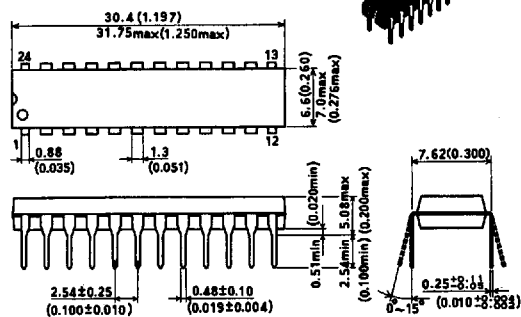
• DP-24



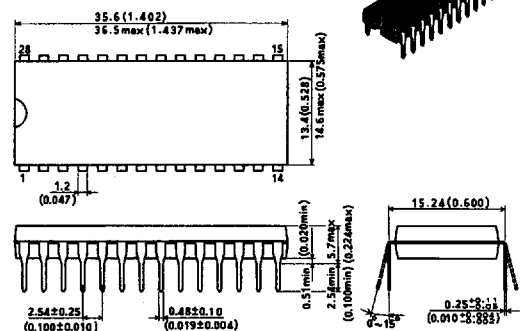
• DP-24A



• DP-24N



• DP-28

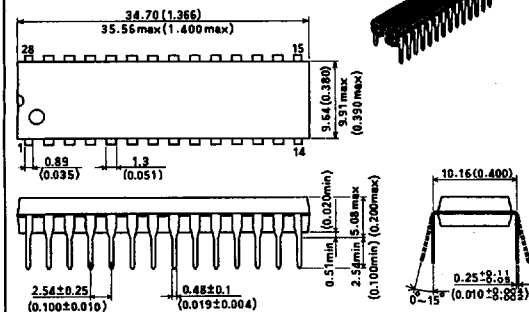


• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

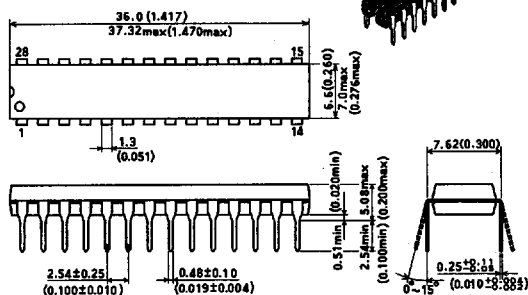
Unit: mm (inch) Scale 3/2

• DP-28C

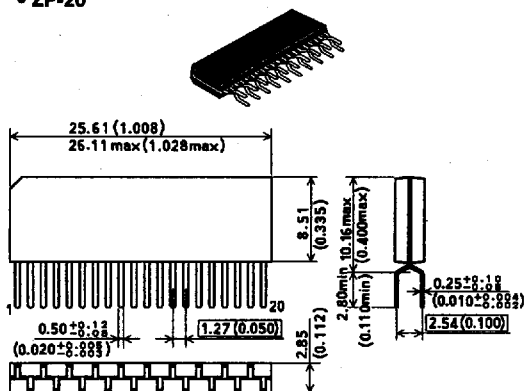


• DP-28N

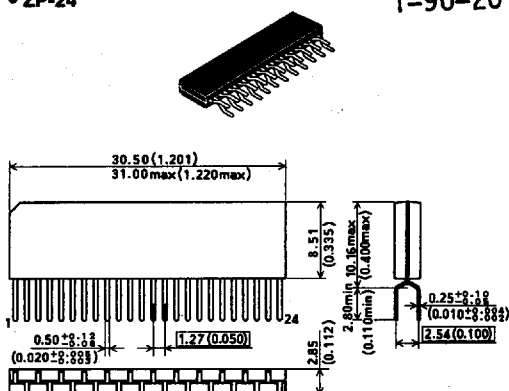
T-90-20



• ZP-20

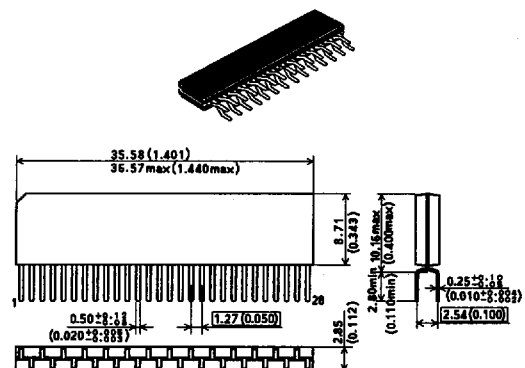


• ZP-24

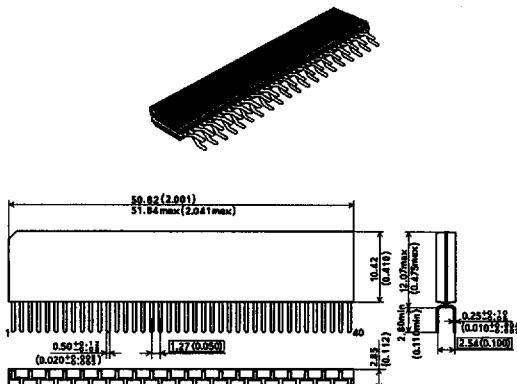


T-90-20

• ZP-28



• ZP-40



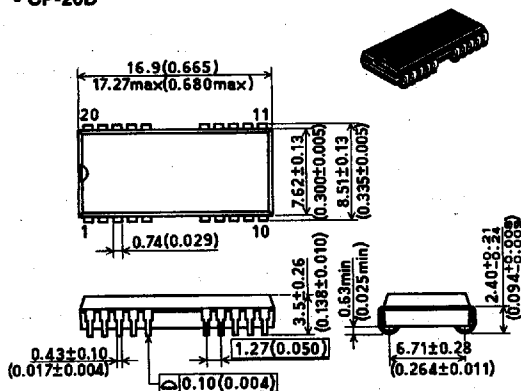
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

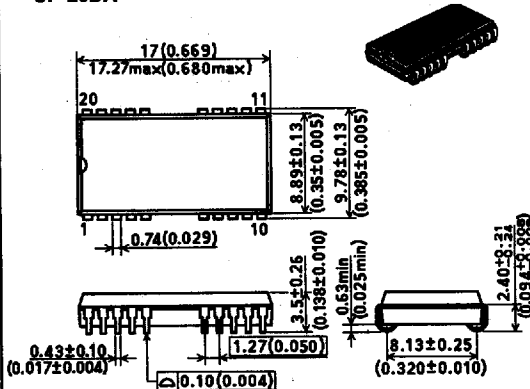
Unit: mm (inch) Scale 3/2

T-90-20

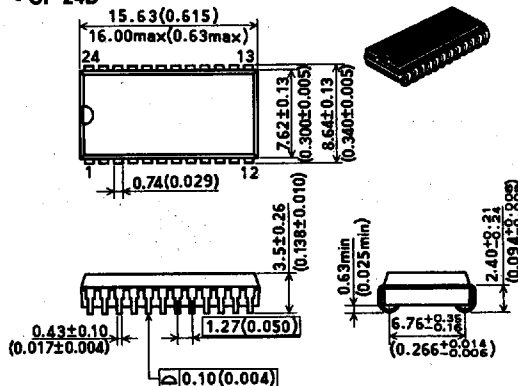
• CP-20D



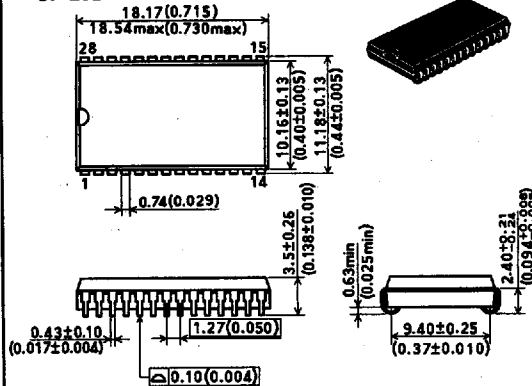
• CP-20DA



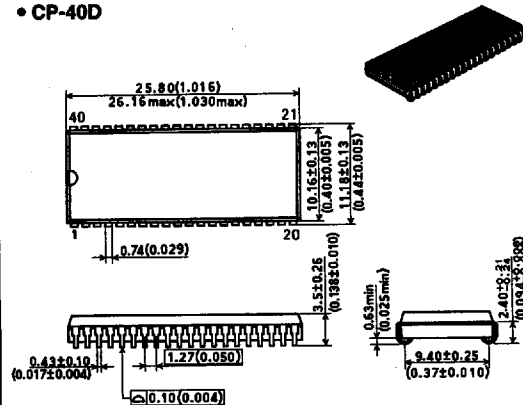
• CP-24D



• CP-28D



• CP-40D

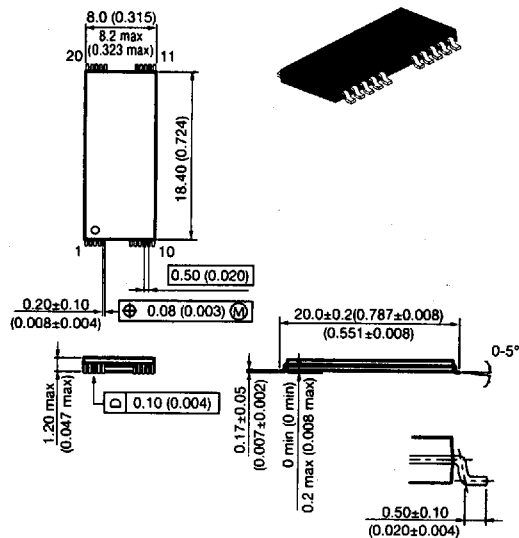


• TSOP (Thin Small Outline Package)

HITACHI/ LOGIC/ARRAYS/MEM

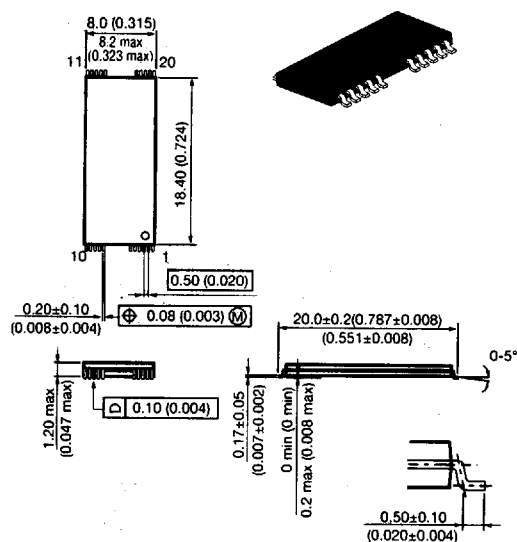
Unit: mm (inch) Scale 3/2

• TFP-20DA

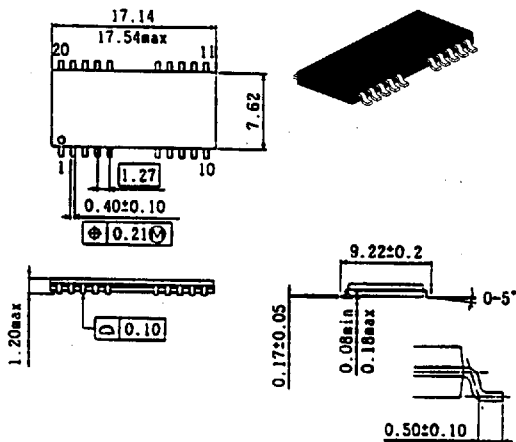


• TFP-20DAR

T-90-20



• TTP-20D



• TTP-20DR

