Am7948

Subscriber Line Interface Circuit

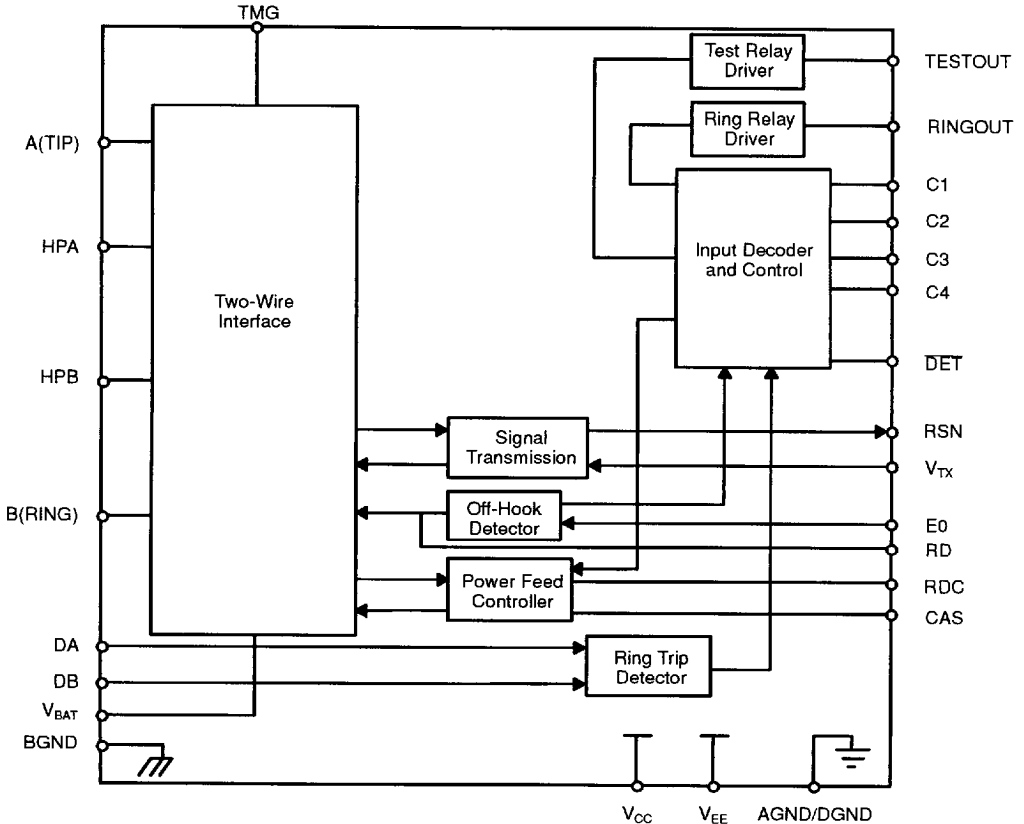**Advanced
Micro
Devices**

DISTINCTIVE CHARACTERISTICS

- Ideal for Long Loop applications
- Low standby power (45 mW)
- −40-V to −58-V battery operation
- On-hook transmission
- Tip open state for ground start lines
- Two-wire impedance set by single external impedance
- Programmable constant current feed
- Programmable loop detect threshold
- Current gain = 200
- Polarity reversal option available
- On-chip thermal management (TMG)
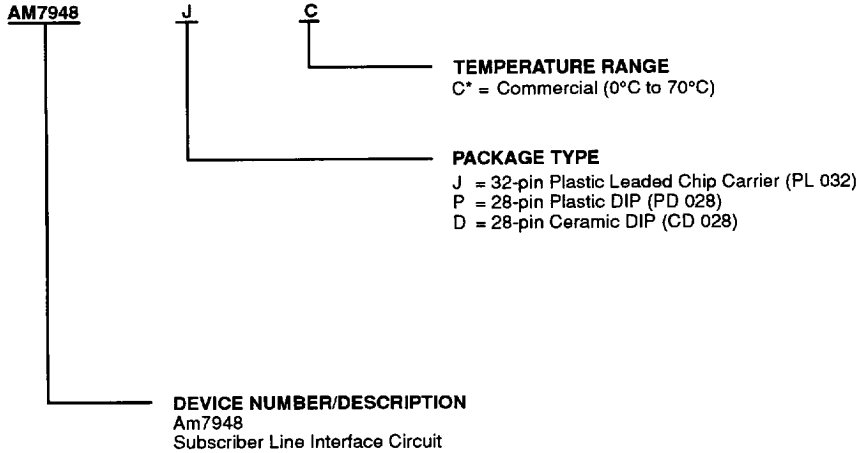- On-chip ring and test relay driver and relay snubber circuits

BLOCK DIAGRAM

This document contains information on a product under development at Advanced Micro Devices Inc The information is intended to help you evaluate this product AMD reserves the right to change or discontinue work on this proposed product without notice

1-125

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ORDERING INFORMATION

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

AM7948   J   C

TEMPERATURE RANGE
C* = Commercial (0°C to 70°C)

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)
P = 28-pin Plastic DIP (PD 028)
D = 28-pin Ceramic DIP (CD 028)

DEVICE NUMBER/DESCRIPTION
Am7948
Subscriber Line Interface Circuit

Valid Combinations	
AM7948	JC
	PC
	DC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.
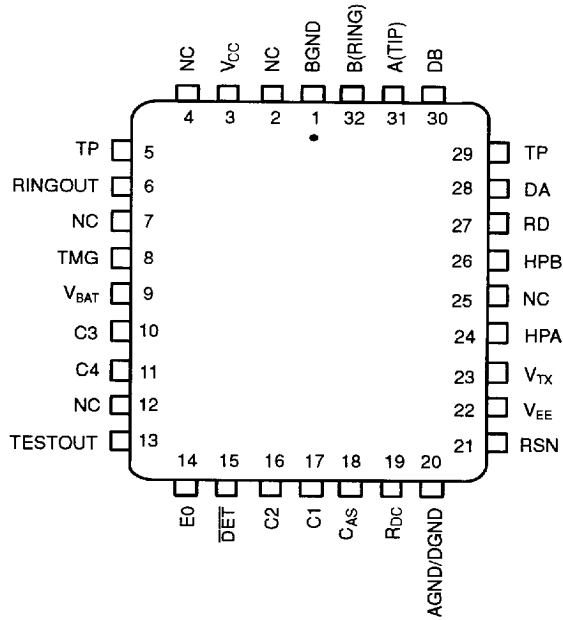
Note:

* Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

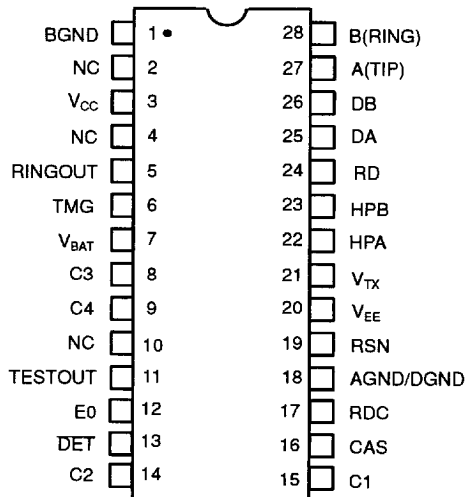0257527 0035419 558

CONNECTION DIAGRAMS
Top View

32-Pin PLCC

28-Pin Plastic or Ceramic DIP

Notes:

1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate.
3. NC = No Connect

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PIN DESCRIPTION

AGND/DGND
Ground

Analog and Digital ground.

A(TIP)
(Output)

Output of A(TIP) power amplifier.

BGND
Ground

Battery (power) ground.

B(RING)
(Output)

Output of B(RING) power amplifier.

CAS
Capacitor for Anti-Saturation

Pin for capacitor to filter reference voltage when operating in Anti-Saturation region.

C4–C1
Decoder (Inputs)

SLIC control pins. C4 is MSB and C1 is LSB.
TTL compatible.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

DET
Switch Hook Detector (Output)

When enabled, a logic LOW indicates that selected condition is detected. The detect condition is selected by the logic inputs (C1, C2, C3, and E0). The output is open-collector with a built in 15 kΩ pull-up resistor.

E0
Detect Enable (Input)

A logic high enables $\overline{DET}$. A logic low disables $\overline{DET}$.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

NC
No Connect

Pin not internally connected.

RD
Detect Resistor Pin

Detector threshold set and filter pin.

RDC
DC Feed Resistor Pin

Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

RSN
Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.

TESTOUT
Test Relay Driver (Output)

Open collector driver with emitter internally connected to AGND.

TMG
Thermal Management

External resistor connects between this pin and V_{BAT} to offload power dissipation from SLIC. Functions during normal polarity and reverse polarity states.

TP
Thermal Pin

Thermal pin for connection to pad for heat dissipation. Thermally connected to substrate.

V$_{BAT}$

Battery supply and connection to substrate.

V$_{CC}$

+5-V power supply.

V$_{EE}$

–5-V power supply.

V$_{TX}$
Transmit Audio (Output)

This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. V_{TX} also sources the two-wire input impedance programming network.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −55°C to +150°C

V_{CC} with respect to AGND/DGND ...... 0.4 V to +7 V

V_{EE} with respect to AGND/DGND ...... 0.4 V to −7 V

V_{BAT} with respect to AGND/DGND:

    Continuous .... +0.4 V to −70 V

    10 ms .... +0.4 V to −75 V

BGND with respect to
AGND/DGND .... +3 V to −3 V

A(TIP) or B(RING) to BGND:

    Continuous .... −70 V to +1 V

    10 ms (F = 0.1 Hz) .... −70 V to +5 V

    1 μs (F = 0.1 Hz) .... −80 V to +8 V

    250 ns (F = 0.1 Hz) .... −90 V to +12 V

Current from A(TIP) or B(RING) .... ±150 mA

RINGOUT/TESTOUT Current .... 75 mA

RINGOUT/TESTOUT voltage .... BGND to +7 V

RINGOUT/TESTOUT transient ...... BGND to +10 V

DA and DB inputs

    Voltage on ring trip inputs .... V_{BAT} to 0 V

    Current into ring trip inputs .... ±10 mA

C4–C1, E0

    Input voltage .... −0.4 V to V_{CC} +0.4 V

Maximum Power Dissipation, Continuous,
T_A = 70°C, No heat sink (see note):

    In 32-pin PLCC package .... 1.7 W

    In 28-pin ceramic DIP package .... 2.5 W

    In 28-pin plastic DIP package .... 1.4 W

Thermal Data: .... θ_{JA}

    In 32-pin PLCC package .... 43°C/W typical

    In 28-pin ceramic DIP package ... 30°C/W typical

    In 28-pin plastic DIP package .... 53°C/W typical

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165° C. The device should never be exposed to this temperature. Operation above 145° C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature .... 0°C to +70°C*

V_{CC} .... 4.75 V to 5.25 V

V_{EE} .... −4.75 V to −5.25 V

V_{BAT} .... −40 V to −58 V

AGND/DGND .... 0 V

BGND with respect to
AGND/DGND .... −100 mV to +100 mV

Load resistance on V_{TX} to ground .... 10 kΩ minimum

Notes:

Operating Ranges define those limits between which the functionality of the device is guaranteed.

*Specifications in this data sheet are guaranteed by testing from 0° C to +70° C. Performance from −40°C to +85°C is guaranteed by characterization and periodic sampling of production units. Steady state operation at T_A = 70° C is guaranteed by testing at 90° C and guard banding.

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ELECTRICAL CHARACTERISTICS (See Note 1)

Description	Test Conditions	Advance Information			Unit	Note
		Min	Typ	Max		
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz	26			dB	1, 4, 7
Analog output (V_{TX}) impedance			3	20	Ω	4
Analog (V_{TX}) output offset voltage	0°C to +70°C −40°C to +85°C	−35 −40		+35 +40	mV mV	4
Overload level, 2-wire and 4-wire	Active state	2.5			Vpk	2a
Overload level	On-hook, $R_{LAC} = 900\ \Omega$	1.18			Vrms	2b
THD, Total Harmonic Distortion	0 dBm 0 dBm, $R_{LDC} = 2030\ \Omega$, BAT $= -42.5$ V +7 dBm		−64 −45 −55	−50 −40	dB dB dB	5 5
THD, on-hook	+1 dBm, $R_{LAC} = 900\ \Omega$			−36	dB	5
Longitudinal Capability (See Test Circuit D)						
Longitudinal to Metallic L-T, L-4	200 Hz to 1 kHz normal polarity 200 Hz to 1 kHz reverse polarity 200 Hz to 1 kHz −40°C to +85°C	63 58 58	70		dB dB dB	 4
	1 kHz to 3.4 kHz 1 kHz to 3.4 kHz −40°C to +85°C	58 54			dB dB	 4
Longitudinal signal generation 4-L	200 Hz to 800 Hz normal polarity	40			dB	
Longitudinal current per pin	Active state Stand-by state	8.5 8.5	27 27		mArms mArms	
Longitudinal impedance at A or B	0 to 100 Hz		25	35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	$R_L = 600\ \Omega$ +25°C to +85°C $R_L = 600\ \Omega$ −40°C to +25°C		+7	+10 +12	dBrnC dBrnC	4
Psophometric weighted noise	$R_L = 600\ \Omega$ +25°C to +85°C $R_L = 600\ \Omega$ −40°C to +25°C		−83	−80 −78	dBmp dBmp	
Insertion Loss (2-Wire to 4-Wire and 4-Wire to 2-Wire, See Test Circuits A and B)						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C 0 dBm, 1 kHz −40°C to +85°C On-hook, OHT mode	−0.15 −0.20 −0.35		+0.15 +0.20 +0.35	dB dB dB	 4 4
Gain accuracy over frequency relative to 1 kHz	300 to 3400 Hz 0°C to +70°C 300 to 3400 Hz −40°C to +85°C	−0.10 −0.15		+0.10 +0.15	dB dB	5 4
Gain tracking relative to 0 dBm	+3 dBm to −55 dBm 0°C to +70°C +3 dBm to −55 dBm −40°C to +85°C +3 dBm, BAT = 42.5 V, $R_{LDC} = 2030\ \Omega$ On-hook	−0.10 −0.15 −0.30 −0.35		+0.10 +0.15 +0.30 +0.35	dB dB dB dB	 4
Balance Return Signal (4-Wire to 4-Wire)						
Gain accuracy	Ref: 0 dBm, 1 kHz 0°C to +70°C Ref: 0 dBm, 1 kHz −40°C to +85°C	−0.15 −0.20		+0.15 +0.20	dB dB	3 4
Gain accuracy over frequency	300 Hz to 3400 Hz 0°C to +70°C 300 Hz to 3400 Hz −40°C to +85°C	−0.10 −0.15		+0.10 +0.15	dB dB	3 4
Gain tracking relative to 0 dBm	+3 dBm to −55 dBm 0°C to +70°C +3 dBm to −55 dBm −40°C to +85°C	−0.10 −0.15		+0.10 +0.15	dB dB	 4
Group delay	0 dBm, 1 kHz		4		μs	4, 7

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ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Advance Information Min	Advance Information Typ	Advance Information Max	Unit	Note
Line Characteristics						
I_L, Short loops, active or OHT	$R_{LDC} = 600\ \Omega$	20	22	24	mA	
I_L, Long loops, active	$R_{LDC} = 2030\ \Omega$, BAT = −42.5 V, $T_A = 25°C$	18	18.6		mA	
I_L, Accuracy, standby	$I_L = \dfrac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 1800}$ $T_A = 25°C$	$0.7 I_L$	I_L	$1.3 I_L$	mA	
I_L, Loop current, tip open mode	$R_L = 0$ B to GND B to $V_{BAT} + 6$ V		0 30 30	100	μA mA mA	
I_L, Loop current, open circuit mode	$R_L = 0$			100	μA	
I_LLIM	Active, A and B to GND		70	100	mA	
VA, Active, ground start signalling	A to −48 V = 7 kΩ, B to GND = 100 Ω	−7.5	−5			4
VAB, Open circuit voltage	BAT = −52 V	−42.75	−45.7		V	
Power Supply Rejection Ratio (Vripple = 100 mVrms), Active Normal Mode						
V_{CC}	50 Hz to 3400 Hz	30	40		dB	5
V_{EE}	50 Hz to 3400 Hz	28	35		dB	5
V_{BAT}	50 Hz to 3400 Hz	28	50		dB	5
Effective internal resistance	CAS pin to GND	85	170	255	kΩ	4
Power Dissipation						
On-hook, open circuit			25	70	mW	
On-hook, standby mode			45	85	mW	
On-hook, OHT mode			120	180	mW	
On-hook, active mode	R_{TMG} = open $R_{TMG} = 2500\ \Omega$		180 195	270 300	mW mW	4
Off-hook, standby mode	$R_L = 600\ \Omega$		860	1100	mW	
Off-hook, OHT mode	$R_L = 300\ \Omega$, R_{TMG} = open		1000	1300	mW	
Off-hook, active mode	$R_L = 300\ \Omega$, $R_{TMG} = 2500\ \Omega$		450	800	mW	
Supply Currents, Battery = −58 V						
I_{CC}, On-hook V_{CC} supply current	Open Circuit Mode OHT Mode Standby Mode Active Mode, BAT = −48 V		1.7 4.9 2.2 6.3	2.5 7.5 3.0 8.5	mA mA mA mA	
I_{EE}, On-hook V_{EE} supply current	Open Circuit Mode OHT Mode Standby Mode Active Mode, BAT = −48 V		0.7 2.0 0.77 2.1	2.0 3.5 2.0 5.0	mA mA mA mA	
I_{BAT}, On-hook V_{BAT} supply current	Open Circuit Mode OHT Mode Standby Mode Active Mode, BAT = −48 V		0.18 1.9 0.45 4.2	1.0 4.7 1.5 5.7	mA mA mA mA	
RFI Rejection						
RFI rejection	100 kHz to 30 MHz, (See Figure F)			1.0	mVrms	4

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ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Advance Information			Unit	Note
		Min	Typ	Max		
Logic Inputs (C1, C2, C3, C4, E0)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8	V	
I_{IH}, Input High current		−75		40	μA	
I_{IL}, Input Low current	C1, C2, C3, C4, E0	−400			μA	
Logic Output (DET)						
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = −0.1 mA, 15 kΩ to V_{CC}	2.4			V	
Ring Trip Detector Input (DA, DB)						
Bias current		−500	−50		nA	
Offset voltage	Source resistance = 2 MΩ	−50	0	+50	mV	6
Loop Detector						
I_T, Loop detect threshold tolerance	R_D = 35.4 kΩ, active R_D = 35.4 kΩ, idle R_D = 35.4 kΩ, tip open	330/R_D 330/R_D 330/R_D	375/R_D 375/R_D 375/R_D	420/R_D 420/R_D 420/R_D	A A A	

Table 1. SLIC Decoding

State	C3	C2	C1	Two-Wire Status	DET Output
0	0	0	0	Open circuit	Ring trip
1	0	0	1	Ringing	Ring trip
2	0	1	0	Active	Loop det.
3	0	1	1	On-hook TX (OHT)	Loop det.
4	1	0	0	Tip open	Loop det.
5	1	0	1	Standby	Loop det.
6	1	1	0	Active polarity reversal	Loop det.
7	1	1	1	OHT polarity reversal	Loop det.

Note:
C4 logic high enables the Testout relay driver.

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SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Note
tshdd	E0 Low to DET Low	Switch hook detect (See Figure E)			1.1	μs	
tshd0	E0 High to DET High				3.8		

SWITCHING WAVEFORMS

E0 to DET
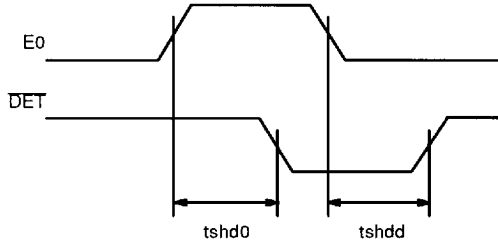
Note:
All delays measured at 1.4-V level.

RELAY DRIVER SPECIFICATIONS
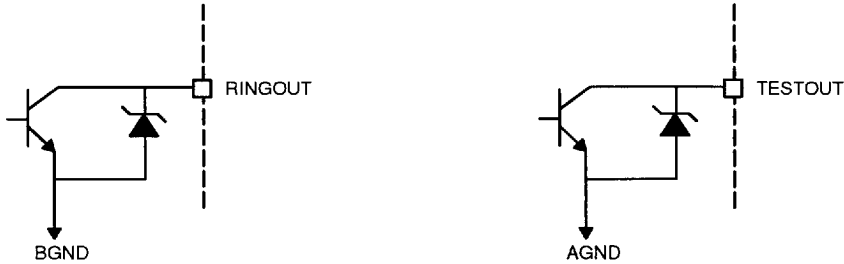
Description	Test Conditions	Min	Typ	Max	Unit	Note
Relay Driver Output (RINGOUT) (−40 °C to +85°C)						
On voltage	I_{OL} = 35 mA		+0.3	+0.5	V	
Off leakage	V_{OH} = +5 V			100	μA	
Zener break over	I_Z = 100 μA	6	7.2		V	
Zener ON voltage	I_Z = 30 mA		10		V	
Test Driver Output (TESTOUT) (−40 °C to +85°C)						
On voltage	I_{OL} = 35 mA		+0.4	+0.75	V	
Off leakage	V_{OH} = +5 V			100	μA	
Zener break over	I_Z = 100 μA	6	7.2		V	
Zener ON voltage	I_Z = 30 mA		10		V	

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Notes:

1. *Unless otherwise noted, test conditions are: BAT = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 11.36 kΩ, R_D = 35.4 kΩ, R_{TMG} = 2500 Ω, No fuse resistors, C_{HP} = 0.2 μF, C_{DC} = 0.1 μF, CCAS = 0.1 μF, D_f = 1N400x, two-wire AC input impedance is a 900 Ω resistance synthesized by the programming network shown below.*
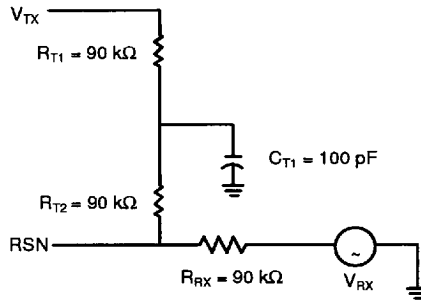

2. a. *Overload level is defined when THD = 1%.*

   b. *Overload level is defined when THD = 1.5%.*

3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes that the two-wire AC load impedance matches the programmed impedance.*

4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*

5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

6. *Tested with 0 Ω source impedance. 2 MΩ specified for system design only.*

7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network will reduce the group delay to less than 2 μs and increase 2WRL. The effect of group delay on linecard performance may also be compensated for by synthesizing complex impedance with the AMD SLAC or DSLAC device.*

Table 2. User-Programmable Components

$Z_T = 200 \, (Z_{2W1N} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F and Z_{2W1N} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \dfrac{Z_L}{G_{42L}} \bullet \dfrac{200 \bullet Z_T}{Z_T + 200 \, (Z_L + 2 \bullet R_F)}$	Z_{RX} is connected from V_{RX} to RSN. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \dfrac{500}{I_{LOOP}}$ $C_{DC} = 1.5\text{ms} \bullet \dfrac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant current region.
$R_D = \dfrac{375}{I_T}, \quad C_D = \dfrac{0.5 \text{ ms}}{R_D}$	R_D and C_D form the network connected from RD to -5 V and I_T is the threshold current between on-hook and off-hook.
$C_{CAS} = \dfrac{1}{3.4 \bullet 10^5 \pi F_c}$	C_{CAS} is the regulator filter capacitor and F_c is the desired filter cut-off frequency.
$I_{OHT} = \dfrac{500}{R_{DC1} + R_{DC2}}$	OHT Loop current (constant current region).
Thermal Management Equations (Normal Active and Tip Open States)	
$RMG \geq \; = \dfrac{V_{BAT} - 6 \text{ V}}{I_{LOOP}}$	R_{TMG} is connected from TMG to V_{BAT} and is used to limit power dissipation within the SLIC in active and tip open modes only.
$P_{RMG} = \dfrac{(V_{BAT} - 6 \text{ V} - (I_L \bullet R_L))^2}{RMG}$	Power dissipated in the thermal management resistor, R_{TMG}, during active and tip open states.
$P_{SLIC} = V_{BAT} \bullet I_L - P_{RMG} - R_L (I_L)^2 + 0 \, 12 \text{ W}$	Power dissipated in the SLIC while in active and tip open states.

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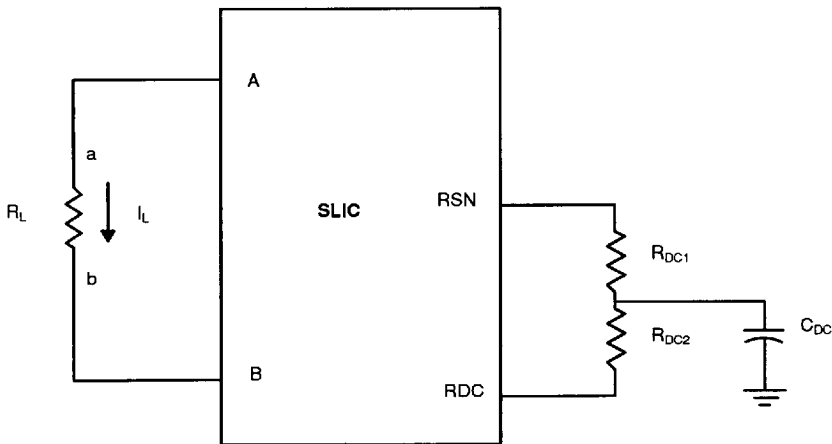
$R_{DC} = R_{DC1} + R_{DC2} = 22.72\ k\Omega$
$BAT = -48\ V$
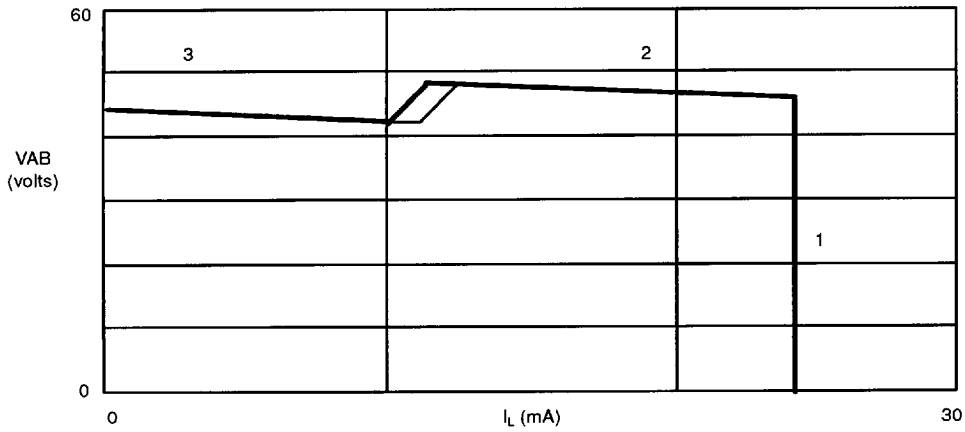
Notes:

1. $V_{AB} = I_L R_L' = \dfrac{500}{R_{DC}}\ R_L',\ \ where\ R_L' = R_L + 2\ R_F$

2. $V_{AB} = 0.925\ (V_{BAT}) + 0.9 - I_L\ \dfrac{R_{DC}}{120}$

3. $V_{AB} = 0.925\ (V_{BAT}) - 1.83 - I_L\ \dfrac{R_{DC}}{120}$
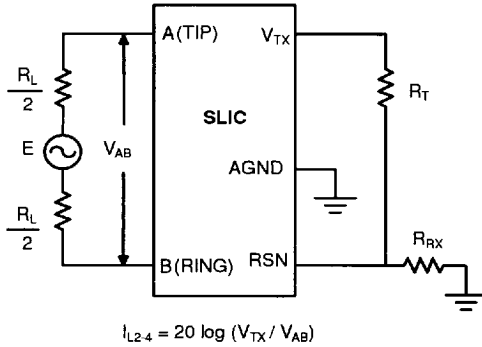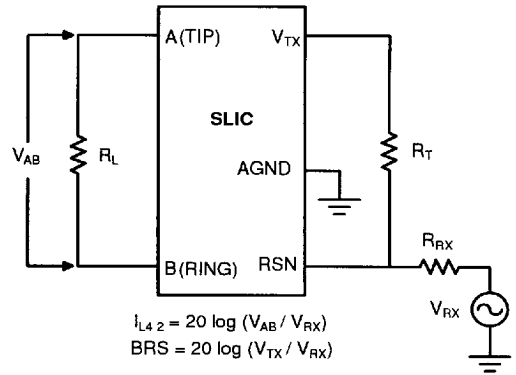
Figure 1. Load Line (Typical)

Note:
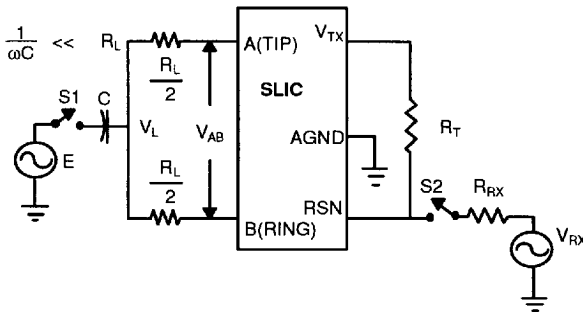*Feed current programmed by R_{DC1} and R_{DC2}.*

Figure 2. Feed Programming

TEST CIRCUITS

$$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$$

A. Two-to-Four-Wire Insertion Loss

$$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$$
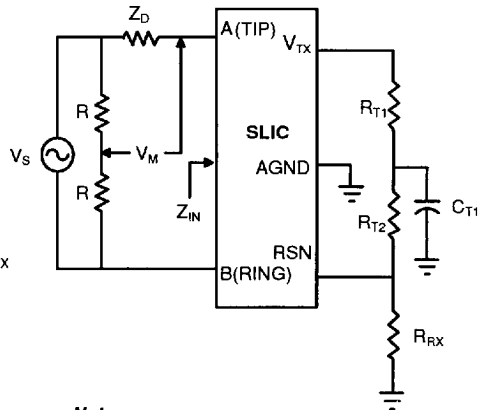$$BRS = 20 \log (V_{TX} / V_{RX})$$

B. Four-to-Two-Wire Insertion Loss and Balance Return Signal

S2 Open, S1 Closed
L-T Long. Bal. = 20 log (V_{AB} / E)
L-T Long. Rej. = 20 log (V_{TX} / E)

S2 Closed, S1 Open
4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance (IEEE 455-1984)
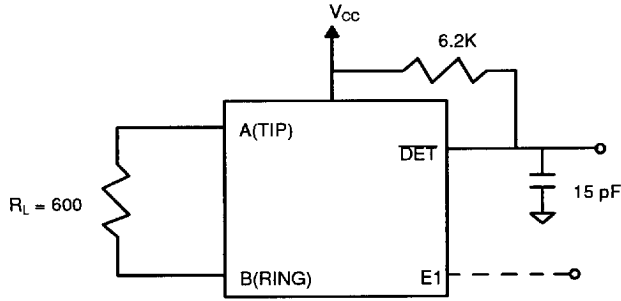

Note:

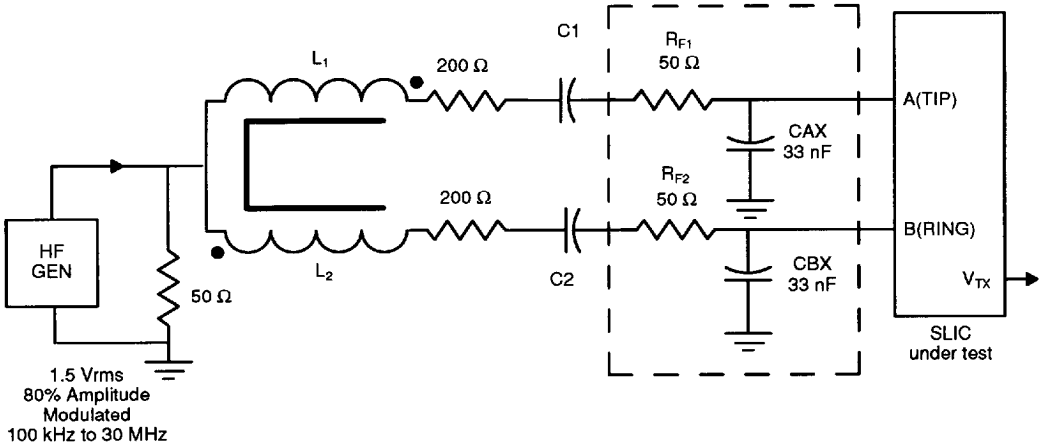*Z_D is the desired impedance (e.g., the charac-teristic impedance of the line).*

$$R_L = -20 \log (2 V_M / V_S)$$

D. Two-Wire Return Loss Test Circuit

◼ ⬚ 0257527 0035430 119 ◼◼
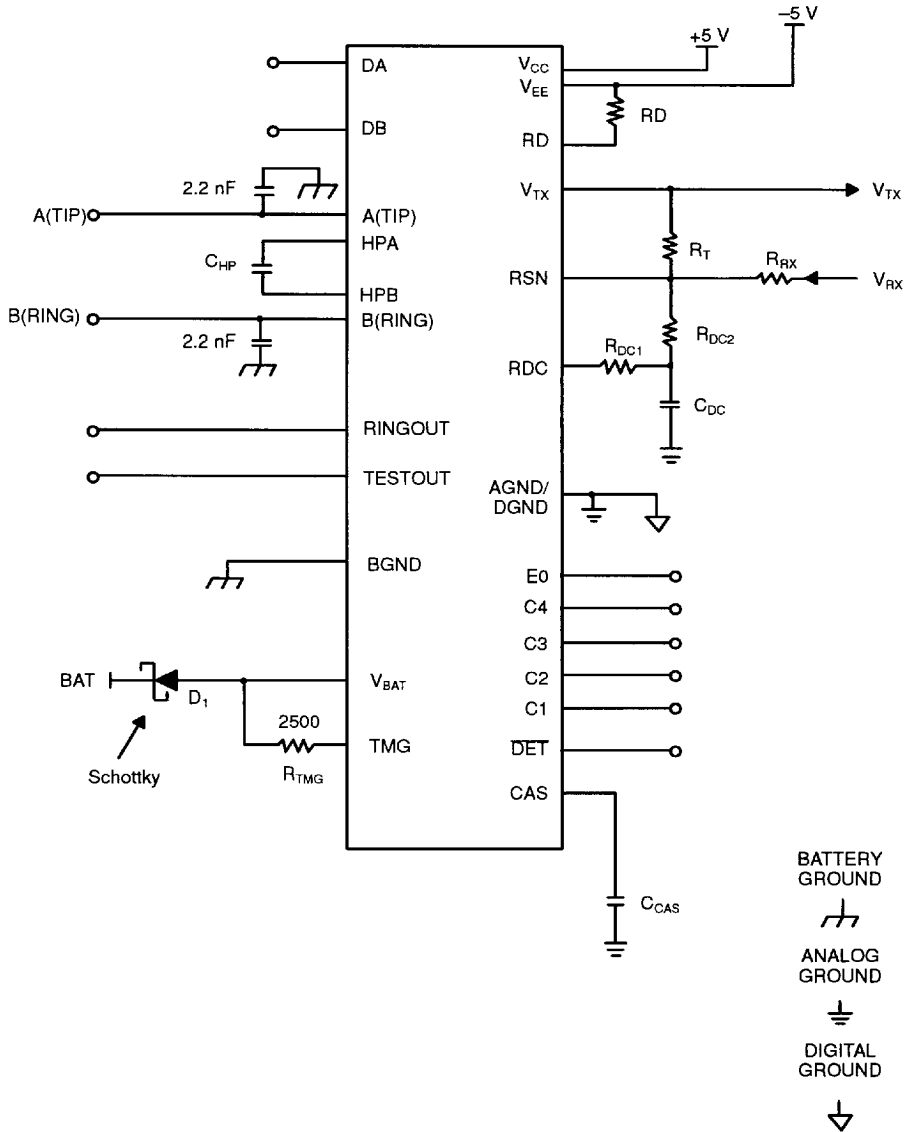
TEST CIRCUITS (continued)

V$_{CC}$

6.2K

A(TIP)

DET

R$_L$ = 600

15 pF

B(RING)   E1

E. Loop Detector Switching

C1

L$_1$

200 Ω

R$_{F1}$
50 Ω

A(TIP)

CAX
33 nF

R$_{F2}$
50 Ω

200 Ω

B(RING)

HF
GEN

50 Ω

L$_2$

C2

CBX
33 nF

V$_{TX}$

SLIC
under test

1.5 Vrms
80% Amplitude
Modulated
100 kHz to 30 MHz

F. RFI Test Circuit

0257527 0035431 055

TEST CIRCUITS (continued)

G. Am7948 Test Circuit

0257527 0035432 T91