Am29C509

12 x 12-Bit CMOS Multiplier/Accumulator

DISTINCTIVE CHARACTERISTICS

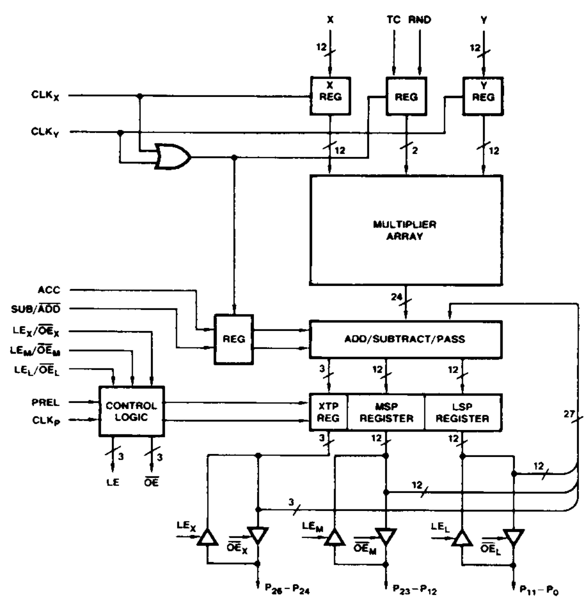
- **High-speed 1.6-μs CMOS Process**
  - 50-ns maximum clock rate supports real-time processing.
- **27-Bit Product Accumulation Result**
  - Provides 24-bit product plus 3-bit extended product.
- **Accumulator Function**
  - Supports LOAD, ADD, and SUBTRACT instructions.
- **Output Register Preload**
  - A predetermined value can be loaded into the output register.
- **Round Control**
  - The most significant 12 bits of the product can be rounded to the value nearest to the full 24-bit product.
- **Accepts Two's-Complement or Unsigned Inputs**

GENERAL DESCRIPTION

The Am29C509 is a high-speed 12 x 12-bit CMOS multiplier/accumulator (MAC). The X and Y input registers accept 12-bit inputs in two's-complement or unsigned magnitude format. A third register stores the Two's Complement (TC), Round (RND), Accumulate (ACC), and Subtraction (SUB/$\overline{\text{ADD}}$) control bits. This register is clocked whenever the X or input registers are clocked.

The 27-bit accumulator/output register contains the full 24-bit multiplier output which is sign-extended or zero-filled based on the TC control bit. The accumulator can also be preloaded from an external source through the bidirectional P-port. The operation of the accumulator is controlled by the signals ACC, SUB/$\overline{\text{ADD}}$, and PREL (Preload). Each of the input registers and the output register have independent clocks.

BLOCK DIAGRAM



BD002831

Publication # 04986 Rev. E Amendment /0

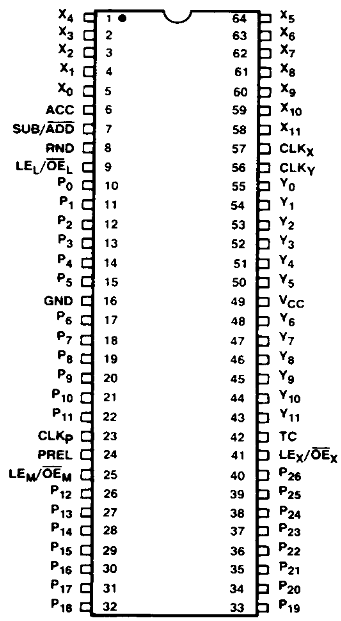
RELATED AMD PRODUCTS

Part No.	Description
Am25S557/558	8 x 8 Multiplier
Am29C01	CMOS 4-Bit Microprocessor Slice
Am29C03	CMOS 4-Bit Super Slice
Am2904	Status and Shift Controller
Am29C10A	CMOS Microprogram Controller
Am29C101	16-Bit CMOS Microprocessor Slice
Am29C111	CMOS 16-Bit Microsequencer
Am29C116	CMOS 16-Bit Microprocessor
Am29PL131	64 x 12-Bit Field-Programmable Controller
Am29PL142	128 x 16-Bit Field Programmable Controller
Am2914	Vectored Interrupt Controller
Am2925	Clock Generator
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am29C334	CMOS 64 x 16 Register File
Am2940	DMA Address Generator
Am29C516A/517A	CMOS 16 x 16 Parallel Multipliers
Am2952A	8-Bit Bidirectional I/O Port
Am29C520	CMOS 4-Deep Pipeline Register
Am29C525	CMOS 16-Deep Pipeline Register
Am29800A	High-Performance Bus Interface Family
Am29C800	High-Performance CMOS Bus Interface Family
Am29818A	SSR™ Diagnostics/Pipeline Register

SSR is a trademark of Advanced Micro Devices, Inc.

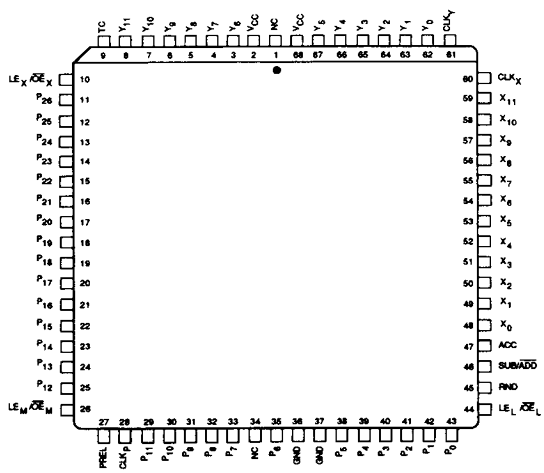
CONNECTION DIAGRAMS
Top View

DIPs



CDR04451

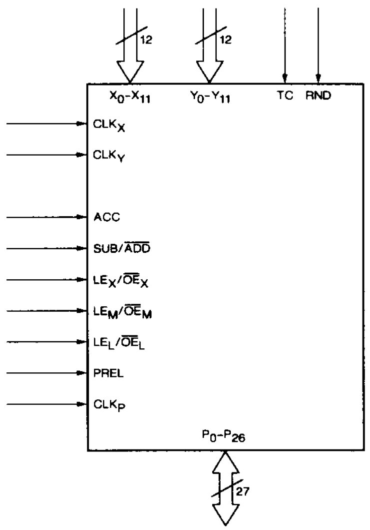
PLCC



CD011201

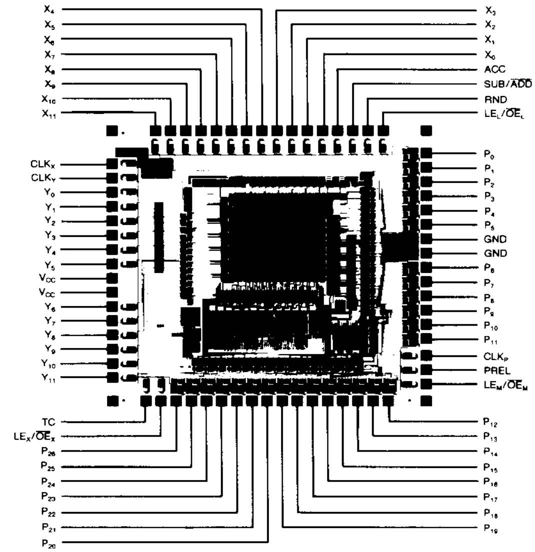
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002720

METALLIZATION AND PAD LAYOUT



Die Size: 199 x 210
Total Transistor Count: 12300

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C509 -1 P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 64-Pin Plastic DIP (PD 064)
D = 64-Pin Topbrazed Ceramic DIP w/o Heatsink (TDX064)
J = 68-Pin Plastic Leaded Chip Carrier (PL 068)

b. SPEED OPTION
−1 = 55 ns
−2 = 40 ns*

a. DEVICE NUMBER/DESCRIPTION
Am29C509
12 x 12-Bit CMOS Multiplier/Accumulator

Valid Combinations	
AM29C509	PC, PCB, DC, DCB, JC
AM29C509-1	PC, DC, JC
AM29C509-2	

* Advance Information

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C509 -1 /B X C

e. LEAD FINISH
C = Gold

d. PACKAGE TYPE
X = 64-Pin Topbrazed Ceramic DIP without Heatsink (TDX064)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
-1 = 60 ns

a. DEVICE NUMBER/DESCRIPTION
Am29C509
12 x 12-Bit CMOS Multiplier/Accumulator

Valid Combinations	
AM29C509	/BXC
AM29C509-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

ACC Accumulate (Input, Active HIGH)
When HIGH, the multiplier product is accumulated in the accumulator. When LOW, the multiplier product is written into the accumulator (see Table 2). The ACC control is loaded on the rising edge of CLK_X or CLK_Y.

CLK_P Clock (Input)
Loads data into the XTP, MSP, and LSP registers on the rising edge.

CLK_X, CLK_Y Clocks (Input)
Load X and Y data respectively and TC, RND, ACC, and $SUB/\overline{ADD}$ on the rising edge.

$LE_L/\overline{OE_L}$ Load Enable Least/$\overline{\text{Output Enable Least}}$ (Input)
Active-HIGH Load Enable for the LSP-port during preloading. Active-LOW three-state control for the LSP-port during normal operation (see Table 1). (TSL*)

$LE_M/\overline{OE_M}$ Load Enable Most/$\overline{\text{Output Enable Most}}$ (Input)
Active-HIGH Load Enable for the MSP-port during preloading. Active-LOW three-state control for the MSP-port during normal operation (see Table 1). (TSM*)

$LE_X/\overline{OE_X}$ Load Enable Extended/$\overline{\text{Output Enable Extended}}$ (Input)
Active-HIGH Load Enable for the XTP-port during preloading. Active-LOW three-state control for the XTP-port during normal operation (see Table 1). (TSX*)

PREL Preload (Input, Active HIGH)
When HIGH, data is preloaded into the specific output register when its respective load enable is HIGH. When LOW, the accumulator register is available at the P-port when the Output Enables are LOW (see Table 1).

$P_0 - P_{11}$ Bidirectional Port (Input/Output, Three-State)
Product Output for the Least Significant Product (LSP) and input to preload the LSP register.

$P_{12} - P_{23}$ Bidirectional Port (Input/Output, Three-State)
Product Output for the Most Significant Product (MSP) and input to preload the MSP register.

$P_{24} - P_{26}$ Bidirectional Port (Input/Output, Three-State)
Product Output for Extended Product (XTP) and input to preload the XTP register.

RND Round (Input, Active HIGH)
When RND is HIGH, a bit with a weight of P_{11} is added to the multiplier product. This addition causes the MSP and XTP to be rounded toward positive infinity. RND is loaded on the rising edge of CLK_X or CLK_Y.

$SUB/\overline{ADD}$ Subtraction/$\overline{\text{Addition}}$ (Input)
When HIGH, the accumulator contents are subtracted from the multiplier product and the result written back into the accumulator. When LOW, the multiplier product is added into the accumulator (see Table 2). The $SUB/\overline{ADD}$ control is loaded on the rising edge of CLK_X or CLK_Y.

TC Two's Complement (Input, Active HIGH)
When HIGH, the X and Y inputs are defined as two's-complement data, or as unsigned data when TC is LOW. The TC control is loaded on the rising edge of CLK_X or CLK_Y.

$X_0 - X_{11}$ Multiplier Data Input (Input, Active HIGH)
Data is loaded into the X register on the rising edge of CLK_X.

$Y_0 - Y_{11}$ Multiplier Data Input (Input, Active HIGH)
Data is loaded into the Y register on the rising edge of CLK_Y.

*TRW TDC1009 pin description.

FUNCTIONAL DESCRIPTION

The Am29C509 is a high-speed 12 x 12-bit CMOS multiplier/accumulator (MAC). It comprises a 12-bit parallel multiplier followed by a 27-bit accumulator. Two 12-bit input registers are provided for the X and Y operands. A third register stores two control bits, TC and RND. TC selects either a two's-complement or an unsigned magnitude format for both data inputs. The RND control, when HIGH, causes a bit to be added to the multiplier product with the weight of P_{11}. This causes the most significant 12 bits of the product to be rounded to the value nearest to the full 24-bit product. Using the RND control once during an accumulation causes the most significant 15 bits of the accumulator to be rounded to the value nearest the full 27-bit accumulation. The TC/RND register is clocked whenever the X or Y input registers are clocked.

The 24-bit multiplier output is zero-filled or sign-extended as appropriate to provide a 27-bit input to the accumulator. The accumulator has four functions: the product may be loaded into the accumulator, the product may be added into the accumulator value, the previous accumulator value may be subtracted from the product and the result stored in the accumulator, or the accumulator may be preloaded from an external source. The operation of the accumulator is controlled by the signals ACC, SUB/$\overline{ADD}$, and PREL. ACC and SUB/$\overline{ADD}$ are stored in a register clocked whenever the X or Y registers are clocked. ACC in conjunction with SUB/$\overline{ADD}$ selects one of the first three accumulator functions (see Table 2). For output and preloading purposes, the accumulator is considered in three sections: Extended Product (XTP, $P_{26} - P_{24}$), controlled by $LE_X/\overline{OE}_X$; Most Significant Product (MSP, P_{23}–P_{12}), controlled by $LE_M/\overline{OE}_M$; and Least Significant Product (LSP, $P_{11} - P_0$), controlled by $LE_L/\overline{OE}_L$. When PREL is LOW these controls are active-LOW Output Enables for the three-state output buffers. When PREL is HIGH, the output buffers automatically become high impedance, and the controls operate as active-HIGH Load Enables to the three sections of the accumulator to permit preloading of data applied to the bidirectional P-port. The P-port has 27 bits.

TABLE 1. PRELOAD FUNCTION

PREL	$LE_X/\overline{OE}_X$	$LE_M/\overline{OE}_M$	$LE_L/\overline{OE}_L$	Output Register		
				XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Key: Z = Output buffers at high impedance (disabled).
Q = Output buffers at low impedance. Contents of output register available through output ports.
PL = Output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLK_P.

TABLE 2. ACCUMULATOR FUNCTION

PREL	ACC	SUB/$\overline{ADD}$	P	OPERATION
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

Key: H = HIGH
L = LOW
X = Don't Care

Am29C509
INPUT FORMATS

Fractional Two's-Complement Input

X_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
-2^{0} (Sign)	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}

Y_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
-2^{0} (Sign)	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}

Integer Two's-Complement Input

X_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
-2^{11} (Sign)	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Y_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
-2^{11} (Sign)	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Input

X_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}

Y_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}

Unsigned Integer Input

X_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Y_{IN}

11	10	9	8	7	6	5	4	3	2	1	0
2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Am29C509
OUTPUT FORMATS

Two's-Complement Fractional Output

XTP

26	25	24
-2^{4} (Sign)	2^{3}	2^{2}

MSP

23	22	21	20	19	18	17	16	15	14	13	12
2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

LSP

11	10	9	8	7	6	5	4	3	2	1	0
2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Two's-Complement Integer Output

XTP

26	25	24
-2^{26} (Sign)	2^{25}	2^{24}

MSP

23	22	21	20	19	18	17	16	15	14	13	12
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}

LSP

11	10	9	8	7	6	5	4	3	2	1	0
2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Output

XTP

26	25	24
2^{2}	2^{1}	2^{0}

MSP

23	22	21	20	19	18	17	16	15	14	13	12
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}

LSP

11	10	9	8	7	6	5	4	3	2	1	0
2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Unsigned Integer Output

XTP

26	25	24
2^{26}	2^{25}	2^{24}

MSP

23	22	21	20	19	18	17	16	15	14	13	12
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}

LSP

11	10	9	8	7	6	5	4	3	2	1	0
2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Case Temperature (T_C) Under Bias .... −55 to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.3 to +7.0 V
DC Voltage Applied to Outputs For
High Output State .... −0.3 to $+V_{CC}$ +0.3 V
DC Input Voltage .... −0.3 to $+V_{CC}$ +0.3 V
DC Output Current, Into LOW Outputs .... 30 mA
DC Input Current .... −10 to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... 4.50 to 5.50 V

Military* (M) Devices
Case Temperature (T_C) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

* Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −0.4 mA		2.4	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4.0 mA		0.5	V
V_{IH}	Guaranteed Input Logical HIGH Voltage (Note 2)			2.0		V
V_{IL}	Guaranteed Input Logical LOW Voltage (Note 2)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V			−10	μA
I_I	Input HIGH Current	V_{CC} = Max., $V_{IN} = V_{CC} - 0.5$ V			10	μA
I_{OZH}	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V		10	μA
I_{OZL}			V_O = 0.5 V		10	
I_{CC}	Static Power Supply Current (Note 3)	V_{CC} = Max., $V_{IN} = V_{CC}$ or GND, I_O = 0 μA (CMOS)			20	mA
C_{PD}	Power Dissipation Capacitance (Note 4)	V_{CC} = 5.0 V, T_A = 25°C, No Load		890 pF Typical		

Notes: 1. V_{CC} conditions shown as Min. or Max. refer to the military (±10%) or commercial (±10%) V_{CC} limits.
2. These input levels provide zero-noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
3. Worst-case I_{CC} is measured at the lowest temperature in the specified operating range.
4. C_{PD} determines the no-load dynamic current consumption:
I_{CC} (Total) = I_{CC} (Static) + C_{PD} V_{CC} f, where f is the switching frequency of the majority of the internal nodes, normally one-half of the clock frequency.

value for Icc?
unspecified

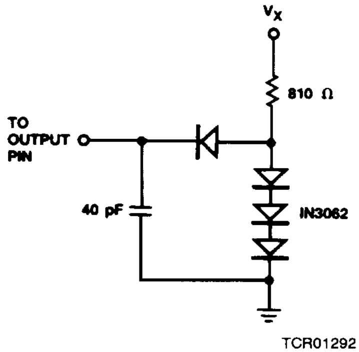
SWITCHING CHARACTERISTICS over COMMERCIAL operating range

No.	Parameter Symbol	Parameter Description		Test Conditions	29C509 Min.	29C509 Max.	29C509-1 Min.	29C509-1 Max.	29C509-2 Min.	29C509-2 Max.	Unit
1	t_{MA}	Multiply Accumulate Time				70		55		40	ns
2	t_S	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Setup Time			16		14		12		ns
3	t_H	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Hold Time			3		3		3		ns
4	t_S	PREL Setup Time			19		16		13		ns
5	t_H	PREL Hold Time			0		0		0		ns
6	t_{PWH}	Clock Pulse Width HIGH			15		15		15		ns
7	t_{PWL}	Clock Pulse Width LOW			15		15		15		ns
8	t_{PDP}	Output Clock to P				26		24		20	ns
9	t_{PHZ}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$, $LE_L/\overline{OE}_L$ to P Disable Time	HIGH to Z	40 pF		25		20		17	ns
10	t_{PLZ}		LOW to Z			25		20		17	ns
11	t_{PZH}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$, $LE_L/\overline{OE}_L$ to P Enable Time	Z to HIGH			30		25		22	ns
12	t_{PZL}		Z to LOW			30		25		22	ns
13	t_{HCL}	Relative Hold Time			0		0		0		ns

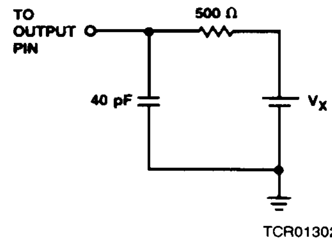
SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description		Test Conditions	29C509 Min.	29C509 Max.	29C509-1 Min.	29C509-1 Max.	Unit
1	t_{MA}	Multiply Accumulate Time				75		60	ns
2	t_S	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Setup Time			16		16		ns
3	t_H	X_i, Y_i, RND, TC, ACC, SUB/$\overline{ADD}$ Hold Time			3		3		ns
4	t_S	PREL Setup Time			20		16		ns
5	t_H	PREL Hold Time			0		0		ns
6	t_{PWH}	Clock Pulse Width HIGH			20		15		ns
7	t_{PWL}	Clock Pulse Width LOW			20		15		ns
8	t_{PDP}	Output Clock to P				30		25	ns
9	t_{PHZ}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$, $LE_L/\overline{OE}_L$ to P Disable Time	HIGH to Z	40 pF		25		21	ns
10	t_{PLZ}		LOW to Z			25		21	ns
11	t_{PZH}	$LE_X/\overline{OE}_X$, $LE_M/\overline{OE}_M$, $LE_L/\overline{OE}_L$ to P Enable Time	Z to HIGH			30		27	ns
12	t_{PZL}		Z to LOW			30		27	ns
13	t_{HCL}	Relative Hold Time			0		0		ns

SWITCHING TEST CIRCUITS



A. Normal Load

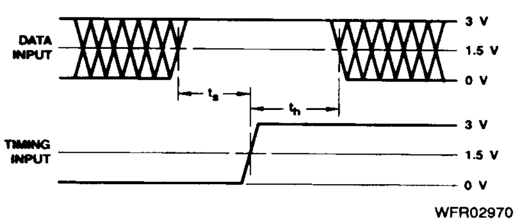


B. Three-State Delay Load

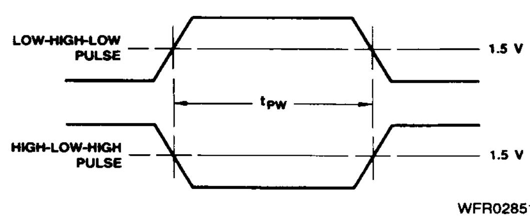
SWITCHING TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	V_{CC}	V_{OH}, V_{OL}; 1.5 V
t_{PHZ}	0.0 V	V_{OH}; 0.5 V; 0.0 V
t_{PLZ}	2.6 V	V_{OL}; 0.5 V; 2.6 V
t_{PZH}	0.0 V	0.0 V; 1.5 V; V_{OH}
t_{PZL}	2.6 V	2.6 V; 1.5 V; V_{OL}

WFR02812



A. Setup and Hold Time



B. Pulse Width

Notes: 1. Diagram shown for HIGH data only.
Output transition may be opposite sense.
2. Cross hatched area is "Don't Care" condition.

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown in the data sheet.

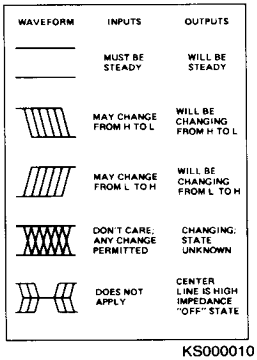
1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins which may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3.0$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Capacitive Loading for AC Testing
   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This makes it impossible to make direct measurements of parameters that call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is peformed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at <u>both</u> capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements (I_{OH}, I_{OL}, for example) have already been taken and are within spec. In some cases, special DC tests are performed in order to facilitate this correlation.
7. Threshold Testing
   The noise associated with automatic testing (due to the long inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for <u>each</u> input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.
8. AC Testing
   Occasionally parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer using data from precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

   In some cases, certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.
9. Output Short-Circuit Testing
   When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0$, $V_{CC} =$ Max. case.

SWITCHING WAVEFORMS

Key to Switching Waveforms



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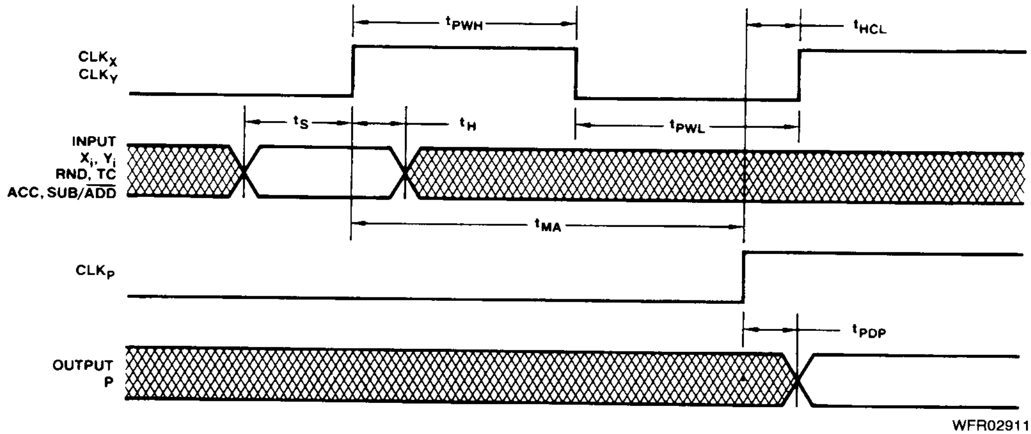
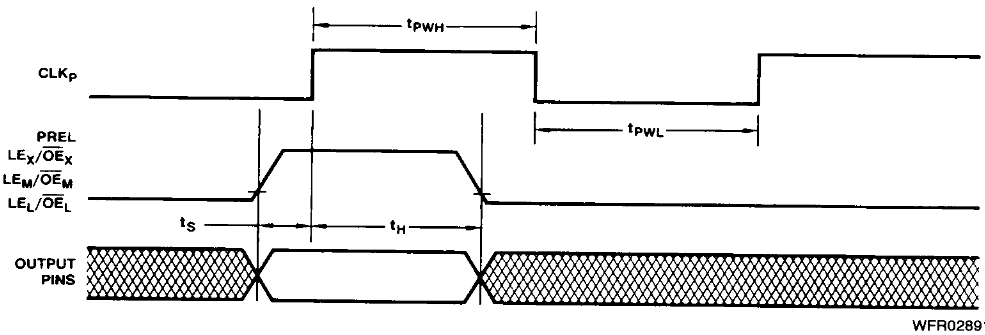
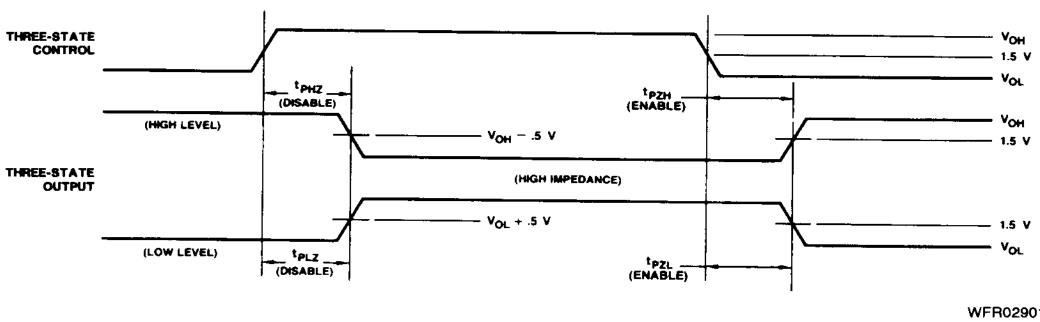
SWITCHING WAVEFORMS (Cont'd.)



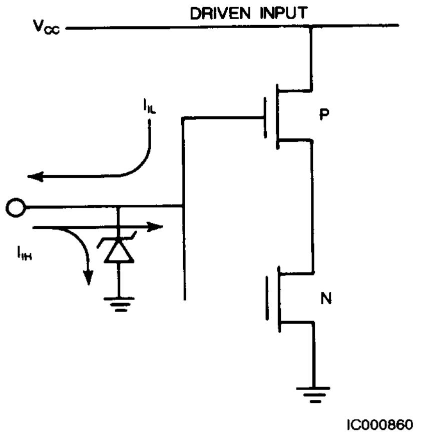


Preload Timing

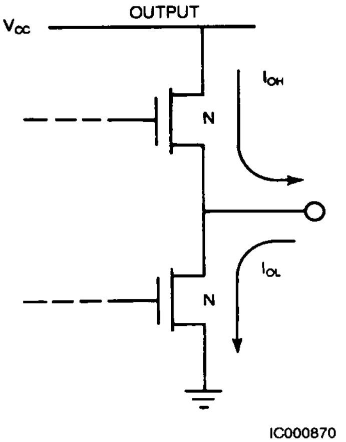


Three-State Timing

INPUT/OUTPUT CIRCUIT DIAGRAMS



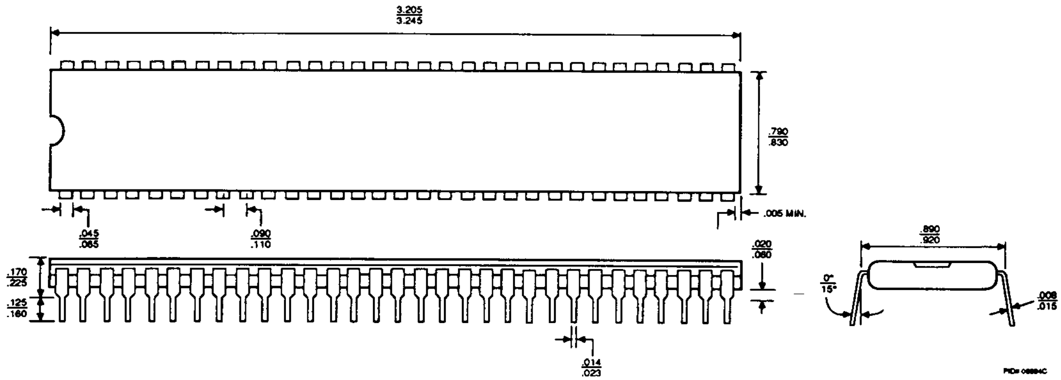
$C_I \approx 5.0$ pF, all inputs



$C_O \approx 5.0$ pF, all outputs

PHYSICAL DIMENSIONS*

PD 064



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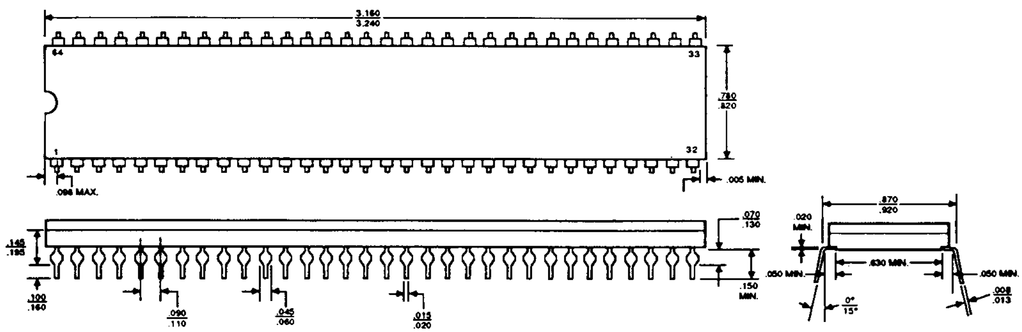
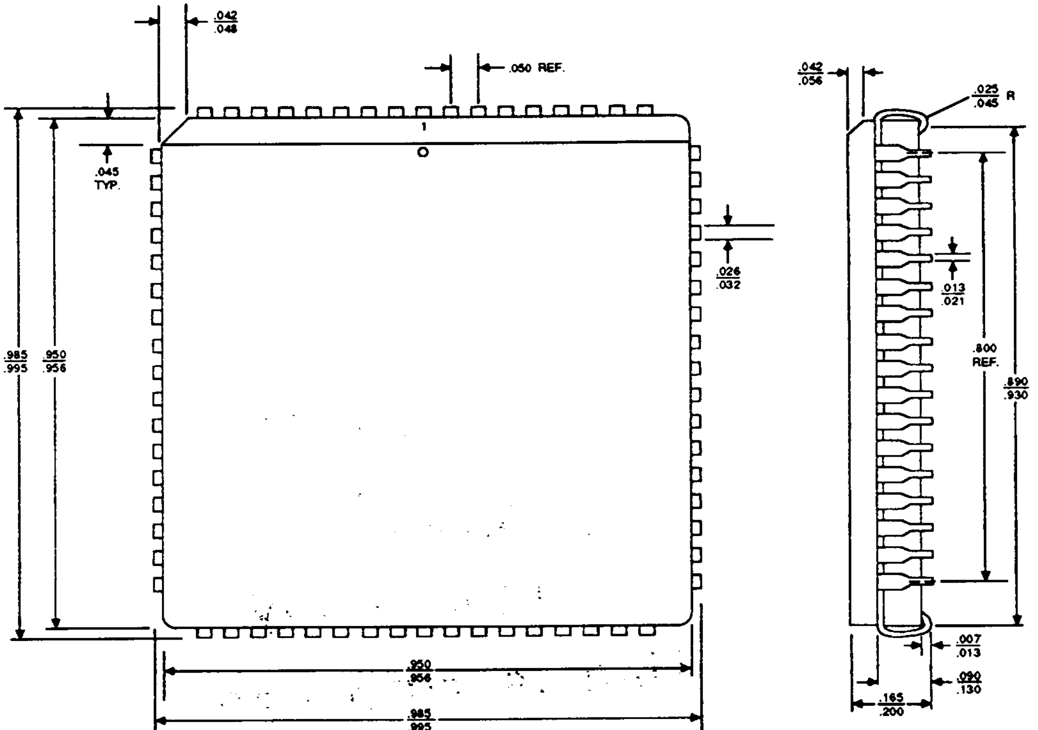


*For reference only.

PHYSICAL DIMENSIONS (Cont'd.)

PL 068



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