ACT™ 1 and ACT 2 Military Field Programmable Gate Arrays

ACT 1 Features

- Up to 2000 Gate Array Gates (6000 PLD equivalent gates)
- Replaces up to 53 TTL Packages
- Replaces up to seventeen 20-Pin PAL® Packages
- Design Library with over 250 Macro Functions
- Single Logic Module Architecture
- Up to 547 Logic Modules
- Up to 273 Flip-Flops
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 25 MHz
- Built-In High Speed Clock Distribution Network
- I/O Drive to 6 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

ACT 2 Features

- Up to 8000 Gate Array Gates (20,000 PLD equivalent gates)
- Replaces up to 200 TTL Packages
- Replaces up to eighty 20-Pin PAL Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to 1232 Programmable Logic Modules
- Up to 998 Flip-Flops
- 16-Bit Counter Performance at 50 MHz (MIL Temp)
- 16-Bit Accumulator Performance to 25 MHz (MIL Temp)
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 6 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

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Product Family Profile

Family	ACT 2		ACT 1	
Device	**A1280A**	**A1240A**	**A1020B**	**A1010B**
Capacity				
Gate Array Equivalent Gates	8,000	4,000	2,000	1,200
PLD Equivalent Gates	20,000	10,000	6,000	3,000
TTL Equivalent Packages	210	105	53	34
20-Pin PAL Equivalent Packages	69	34	17	12
Logic Modules	1,232	684	547	295
S-Modules	624	348	0	0
C-Modules	608	336	547	295
Flip-Flops (maximum)	998	565	273	147
Routing Resources				
Horizontal Tracks/Channel	36	36	22	22
Vertical Tracks/Channel	15	15	13	13
PLICE Antifuse Elements	750,000	400,000	190,000	110,000
User I/Os (maximum)	140	104	69	57
Packages[1]	176 CPGA 172 CQFP	132 CPGA	84 CPGA 84 CQFP	84 CPGA
CMOS Process	1.0 µm	1.0 µm	1.0 µm	1.0 µm

Note:
1. See product plan on page 1-142 for package availability.

High Reliability, Low Risk Solution

Actel builds the most reliable field programmable gate arrays (FPGAs) in the industry, with overall antifuse reliability ratings of less than 10 Failures-In-Time (FITs), corresponding to a useful life of more than 40 years. Actel FGPAs have been production-proven, with more than one million devices shipped and more than 130 billion antifuses manufactured. Actel devices are fully tested prior to shipment, with an outgoing defect level of only 122 ppm. (Further reliability data is available in the "Actel Reliability Report.")

100% Tested

Device functionality is fully tested before shipment and during device programming. Routing tracks, logic modules, and programming, debug, and test circuits are 100% tested before shipment. Antifuse integrity also is tested before shipment. Programming algorithms are tested when a device is programmed using Actel's Activator® 2 or Activator 2S programming stations.

Benefits

No Cost Risk—Once you have a Designer/Designer Advantage™ System, Actel's CAE software and programming package, you can produce as many chips as you like for just the cost of the device itself, with no NRE charges to eat up your development budget each time you want to try out a new design.

No Time Risk—After entering your design, placement and routing is automatic, and programming the device takes only about 5 to 15 minutes for an average design. You save time in the design entry process by using tools that are familiar to you. The Action Logic System software interfaces with popular CAE Cadence software such as Mentor Graphics®, OrCAD™, and Viewlogic® and runs on popular platforms such as HP™, Sun™, and 386/486™ PC compatible machines.

No Reliability Risk—The PLICE® antifuse is a one-time programmable, nonvolatile connection. Since Actel devices are permanently programmed, no downloading from EPROM or SRAM storage is required. Inadvertent erasure is impossible and there is no need to reload the program after power disruptions. Both the PLICE antifuses and the base process are radiation tolerant. Fabrication using a low-power CMOS process means cooler junction temperatures. Actel's non-PLD architecture delivers lower dynamic operating current. Our reliability tests show a very low failure rate of 66 FITs at 90°C junction temperature with no degradation in AC performance. Special stress testing at wafer test eliminates infant mortalities prior to packaging.

No Security Risk—Reverse engineering of programmed Actel devices from optical or electrical data is extremely difficult. Programmed antifuses cannot be identified from a photograph or by using a SEM. The antifuse map cannot be deciphered either electrically or by microprobing. Each device has a silicon signature that identifies its origins, down to the wafer lot and fabrication facility.

No Testing Risk—Unprogrammed Actel parts are fully tested at the factory. This includes the logic modules, interconnect tracks, and I/Os. AC performance is ensured by special speed path tests, and programming circuitry is verified on test antifuses. During the programming process, an algorithm is run to ensure that all antifuses are correctly programmed. In addition, Actel's Actionprobe® diagnostic tools allow 100% observability of all internal nodes to check and debug your design.

ACT 1 Description

The ACT™ 1 family of FPGAs offers a variety of package, speed, and application combinations. Devices are implemented in silicon gate, 1.2-micron two-level metal CMOS, and they employ Actel's PLICE antifuse technology. The unique architecture offers gate array flexibility, high performance, and instant turnaround through user programming. Device utilization is typically 95 percent of available logic modules.

ACT 1 devices also provide system designers with unique on-chip diagnostic probe capabilities, allowing convenient testing and debugging. Additional features include an on-chip clock driver with a hardwired distribution network. The network provides efficient clock distribution with minimum skew.

The user-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages include ceramic J-leaded chip carriers, ceramic quad flatpacks, and ceramic pin grid array.

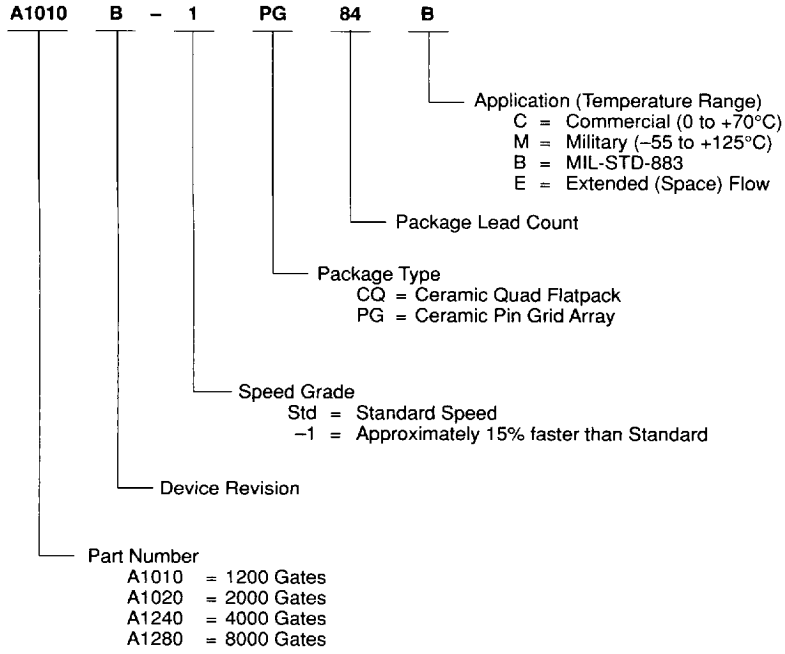
A security fuse may be programmed to disable all further programming and to protect the design from being copied or reverse engineered.

ACT 2 Description

The ACT 2 family represents Actel's second generation of FPGAs. The ACT 2 family presents a two-module architecture consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment. The devices are implemented in silicon gate, 1.0-µm, two-level metal CMOS, and employ Actel's PLICE antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming.

The ACT 2 family is supported by the ALS, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and debug and diagnostic probe capabilities. The Action Logic System is supported on the following platforms: 386/486 PC, Sun, and HP workstations. It provides CAE interfaces to the following design environments: Cadence, Viewlogic, Mentor Graphics, and OrCAD.

Military Device Ordering Information



SMD Drawing Number at Actel Part Number Cross Reference

SMD Number	Cage Number	Actel Part Number
5962-9096401MZC	0J4Z0	A1010A-PG84B
5962-9096501MUC	0J4Z0	A1020B-PG84B
5962-9096502MUC	0J4Z0	A1020B-IPG84B
5962-9096501MTC	0J4Z0	A1020B-CQ84B
5962-9096502MTC	0J4Z0	A1020B-ICQ84B
5962-9215601MXC	0J4Z0	A1280A-PG176B
5962-9215601MYC	0J4Z0	A1280A-CQ172B
5962-9215602MXC	0J4Z0	A1280A-1PG176B
5962-9215602MYC	0J4Z0	A1280A-1CQ172B

Product Plan

	Speed Grade*		Application			
	Std	–1	C	M	B	E
A1280A Device						
176-pin Ceramic Pin Grid Array (PG)	✔	P	✔	✔	✔	—
172-pin Ceramic Quad Flatpack (PQ)	✔	P	✔	✔	✔	✔
A1240A Device						
132-pin Ceramic Pin Grid Array (PG)	✔	P	✔	✔	✔	—
A1020B Device						
84-pin Ceramic Pin Grid Array (PG)	✔	✔	✔	✔	✔	—
84-pin Ceramic Quad Flatpack (CQ)	✔	✔	✔	✔	✔	✔
A1010B Device						
84-pin Ceramic Pin Grid Array (PG)	✔	✔	✔	✔	✔	—

Applications: C = Commercial, M = Military, B = MIL-STD-883, E = Extended Flow

Availability: ✔ = Available, P = Planned, — = Not Planned

* Speed Grade: –1 = Approx. 15% faster than Standard

Device Resources

			User I/Os				
			CPGA			CQFP	
Device Series	Logic Modules	Gates	176-pin	132-pin	84-pin	172-pin	84-pin
A1280A	1232	8000	140	—	—	140	—
A1240A	684	4000	—	104	—	—	—
A1020B	547	2000	—	—	69	—	69
A1020B	295	1200	—	—	57	—	—

Pin Description

CLKA **Clock A (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB **Clock B (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK **Diagnostic Clock (Input)**

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND **Ground**

LOW supply voltage.

I/O **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE **Mode (Input)**

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.

NC **No Connection**

This pin is not connected to circuitry within the device.

PRA **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} **5 V Supply Voltage**

HIGH supply voltage.

V_{KS} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to GND during normal operation.

V_{PP} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

V_{SV} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

Actel Military Product Flow

Step	Screen	833C—Class B 833C Method	833C—Class B Requirement	Military Datasheet Requirement
1.0	Internal Visual	2010, Test Condition B	100%	100%
2.0	Temperature Cycling	1010, Test Condition C	100%	100%
3.0	Constant Acceleration	2001, Test Condition E (min), Y1, Orientation Only	100%	100%
4.0	Seal	1014		
	a. Fine		100%	100%
	b. Gross		100%	100%
5.0	Visual Inspection		100%	100%
6.0	Pre Burn-in Electrical Parameters	In accordance with Actel applicable device specification	100%	N/A
7.0	Burn-in Test	1015 Condition D 160 hours @ 125°C Min.	100%	N/A
8.0	Interim (post burn-in) Electrical Parameters	In accordance with Actel applicable device specification	100%	100% (as final test)
9.0	Percent Defective Allowable	5%	All Lots	N/A
10.0	Final Electrical Test	In accordance with Actel applicable device specification		
	a. Static Tests (1) 25°C (Subgroup 1, Table I, 5005) (2) –55°C and +125°C (Subgroups 2, 3, Table I, 5005)		100%	100%
	b. Dynamic and Functional Tests (1) 25°C (Subgroup 7, Table I, 5005) (2) –55°C and +125°C (Subgroups 8A and 8B, Table I, 5005)		100%	100%
	c. Switching Tests at 25°C (Subgroup 9, Table I, 5005)		100%	100%
11.0	Qualification or Quality Confirmation Inspection Test Sample Selection (Group A)	5005	All Lots	N/A
12.0	External Visual	2009	100%	Actel specification

Actel Extended Flow[1]

	Screen	Method	Requirement
1.	Wafer Lot Acceptance	5007 with step coverage waiver	All Lots
2.	Destructive In-Line Bond Pull[2]	2011, condition D	Sample
3.	Internal Visual	2010, condition A	100%
4.	Temperature Cycling	1010, condition C	100%
5.	Constant Acceleration	2001, condition E (min), Y_1 orientation only	100%
6.	Visual Inspection	2009	100%
7.	Particle Impact Noise Detection	2020, condition A	100%
8.	Serialization		100%
9.	Pre Burn-in Test	In accordance with Actel applicable device specification	100%
10.	Burn-in Test	1015, 240 hours @ 125°C minimum	100%
11.	Interim (Post Burn-in) Electrical Parameters	In accordance with Actel applicable device specification	100%
12.	Reverse Bias Burn-in	1010, condition A or C, 72 hours @ 150°C minimum	100%
13.	Interim (Post Burn-in) Electrical Parameters	In accordance with Actel applicable device specification	100%
14.	Percent Defective Allowable (PDA) Calculation	5%, 3% functional parameters @ 25°C	All Lots
15.	Final Electrical Test	In accordance with Actel applicable device specification	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Dynamic and Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 5 and 6, 8a and b, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table I, 5005)	5005	100%
16.	Seal a. Fine b. Gross	1014	100%
17.	Radiographic	2012	100%
18.	Qualification or Quality Conformance Inspection Test Sample Selection	5005	Per Group A
19	External Visual	2009	100%

Notes:

1. Actel offers the Extended Flow in order to satisfy those customers that require additional screening beyond the requirements of MIL-STD-883C, Class B. Actel is compliant to the requirements of MIL-STD-883C, Paragraph 1.2.1, and MIL-M-38510 Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883C Class S. The exceptions to Method 5004 are shown in Notes 2 to 4 below.
2. Method 5004 requires a 100%, Non-Destructive Bond Pull to Method 2023. Actel substitutes a Non-Destructive Bond Pull to Method 2011, condition D on a sample basis only.

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2,3,4]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[5]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
2. $V_{PP} = V_{CC}$, except during device programming.
3. $V_{SV} = V_{CC}$, except during device programming.
4. V_{KS} = GND, except during device programming.
5. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diode will be forward biased and can draw excessive current.

Recommended Operating Conditions

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	–55 to +125	°C
Power Supply Tolerance	±5	±10	%V_{CC}

Note:

1. Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 176-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp.}}{\theta ja\ (°C/W)} = \frac{150°C - 125°C}{23°C/W} = 1.1\ W$$

Package Type	Pin Count	θjc	θja Still Air	θja 300 ft/min	Units
Ceramic Pin Grid Array	84	8	33	20	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	84	5	40	30	°C/W
	172	8	25	15	°C/W

ACT 1 Electrical Specifications

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –6 mA)	3.84				V
	(I_{OH} = –4 mA)			3.7		V
V_{OL}[1]	(I_{OL} = 6 mA)		0.33		0.40	V
V_{IL}		–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10	pF
Standby Current, I_{CC}[4]			3		20	mA
Leakage Current[5]		–10	10	–10	10	µA
I_{OS} Output Short Circuit Current[6]	(V_O = V_{CC})	20	140	20	140	mA
	(V_O = GND)	–10	–100	–10	–100	mA

Notes:
1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. Typical standby current = 3 mA. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O, V_{IN} = V_{CC} or GND.
6. Only one output tested at a time. Min. at V_{CC} = 4.5 V; Max. at V_{CC} = 5.5 V.

ACT 2 Electrical Specifications

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –6 mA)	3.84				V
	(I_{OH} = –4 mA)			3.7		V
V_{OL}[1]	(I_{OL} = 6 mA)		0.33		0.40	V
V_{IL}		–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10	pF
Standby Current, I_{CC}[4]			2		20	mA
Leakage Current[5]		–10	10	–10	10	µA

Notes:
1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 176 CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O , V_{IN} = V_{CC} or GND.

ACT 1 Power Dissipation

The following formula is used to calculate total device dissipation.

Total Device Power (mW) = (0.20 x N x F1) + (0.085 x M x F2) + (0.80 x P x F3)

Where:

F1 = Average logic module switching rate in MHz

F2 = CLKBUF macro switching rate in MHz

F3 = Average I/O module switching rate in MHz

M = Number of logic modules connected to the CLKBUF macro

N = Total number of logic modules used in the design (including M)

P = Number of outputs loaded with 50 pF

Average switching rate of logic modules and of I/O modules is some fraction of the device operating frequency (usually CLKBUF). Logic modules and I/O modules switch states (from low-to-high or from high-to-low) only if the input data changes when the module is enabled. A conservative estimate for average logic module and I/O module switching rates (variables F1 and F3, respectively) is 10% of device clock driver frequency.

If the CLKBUF macro is not used in the design, eliminate the second term (including F2 and M variables) from the formula.

Sample A1020 Device Power Calculation

To illustrate the power calculation, consider a large design operating at high frequency. This sample design utilizes 85% of available logic modules on the A1020-series device (.85 x 547 = 465 logic modules used). The design contains 104 flip-flops (208 logic modules). Operating frequency of the design is 16 MHz. In this design, the CLKBUF macro drives the clock network. Logic modules and I/O modules are switching states at approximately 10% of the clock frequency rate (.10 x 16 MHz = 1.6 MHz). Sixteen outputs are loaded with 50 pF.

To summarize the design described above: N = 465; M = 208; F2 = 16; F1 = 4; F3 = 4; P = 16. Total device power can be calculated by substituting these values for variables in the device dissipation formula.

Total device power for this example =

(0.20 x 465 x 1.6) + (0.085 x 208 x 16) + (0.80 x 16 x 1.6) = 452 mW

ACT 2 Power Dissipation

$P = [I_{CC} + I_{active}] * V_{CC} + I_{OL}*V_{OL}*N + I_{OH}*(V_{CC}-V_{OH})*M$

Where:

I_{CC} is the current flowing when no inputs or outputs are changing.

I_{active} is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematic because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power

Static power dissipation is typically a small component of the overall power. From the values provided in the Electrical Specifications, the maximum static power (commercial) dissipation is:

2 mA * 5.25 V = 10.5 mW

The static power dissipation by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32-bit bus driving TTL loads will generate 42 mW with all outputs driving low or 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Time

The active power component in CMOS devices is frequency dependent and is contingent on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power } (\mu W) = C_{EQ} * V_{CC}^2 * f \quad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in picofarads(pF).
V_{CC} is power supply in volts (V).
f is the switching frequency in megahertz (MHz).

Equivalent capacitance is calculated by measuring I_{active} at a specified frequency and voltage for each circuit component of interest. The results for ACT 2 devices are:

	C_{EQ} (pF)
Modules	7.7
Input Buffers	18.0
Output Buffers	25.0
Clock Buffer Loads	2.5

To calculate the active power dissipated from the complete design, you must solve Equation 1 for each component. To do this, you must know the switching frequency of each part of the logic. The exact equation is a piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Power } (\mu W) = [(m * 7.7 \times f_1) + (n * 18.0 \times f_2) + (p * (25.0 + C_L) * f_3) + (q \times 2.5 \times f_4)] * V_{CC}^2 \quad (2)$$

Where:

m = Number of logic modules switching at frequency f_1
n = Number of input buffers switching at frequency f_2
p = Number of output buffers switching at frequency f_3
q = Number of clock loads on the global clock network
f_1 = Average logic module switching rate in MHz
f_2 = Average input buffer switching rate in MHz
f_3 = Average output buffer switching rate in MHz
f_4 = Frequency of global clock
C_L = Output load capacitance in pF

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules will help you to determine average switching frequency in logic circuits. These rules are meant to represent worst-case scenarios so that they generally can be used to predict the upper limits of power dissipation. These rules are as follows:

Module Utilization = 80% of combinatorial modules

Average Module Frequency = F/10

Inputs = 1/3 of I/O

Average Input Frequency = F/5

Outputs = 2/3 of I/Os

Average Output Frequency = F/10

Clock Net 1 Loading = 40% of sequential modules

Clock Net 1 Frequency = F

Clock Net 2 Loading = 40% of sequential modules

Clock Net 2 Frequency = F/2

Estimated Power

The results of estimating active power are displayed in Figure 1. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies.

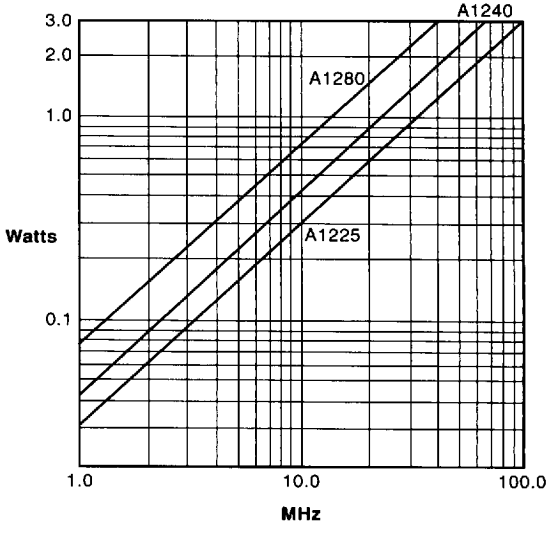
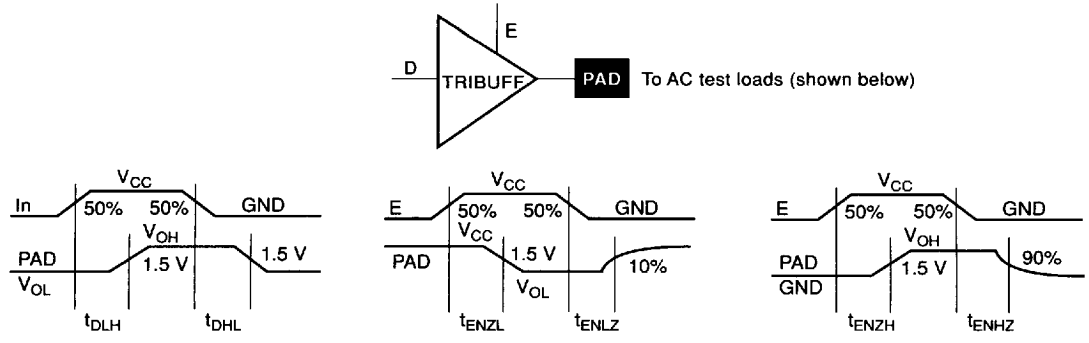


Figure 1. ACT 2 Power Estimates

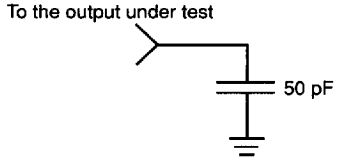
Parameter Measurement

Output Buffer Delays

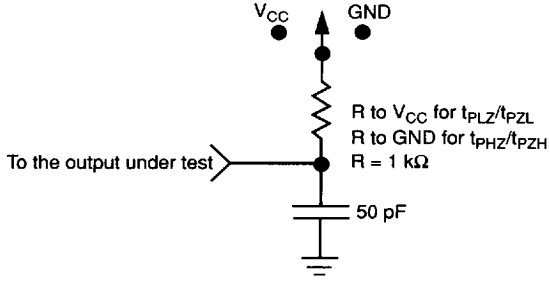


AC Test Load

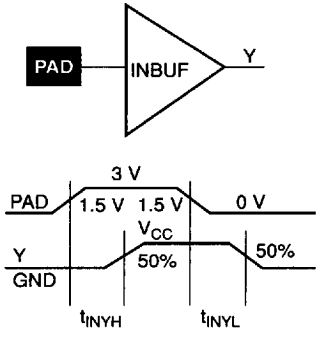
Load 1
(Used to measure propagation delay)



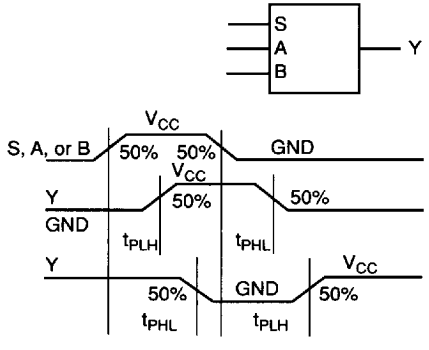
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

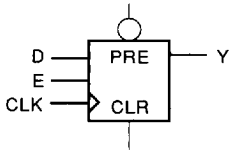


Combinatorial Macro Delays

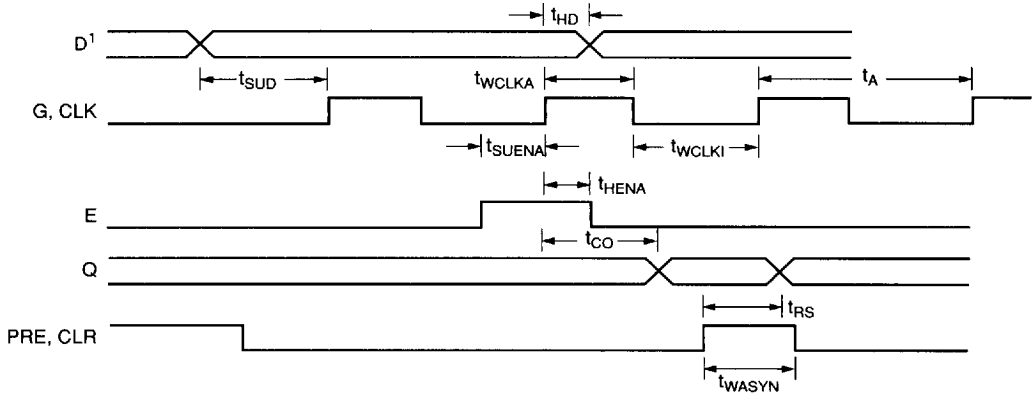


Sequential Timing Characteristics

Flip-Flops and Latches



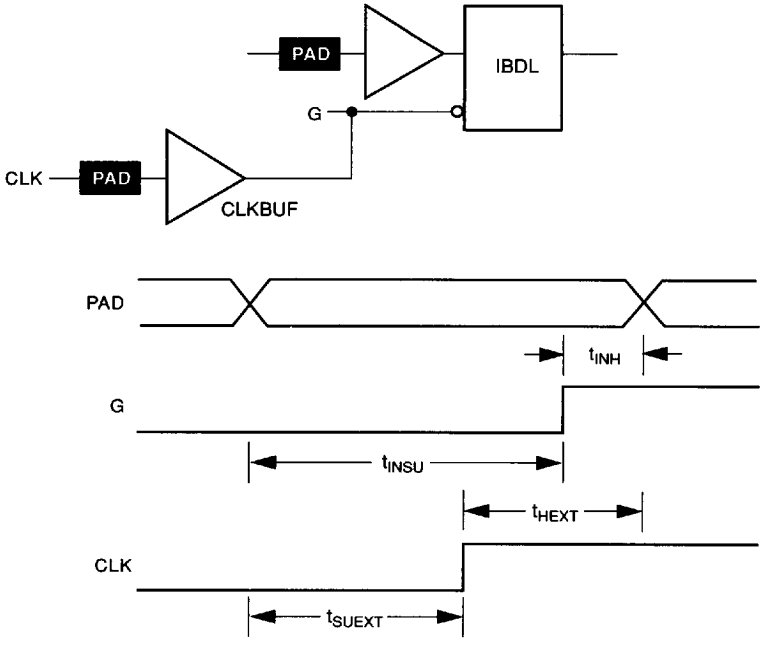
(Positive edge triggered)



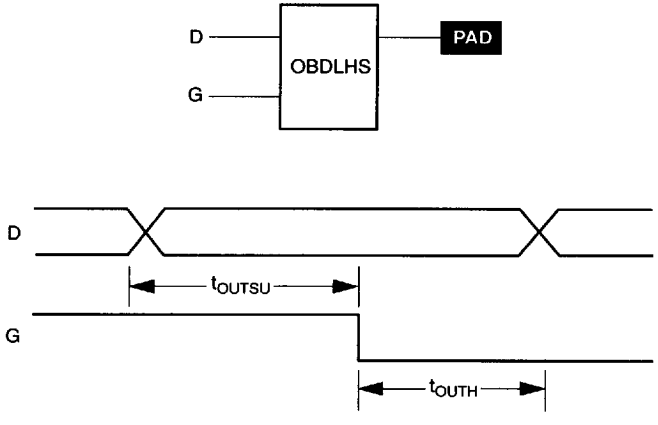
Note:
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

Input Buffer Latches (ACT 2 only)



Output Buffer Latches (ACT 2 only)



ACT 1 Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		5.5		4.7	ns
t_{PD2}	Dual Module Macros		12.7		10.8	ns
t_{CO}	Sequential Clk to Q		5.5		4.7	ns
t_{GO}	Latch G to Q		5.5		4.7	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.5		4.7	ns
Predicted Routing Delays[1]						
t_{RD1}	FO=1 Routing Delay		1.7		1.5	ns
t_{RD2}	FO=2 Routing Delay		2.7		2.3	ns
t_{RD3}	FO=3 Routing Delay		4.0		3.4	ns
t_{RD4}	FO=4 Routing Delay		5.9		5.0	ns
t_{RD8}	FO=8 Routing Delay		12.5		10.6	ns
Sequential Timing Characteristics[2]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	10.4		8.8		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	10.4		8.8		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	12.9		10.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	12.9		10.9		ns
t_A	Flip-Flop Clock Input Period	27.3		23.2		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		37		44	MHz

Notes:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
2. Setup times assume fanout of 3. Further derating information can be obtained from the ALS Timer utility.

ACT 1 Timing Characteristics (continued)

(Worst-Case Military Conditions)

Input Module Propagation Delays			'Std' Speed		'–1' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			5.8		4.9	ns
t_{INYL}	Pad to Y Low			5.8		4.9	ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			1.7		1.5	ns
t_{IRD2}	FO=2 Routing Delay			2.7		2.3	ns
t_{IRD3}	FO=3 Routing Delay			4.0		3.4	ns
t_{IRD4}	FO=4 Routing Delay			5.9		5.0	ns
t_{IRD8}	FO=8 Routing Delay			12.5		10.6	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 16 FO = 128		9.2 10.5		7.8 8.9	ns
t_{CKL}	Input High to Low	FO = 16 FO = 128		12.1 13.2		10.3 11.2	ns
t_{PWH}	Minimum Pulse Width High	FO = 16 FO = 128	12.2 12.9		10.4 10.9		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16 FO = 128	12.2 12.9		10.4 10.9		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		2.2 3.4		1.9 2.9	ns
t_P	Minimum Period	FO = 16 FO = 128	25.6 27.3		21.7 23.2		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		40 37		46 44	MHz

Note:

1. These parameters should be used for estimating device performance. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

ACT 1 Timing Characteristics (continued)

(Worst-Case Military Conditions)

Output Module Timing		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		14.2		12.1	ns
t_{DHL}	Data to Pad Low		16.3		13.8	ns
t_{ENZH}	Enable Pad Z to High		14.1		12.0	ns
t_{ENZL}	Enable Pad Z to Low		17.1		14.6	ns
t_{ENHZ}	Enable Pad High to Z		18.8		16.0	ns
t_{ENLZ}	Enable Pad Low to Z		17.0		14.5	ns
d_{TLH}	Delta Low to High		0.11		0.09	ns/pF
d_{THL}	Delta High to Low		0.15		0.12	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		17.7		15.1	ns
t_{DHL}	Data to Pad Low		13.6		11.5	ns
t_{ENZH}	Enable Pad Z to High		14.1		12.0	ns
t_{ENZL}	Enable Pad Z to Low		17.1		14.6	ns
t_{ENHZ}	Enable Pad High to Z		18.8		16.0	ns
t_{ENLZ}	Enable Pad Low to Z		17.0		14.5	ns
d_{TLH}	Delta Low to High		0.18		0.16	ns/pF
d_{THL}	Delta High to Low		0.11		0.09	ns/pF

Note:
1. Delays based on 50 pF loading.

A1240A Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays[1]		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		6.1		5.2	ns
t_{CO}	Sequential Clk to Q		6.1		5.2	ns
t_{GO}	Latch G to Q		6.1		5.2	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		6.1		5.2	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		2.2		1.9	ns
t_{RD2}	FO=2 Routing Delay		2.8		2.4	ns
t_{RD3}	FO=3 Routing Delay		3.7		3.1	ns
t_{RD4}	FO=4 Routing Delay		5.0		4.3	ns
t_{RD8}	FO=8 Routing Delay		7.7		6.6	ns
Sequential Timing Characteristics[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	1.0		1.0		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	2.0		2.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	7.5		7.5		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	8.4		7.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	8.4		7.1		ns
t_A	Flip-Flop Clock Input Period	18.6		15.8		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Setup	–3.5		–3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	1.0		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		54		63	MHz

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the ALS Timer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Input Module Propagation Delays			'Std' Speed		'–1' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			4.7		4.0	ns
t_{INYL}	Pad to Y Low			4.3		3.6	ns
t_{INGH}	G to Y High			8.1		6.9	ns
t_{INGL}	G to Y Low			7.7		6.6	ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			6.9		5.8	ns
t_{IRD2}	FO=2 Routing Delay			7.8		6.7	ns
t_{IRD3}	FO=3 Routing Delay			8.8		7.5	ns
t_{IRD4}	FO=4 Routing Delay			9.7		8.2	ns
t_{IRD8}	FO=8 Routing Delay			12.9		10.9	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 32		15.7		13.3	ns
		FO = 256		19.2		16.3	
t_{CKL}	Input High to Low	FO = 32		15.7		13.3	ns
		FO = 256		19.5		16.5	
t_{PWH}	Minimum Pulse Width High	FO = 32	6.7		5.7		ns
		FO = 256	7.1		6.0		
t_{PWL}	Minimum Pulse Width Low	FO = 32	6.7		5.7		ns
		FO = 256	7.1		6.0		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5	ns
		FO = 256		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		ns
		FO = 256	0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		ns
		FO = 256	11.2		11.2		
t_P	Minimum Period	FO = 32	13.5		11.5		ns
		FO = 256	14.3		12.2		
f_{MAX}	Maximum Frequency	FO = 32		74		87	MHz
		FO = 256		70		82	

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Output Module Timing		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		13.0		11.0	ns
t_{DHL}	Data to Pad Low		16.4		13.9	ns
t_{ENZH}	Enable Pad Z to High		14.4		12.3	ns
t_{ENZL}	Enable Pad Z to Low		19.0		16.1	ns
t_{ENHZ}	Enable Pad High to Z		11.5		9.8	ns
t_{ENLZ}	Enable Pad Low to Z		13.6		11.5	ns
t_{GLH}	G to Pad High		14.6		12.4	ns
t_{GHL}	G to Pad Low		18.2		15.5	ns
d_{TLH}	Delta Low to High		0.11		0.09	ns/pF
d_{THL}	Delta High to Low		0.20		0.17	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		16.5		14.0	ns
t_{DHL}	Data to Pad Low		13.7		11.7	ns
t_{ENZH}	Enable Pad Z to High		14.4		12.3	ns
t_{ENZL}	Enable Pad Z to Low		19.0		16.1	ns
t_{ENHZ}	Enable Pad High to Z		11.5		9.8	ns
t_{ENLZ}	Enable Pad Low to Z		13.6		11.5	ns
t_{GLH}	G to Pad High		14.6		12.4	ns
t_{GHL}	G to Pad Low		18.2		15.5	ns
d_{TLH}	Delta Low to High		0.20		0.17	ns/pF
d_{THL}	Delta High to Low		0.15		0.12	ns/pF

Note:
1. Delays based on 50 pF loading.

A1280A Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays[1]		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		6.1		5.2	ns
t_{CO}	Sequential Clk to Q		6.1		5.2	ns
t_{GO}	Latch G to Q		6.1		5.2	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		6.1		5.2	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		2.8		2.4	ns
t_{RD2}	FO=2 Routing Delay		4.0		3.4	ns
t_{RD3}	FO=3 Routing Delay		4.9		4.2	ns
t_{RD4}	FO=4 Routing Delay		6.0		5.1	ns
t_{RD8}	FO=8 Routing Delay		10.8		9.2	ns
Sequential Timing Characteristics[3,4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	1.0		1.0		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	2.0		2.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	7.5		7.5		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	11.6		9.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	11.6		9.9		ns
t_A	Flip-Flop Clock Input Period	24.5		20.8		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Setup	–3.5		–3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	1.0		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		41		48	MHz

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the ALS Timer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Input Module Propagation Delays			'Std' Speed		'–1' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			4.7		4.0	ns
t_{INYL}	Pad to Y Low			4.3		3.6	ns
t_{INGH}	G to Y High			8.1		6.9	ns
t_{INGL}	G to Y Low			7.7		6.6	ns
Input Module Predicted Routing Delays[1]							
t_{RD1}	FO=1 Routing Delay			7.3		6.2	ns
t_{RD2}	FO=2 Routing Delay			8.4		7.2	ns
t_{RD3}	FO=3 Routing Delay			9.1		7.7	ns
t_{RD4}	FO=4 Routing Delay			10.5		8.9	ns
t_{RD8}	FO=8 Routing Delay			15.2		12.9	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 32		15.7		13.3	ns
		FO = 384		21.1		17.9	
t_{CKL}	Input High to Low	FO = 32		15.7		13.3	ns
		FO = 384		21.4		18.2	
t_{PWH}	Minimum Pulse Width High	FO = 32	8.1		6.9		ns
		FO = 384	9.3		7.9		
t_{PWL}	Minimum Pulse Width Low	FO = 32	8.1		6.9		ns
		FO = 384	9.3		7.9		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5	ns
		FO = 384		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		ns
		FO = 384	0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		ns
		FO = 384	11.2		11.2		
t_P	Minimum Period	FO = 32	16.2		13.7		ns
		FO = 384	18.9		16.0		
f_{MAX}	Maximum Frequency	FO = 32		62		73	MHz
		FO = 384		53		63	

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1280A Timing Characteristics (continued)

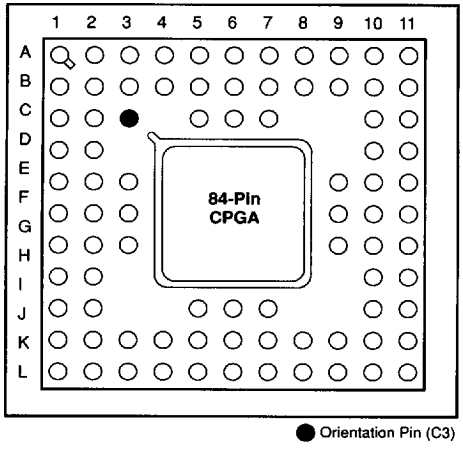
(Worst-Case Military Conditions)

Output Module Timing		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		13.0		11.0	ns
t_{DHL}	Data to Pad Low		16.4		13.9	ns
t_{ENZH}	Enable Pad Z to High		14.4		12.3	ns
t_{ENZL}	Enable Pad Z to Low		19.0		16.1	ns
t_{ENHZ}	Enable Pad High to Z		11.5		9.8	ns
t_{ENLZ}	Enable Pad Low to Z		13.6		11.5	ns
t_{GLH}	G to Pad High		14.6		12.4	ns
t_{GHL}	G to Pad Low		18.2		15.5	ns
d_{TLH}	Delta Low to High		0.11		0.09	ns/pF
d_{THL}	Delta High to Low		0.20		0.17	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		16.5		14.0	ns
t_{DHL}	Data to Pad Low		13.7		11.7	ns
t_{ENZH}	Enable Pad Z to High		14.4		12.3	ns
t_{ENZL}	Enable Pad Z to Low		19.0		16.1	ns
t_{ENHZ}	Enable Pad High to Z		11.5		9.8	ns
t_{ENLZ}	Enable Pad Low to Z		13.6		11.5	ns
t_{GLH}	G to Pad High		14.6		12.4	ns
t_{GHL}	G to Pad Low		18.2		15.5	ns
d_{TLH}	Delta Low to High		0.20		0.17	ns/pF
d_{THL}	Delta High to Low		0.15		0.12	ns/pF

Note:
1. Delays based on 50 pF loading.

Package Pin Assignments

84-Pin CPGA (Top View)

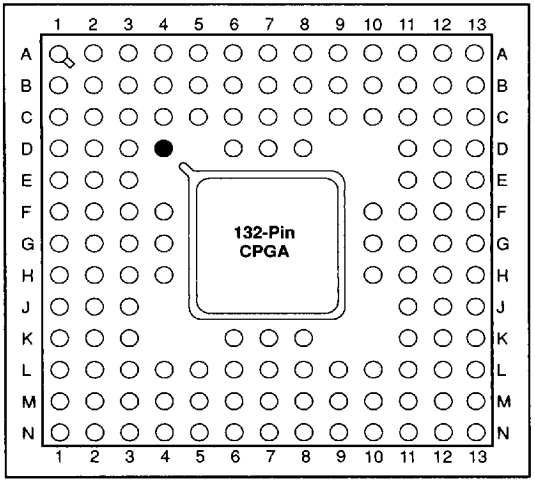


Signal	A1010B Devices	A1020B Devices
PRA	A11	A11
PRB	B10	B10
MODE	E11	E11
SDI	B11	B11
DCKL	C10	C10
V_{PP}	K2	K2
CLK or I/O	F9	F9
GND	B7, E2, E3, K5, F10, G10	B7, E2, E3, K5, F10,G10
V_{CC}	B5, F1, G2, K7, E9, E10	B5, F1, G2, K7, E9, E10
N/C (No Connection)	B1, B2, C1, C2, K1, J2, J10, K10, K11, C11, D10, D11	B2

Notes:
1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

Package Pin Assignments

132-Pin CPGA (Top View)

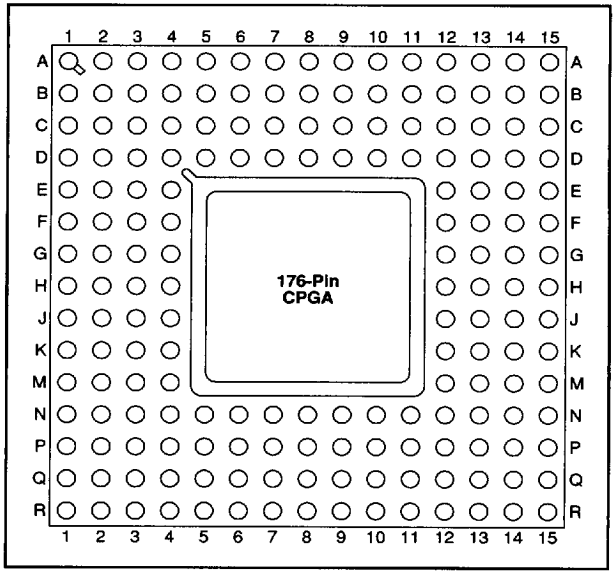


Signal	Pad Number	Location
PRA or I/O	113	B8
PRB or I/O	121	C6
MODE	2	A1
SDI or I/O	101	B12
DCLK or I/O	132	C3
CLKA or I/O	115	B7
CLKB or I/O	119	B6
GND	9, 10, 26, 27, 41, 58, 59, 73, 74, 92, 93, 107, 108, 125, 126	E3, F4, J2, J3, L5, L9, M9, K12, J11, E12, E11, C9, B9, B5, C5
V_{CC}	18, 19, 49, 50, 83, 84, 116, 117	G3, G2, L7, K7, G10, G11, D7, C7
V_{PP}	82	G13
V_{SV}	17, 85	G4, G12
V_{KS}	81	H13

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments

176-Pin CPGA (Top View)

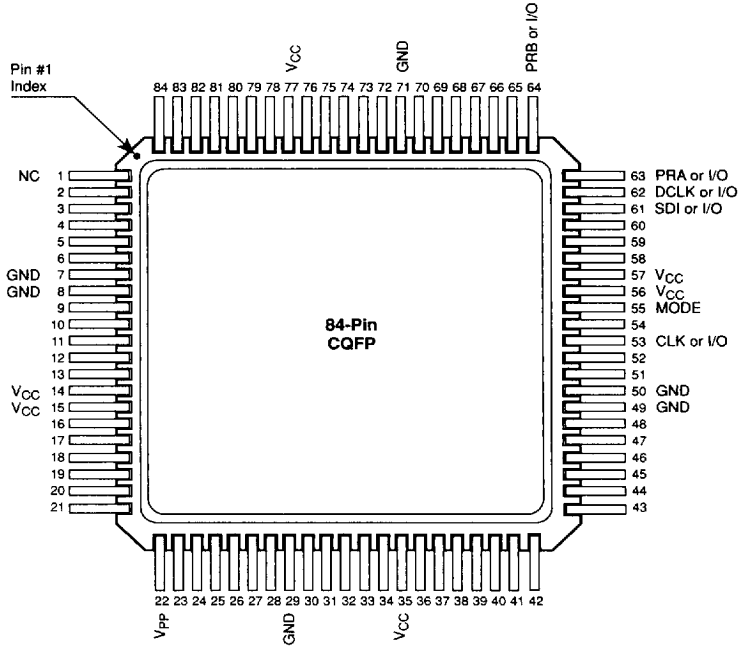


Signal	Pad Number	Location
PRA or I/O	152	C9
PRB or I/O	160	D7
MODE	2	C3
SDI or I/O	135	B14
DCLK or I/O	175	B3
CLKA or I/O	154	A9
CLKB or I/O	158	B8
GND	1, 8, 18, 23, 33, 38, 45, 57, 67, 77, 89 101, 106, 111, 121, 126, 133, 145, 156, 165	D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12 K12, J12, H12, F12, E12, D12, D10, C8, D6
V_{CC}	13, 24, 28, 52, 68, 82, 112, 116, 140, 155, 170	F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5
V_{PP}	110	J14
V_{SV}	25, 113	H2, H14
V_{KS}	109	J13

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments

84-Pin CQFP

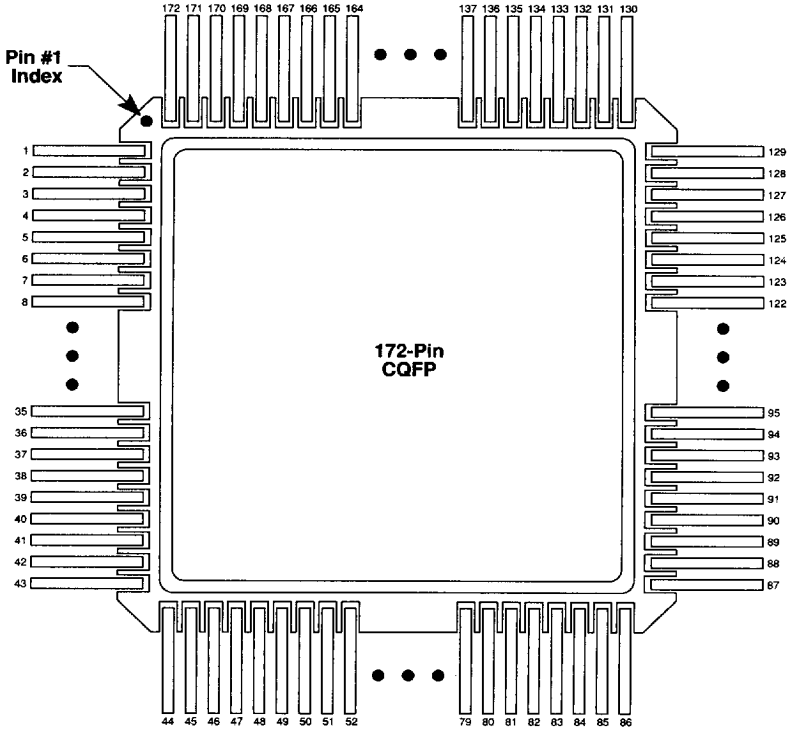


Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

Package Pin Assignments

172-Pin CQFP (Top View)



Signal	PIN Number
MODE	1
GND	7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 108, 118, 123, 141, 152, 161
V_{CC}	12, 23, 27, 50, 66, 80, 109, 113, 136, 151, 166
V_{SV}	24, 110
V_{KS}	106
V_{PP}	107
SDI or I/O	131
PRA or I/O	148
PRB or I/O	156
CLKA or I/O	150
CLKB or I/O	154
DCLK or I/O	171

Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.