



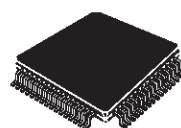
ADSL MODEM CHIP SET

PRODUCT PREVIEW

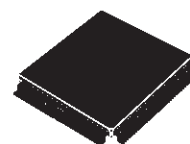
- COMPLETE CHIP SET FOR ADSL MODEM FUNCTIONS
- COMPLIANCE WITH ANSI T1.413 ISSUE 1 & ISSUE 2
- IMPLEMENTS DISCRETE MULTITONE (DMT) MODULATION AND DEMODULATION
- DATA RATES UP TO 8Mbps DOWNSTREAM AND TO 1Mbps UPSTREAM WITH 32Kbps GRANULARITY
- BUILT-IN ATM TRANSPORT
- SUPPORT ADAPTIVE RATE MODE IN 32Mbps INCREMENTS
- APPLICABLE AT BOTH ENDS OF LOOP: ATU-C (LT) AND ATU-R (NT)
- 255 CARRIERS WITH 4.3125KHz SPACING
- DEDICATED SOFTWARE DRIVER AVAILABLE
- PROCESSOR INDEPENDENT C++ SOURCE COMPILATION
- FREQUENCY DIVISION MULTIPLEXING (FDM) FOR HIGH ROBUSTNESS IN PRESENCE OF CROSSTALK
- REED-SOLOMON FORWARD ERROR CORRECTION
- TRELLIS CODER AND DECODER
- PROGRAMMABLE SIMULTANEOUS SUPPORT OF INTERLEAVED AND NON-INTERLEAVED CHANNELS (DUAL LATENCY)
- FULL, REDUCED AND MINIMAL ATM OVERHEAD FRAMING MODES
- BIT STREAM MODE CAPABILITY FOR STM TRANSPORT
- DIRECT CONNECTION TO ATM SYSTEMS VIA UTOPIA INTERFACE (LEVEL 1 OR 2)
- MICROCONTROLLER INTERFACE WITH 16 BITS MULTIPLEXED ADDRESS/DATA BUS
- LOW POWER TECHNOLOGY: 1.3w TOTAL
- SINGLE 3.3V POWER SUPPLY
- -40 TO +85°C OPERATING TEMP RANGE

Applications

- HIGH SPEED INTERNET ACCESS
- REMOTE ACCESS TO CORPORATE NETWORK FOR TELECOMMUTERS AND BRANCH OFFICES
- VIDEO-ON-DEMAND OVER TWISTED PAIR



TQFP64



PQFP144

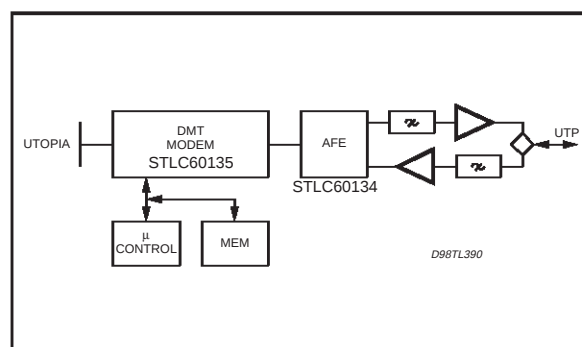
ORDERING NUMBERS: STLC60134 (TQFP64)
STLC60135 (PQFP144)

- ADSL MODEMS, DSLAMS, ROUTERS, AND CONCENTRATORS
- ADSL PC NIC's
- LITE-ADSL T1.413 BASED FOR NT-SIDE SPLITTERLESS APPLICATIONS

GENERAL DESCRIPTION

The ADSL modem chip set with ATM interface provides all the active functions required to build a complete ATM-based ADSL modem from line interface to ATM UTOPIA bus. The chip set employs Discrete MultiTone modulation as specified in ANSI T1.413. The chip set can operate at either end of the loop (in ATU-C or ATU-R mode) with only changes in the microcontroller code. Reed-Solomon forward error correction plus Trellis coding with or without interleaving in internal interleaving RAM provides maximum noise immunity.

Figure 1. ADSL modem block configuration.



Interleaving is optional and can be used simultaneously on a slow channel (e.g., for data or control info) while a fast channel (e.g., video) operates without interleaving. ICs include rate adaptation capabilities during show time.

In transmit direction the chip set allows to select an attenuation of the signal in case of short loops or large echo (politeness). In receive direction the chip set can optionally control an external multiplexer to select an external attenuation of the signal in case of short loops.

TOSCA chip set

TOSCA is a two-chip ADSL modem transceiver. ST also provides the necessary software for transceiver's external controller.

TOSCA can easily be hooked up with ATM systems through the built-in UTOPIA level 2 interface. That allows ATM traffic to be carried, at up to 8Mbit/s downstream and 1Mbit/s upstream, over a very plain and widespread twisted pair.

TOSCA can be used at both ends of the loop (ATU-C and ATU-R ends).

The modem control software can be compiled as C++ code, independently on the processor used.

The driver can be interfaced to any external real time operating system.

These pages block diagrams show the main functions built-in in STLC60134 and STLC60135.

TOSCA chip set supports three different rate adaptation modes: fixed rate adaptation mode, fixed with capability to boost within fixed range, dynamic rate adaptation during show time.

Modem's performances are set by the following

parameters: Rate adaptation mode, Downstream and Upstream bit rate for both latency paths, Noise margins (min, max and target typically at $10E-7$ BER without RS, interleaving and trellis), Maximum power spectral density for downstream, Maximum power for both up and downstream, Carrier mask (which tones are disabled), maximum interleaving delay.

Tones from number 8 to number 255 can be used: from 8 to 31 for upstream signals and from 32 to 255 for downstream signals. Numbers 16 and 64 are dedicated to pilot tones which are employed for synchronisation purposes between ATU-C and ATU-R ends. The software sets the use of tones for optimisation of performances.

At ATU-R, time recovery is carried out by the chip-set through the pilot tones. This activity is undertaken in two steps in order to achieve no more than 2ppm between ATU-C and ATU-R.

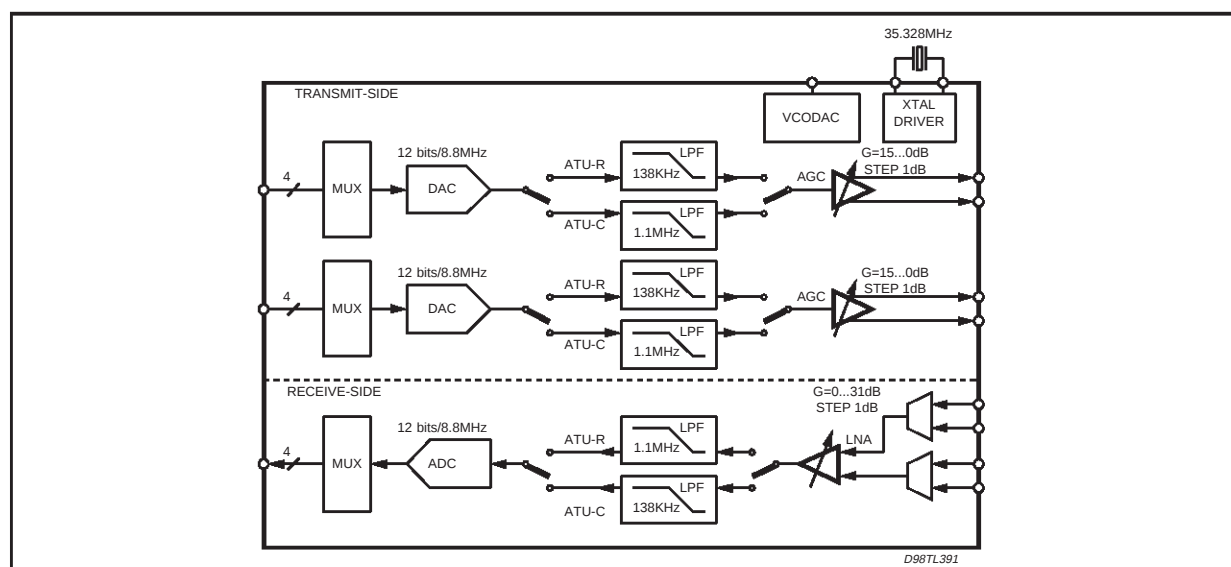
The transceiver controller software monitors line and channel. As far as line is concerned noise margin, attenuation, power, carrier load, relative capacity occupation are checked. Channel's monitoring deals with cell-delineation, actual ATM (fast and interleaved) up and downstream rates, achievable ATM DS and US rates (only at ATU-C side).

TOSCA ICs

TOSCA consists of an Analog Front End (STLC60134) and a Discrete Multitone Modem (STLC60135) integrated circuits which are produced by STMicroelectronics.

Here below we will briefly go through the main topics of both the ICs.

Figure 2. Analog Front End block diagram.



Analog Front End (STLC60134)

HCMOS5A (0.5 μ m) mixed digital and analog technology has been chosen to produce this component that embodies the analog functions of the TOSCA. Automatic gain control amplifiers, placed at the analog functions of the TOSCA. Automatic gain control amplifiers, placed at the analog interface of transmit and receive paths, allow for line's high attenuation in order to keep acceptable noise level of the signal ADC's and DAC's resolution, that is 12-bit wide with 8.8MHz sampling rate. Thanks to the symmetrical architecture the same channel filter can be used as a part of either the upstream or the downstream path: ATU-C or ATU-R end.

A built-in driver allows for single external clock generation using a XTAL (ATU-C) or a VCXO (ATU-R).

STLC60134 Analog Front End's main features:

- Rx automatic gain control: 0-31dB in 1dB steps
- Two input ports allow selection of RX signals, e.g. with or without external attenuation
- Second transmit port available (i.e. echo cancellation)
- Programmable low pass and band pass filters
- 12-bit DAC and ADC, sampling at 8.832MHz
- Xtal: 35.328MHz, ± 50 ppm, the accuracy of the frequency is determined by the External XTAL
- Direct connection to STLC60135 DTM modem
- Error correction on ADC output
- Test interface for digital and analog sections
- Analog and digital loop back modes

- Single 3.3V supply, or 3.3V analog and 3.0V digital supplies
- Power dissipation 0.4W
- Power-down mode 0.1W
- TQFP-64 (10 x 10mm body, 0.5mm pitch)

Discrete MultiTone Digital Modem (STLC60135)

The DMT modem has been developed in HCMOS6 (0.35 μ m) technology.

It performs PMD (Physycal Medium Dependant) sub-layer and TC (Transmission Convergence) sub-layer functions. In other words we can think to split up the chip into two separate blocks: the first one which carries out modem functions (PMD sub layer) and a second one in charge of ATM framing.

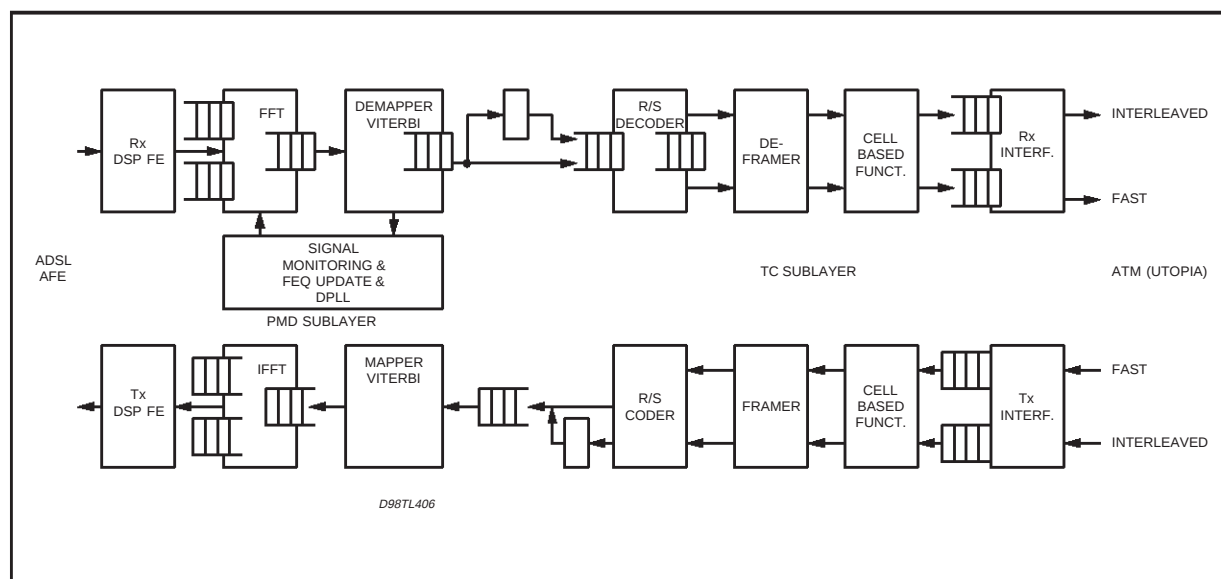
The chip is controlled and programmed by an external processor and is seen as a memory mapped device.

MODEM Functions

The modem part of the chip includes all the necessary blocks needed for digitally DMT mapping and demapping. A 14-bit code for every carrier allows constellations with up to 16383 points.

Internally digital filters carry out Time Equalization to reduce the effects of the inter symbol interfaces. That is followed by Fast Fourier Transform (in transmit direction an Inverse FFT is performed) in order to change from time domain to frequency domain. Afterwards a Frequency Equalization cuts down carrier by carrier the channel distortion; signal's amplitude attenuation and phase rotation. By efficient algorithms, this

Figure 3. DMT Modem block diagram.



block drives, through the STLC60134's integrated VCXO controller, the NT crystal oscillator which comes up in an excellent synchronisation (less than 2ppm) between ATU-C and ATU-R.

FRAMING Functions

STLC60135 performs framing functions for generic and ATM TC sub layers.

ATM TC sub layer performs cell level functions: delineation, idle cells or unassigned cells insertion/extraction, payload scrambling, Header Error Correction (HEC) check and data frame generation.

In order to comply with T1.413 Issue 2 rules and full interoperability with other manufacturers' modems (providing they guarantee compliance with either Issue 1 or Issue 2) framing features (such as interleaving and fast mode) are implemented with programmable parameters.

ATM frames can be bypassed in order to carry non-ATM bit streams, which makes the chip set very fit for applications using dedicated framing such as Frame-relay, etc.

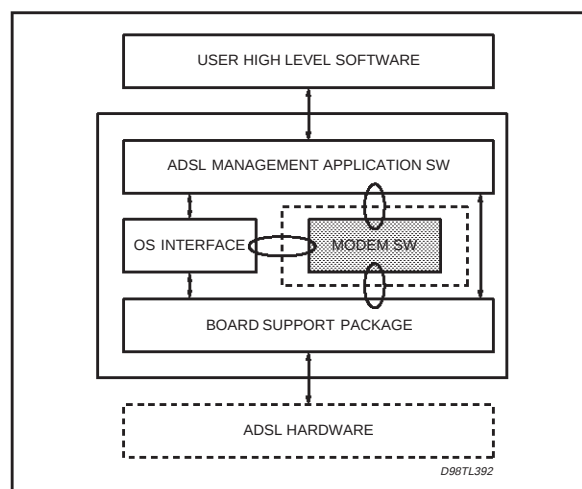
STLC60135 DTM modem main features:

- Time-domain equalisation
- Decimation, interpolation,
- FFT and IFFT, with different length and sampling rate at ATU-C and ATU-R side
- Rotor and frequency-domain equalisation
- Mapping/demapping
- Trellis coding and decoding using Viterbi algorithm
- Error and noise monitoring on individual tones
- Reed-Solomon encoding and decoding
- (De) framing and (de) interleaving
- Cell HEC generation/verification
- Payload (de) scrambling
- ATM cell insertion/extraction
- Idle &/or Unassigned cell insertion/filtering
- VPI/VCI filtering
- UTOPIA interface (Level 1 or 2)
- Microcontroller interface with 16-bit multiplexed address/data bus and big/little endian format supported
- JTAG test port
- Single 3.3V supply, 1.0W
- PQFP144 (28 x 28mm body, 0.65mm pitch)

ADSL Modem control software

The ADSL transceiver is based on a programmable DMT modem (STLC60135) whose configuration is loaded by an external controller.

Figure 4. Software Architecture.



Additionally the control functions, STMicroelectronics provides the DTM modem software. The software is written in C++ language, and is designed to be portable to any processor.

The driver has to be interfaced with a real time OS kernel, it is compatible with any standard product available on the market. The kernel manages the tasks dedicated to modem software.

The modem 5W core comes with three additional two software modules: a Board Support Package (BSP) and two Application Program Interfaces (API). BSP manages the hardware dependent features (i.e. interrupts, peripheral mapping).

APIs interface to the higher level application software and to the OS.

ADSL Loop performances

The hereafter tables show the performances that a system, which houses TOSCA, can achieve for ANSI and ETSI loops. The following results refer to an end-to end ADSLequipment with no external disturbance.

ANSI Loop (26awg)

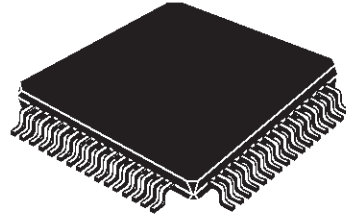
Length	Downstream	Upstream
9Kft	7.47 E +0.6	1.05 E +06
12Kft	3.69 E +0.6	9.37 E +05
15Kft	1.56 E +0.6	7.25 E +05

ETSI Loop (Loop 2, noise model A)

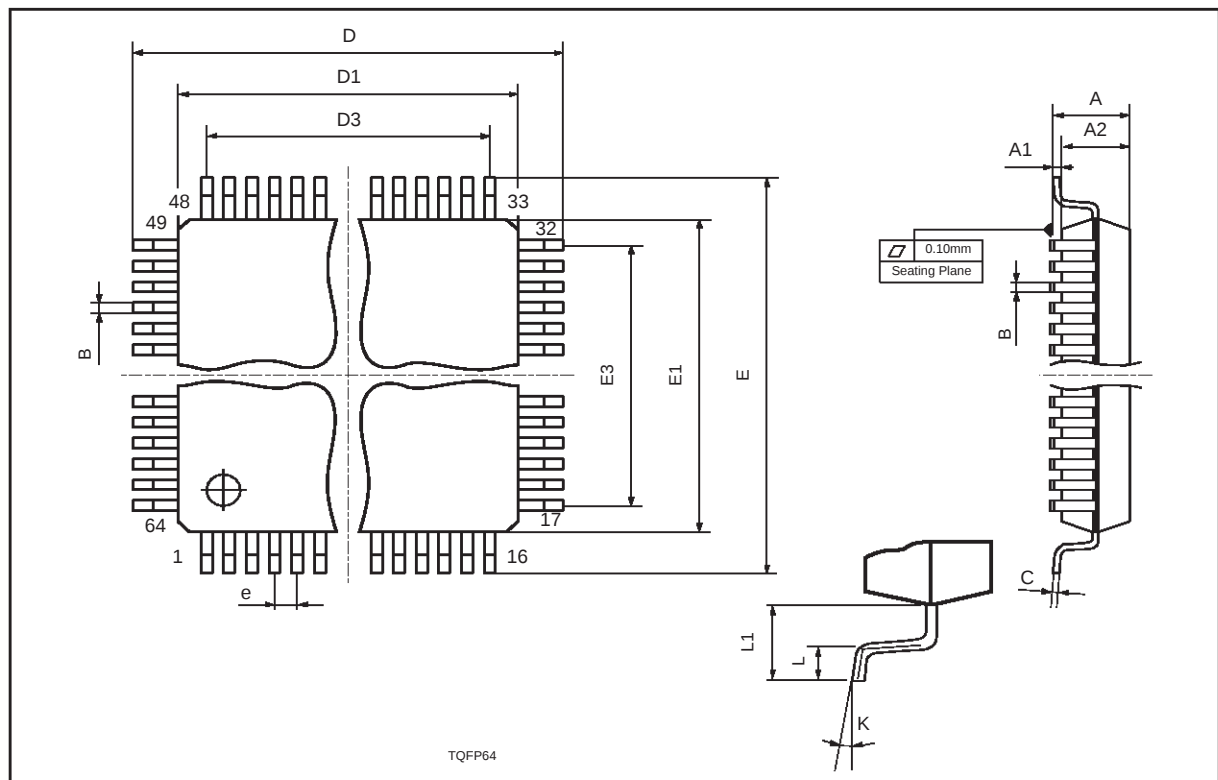
Length	Downstream	Upstream
2Km	8.00 E +0.6	8.32 E +05
4Km	4.07 E +0.6	6.72 E +05
5Km	1.70 E +0.6	4.72 E +05

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA

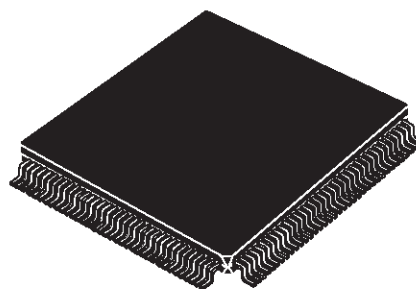


TQFP64

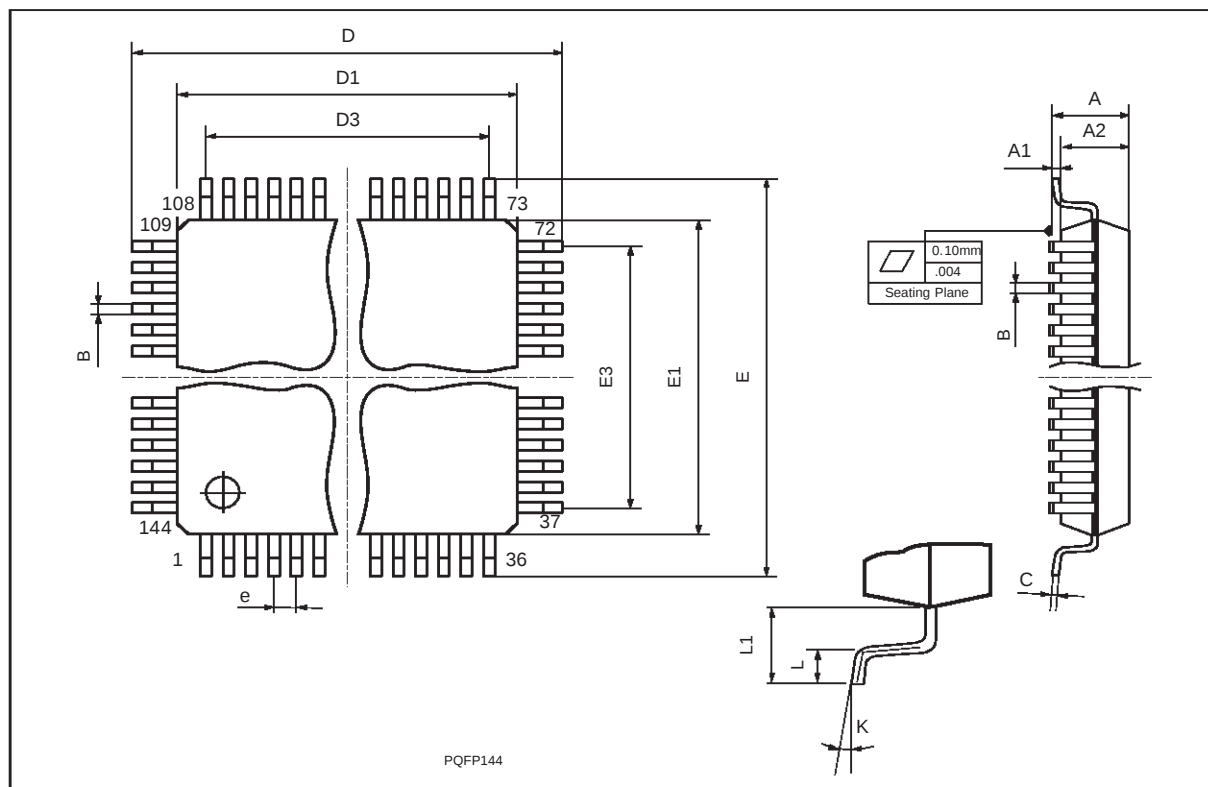


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.144
B	0.22		0.38	0.009		0.015
C	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.219	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		22.75			0.896	
e		0.65			0.026	
E	30.95	31.20	31.45	1.219	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		22.75			0.896	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



PQFP144



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