1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12-bit multiplying digital-to-analog converter designed for serial interface applications.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
–1	AD7543S(X)/883B
–2	AD7543T(X)/883B
–3	AD7543GT(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	V_{DD}
DGND to AGND	V_{DD}
Digital Input Voltage to DGND (Pins 4–11, 13)	−0.3V, +15V
V_{PIN1}, V_{PIN2} to AGND	−0.3V, +15V
V_{REF} to AGND	±25V
V_{RFB} to AGND	±25V
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-16 and E-20A
θ_{JA} = 120°C/W for Q-16 and E-20A

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Table 1.

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	−1, 2, 3	12					Bits
Relative Accuracy	RA	−1	1	1	1			± LSB max
		−2, 3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	−1	2	2	2		Monotonic to 11 Bit from T_{min} to T_{max}	± LSB max
		−2, 3	1	2	1	1	Monotonic to 12 Bit from T_{min} to T_{max}	
Gain Error[2]	AE	−1, 2	14.5	12.3	14.5			± LSB max
		−3	2	12.3	2	1		
Gain Tempco	TC_{AE}	−1, 2, 3	5					± ppm/°C max
Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	−1, 2, 3	0.01	0.005	0.01		ΔV_{DD} = ± 5%	± % per % max
Output Leakage Current I_{OUT1} (Pin 4)	I_{OUT1}	−1, 2, 3	200	± 10	200		DAC Registers Loads with All 0's	± nA max
I_{OUT2} (Pin 5)	I_{OUT2}	−1, 2, 3	200	± 10	200		DAC Register Loads with All 1's	
Output Current Settling Time	t_{SL}	−1, 2, 3	2				To ± 1/2LSB R_{OUT} 1 = 100Ω, C_{OUT1} = 13pF DAC. Output Measured from Falling Edge of $\overline{LD1}$ and $\overline{LD2}$.	μs max
Feedthrough Error[3]	FTE	−1, 2, 3	2.5				V_{REF} = 10V, 10kHz Sinewave	mV p-p max
Reference Input Resistance (Pin 15)	R_{IN}	−1, 2, 3	8	8	8			kΩ min
			25	25	25			kΩ max
Digital Input High Voltage	V_{IH}	−1, 2, 3	3.0	3.0	3.0			V min
Digital Input Low Voltage	V_{IL}	−1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	−1, 2, 3	1	1	1		V_{IN} = 0V or V_{DD}	± μA max
Digital Input Capacitance	C_{IN}	−1, 2, 3	8					pF max
Output Capacitance C_{OUT1} (Pin 1)	C_{OUT1}	−1, 2, 3	260				Digital Inputs = V_{IH}. DAC Register Loaded with 1111 1111 1111	pF max
C_{OUT2} (Pin 2)	C_{OUT2}	−1, 2, 3	75				Digital Inputs = V_{IH}. DAC Register Loaded with 1111 1111 1111	pF max
C_{OUT1} (Pin 1)	C_{OUT1}	−1, 2, 3	75				Digital Inputs = V_{IL}. DAC Register Loaded with 0000 0000 0000	pF max
C_{OUT2} (Pin 2)	C_{OUT2}	−1, 2, 3	260				Digital Inputs = V_{IL}. DAC Register Loaded with 0000 0000 0000	pF max
Serial Input to Strobe Setup Time[4]	t_{DS1}	−1, 2, 3	100				STB1 Used as a Strobe	ns min
	t_{DS4}	−1, 2, 3	0				STB4 Used as a Strobe	
	t_{DS3}	−1, 2, 3	0				STB3 Used as a Strobe	
	t_{DS2}	−1, 2, 3	40				STB2 Used as a Strobe	
Serial Input to Strobe Hold Time[4]	t_{DH1}	−1, 2, 3	70				STB1 Used as a Strobe	ns min
	t_{DH4}	−1, 2, 3	250				STB4 Used as a Strobe	
	t_{DH3}	−1, 2, 3	250				STB3 Used as a Strobe	
	t_{DH2}	−1, 2, 3	200				STB2 Used as a Strobe	
	t_{SR1}	−1, 2, 3	160				SR1 Data Pulse Width[4]	
	t_{STB1}	−1, 2, 3	160				STB1 Pulse Width[4]	
	t_{STB4}	−1, 2, 3	230				STB4 Pulse Width[4]	
	t_{STB3}	−1, 2, 3	230				STB3 Pulse Width[4]	
	t_{STB2}	−1, 2, 3	180				STB2 Pulse Width[4]	
	t_{LD1}, t_{LD2}	−1, 2, 3	300				Min Time Between Strobing LSB into Register A and Loading Register B[4]	
	t_{ASB}	−1, 2, 3	80				Min Time Between Strobing LSB into Register A and Loading Register B[4]	
	t_{CLR}	−1, 2, 3	400				CLK Pulse Width[4]	

NOTES
[1] V_{DD} = +5V; V_{OUT1} = V_{OUT2} = 0V, V_{REF} = +10V unless otherwise stated.
[2] Measured using internal feedback resistor and includes the effect of 5ppm max gain TC.
[3] Feedthrough can be further reduced by connecting the metal lid to ground.
[4] Timing per Figure 1.

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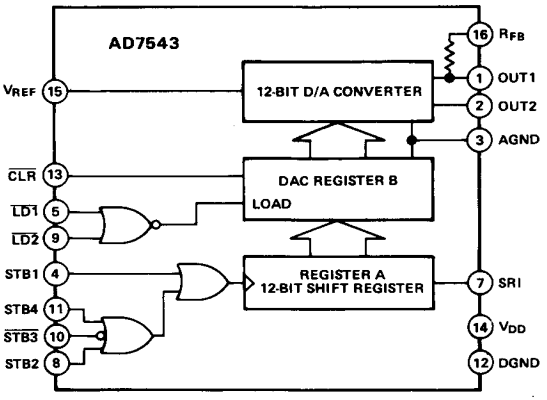
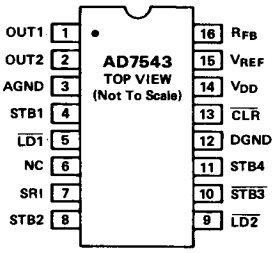
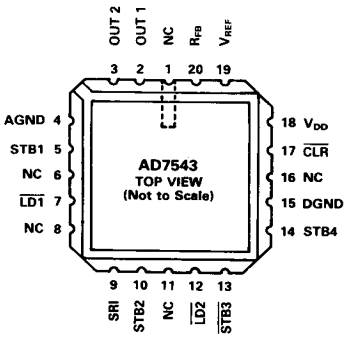
3.2.1 Functional Block Diagram and Terminal Assignments.



DIP (Q) Package



LCC (E) Package

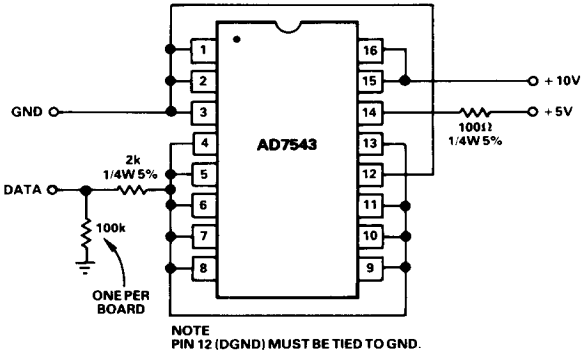


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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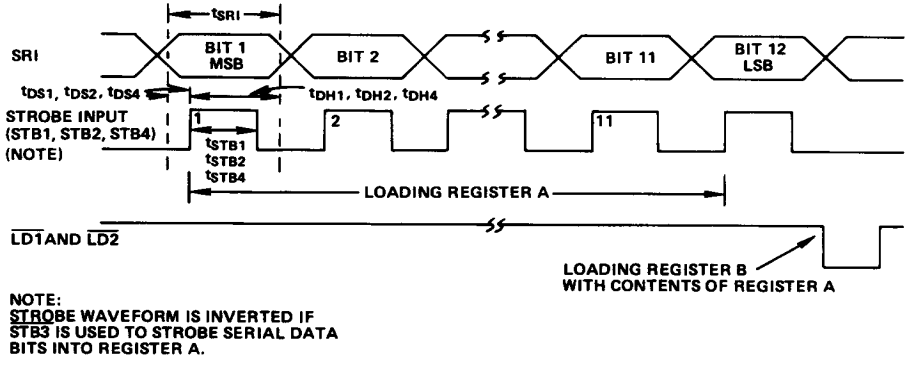

Figure 1. Timing Diagram

Table 2. Truth Table

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↑	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1	↑	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	↓	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
↑	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↑ is positive edge ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

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