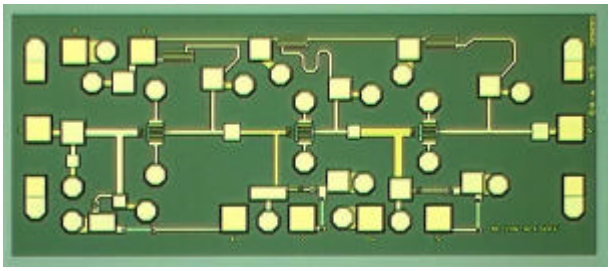
HEMT LNA
37-42GHz



Features

- 20dB gain
- 3 dB Noise Figure

Description

This datasheet shows the performance of a 37 – 42GHz Gallium Arsenide Low Noise Amplifier. This product is intended for use in fixed-point and point to point microwave systems. The LNA has a single drain supply, with access to each of the gates to enable customer optimization.

The die is fabricated using Caswell Technology's 0.20µm gate length, pHEMT process and is fully protected using Silicon Nitride passivation for excellent performance and reliability.

Electrical Performance

Ambient Temperature 22 ±3 °C, Z_O = 50Ω, Vdd=2V, Vg1 & 2 set for Id1/2=12mA, Vg3 set for Id3=20mA U.O.S

Parameter	Conditions	Min	Typ	Max	Units
Small Signal Gain	37 – 40GHz	18	20		dB
Input Return Loss	37 – 40GHz	6	10		dB
Output Return Loss	37 – 40GHz	6	10		dB
Noise Figure	37 – 40GHz		3	4	dB
Stage 1 Drain Current	By adjustment of Vg1		12		mA
Stage 2 Drain Current	By adjustment of Vg2		12		mA
Stage 3 Drain Current	By adjustment of Vg3		20		mA
P1dB	38GHz		8		dBm
IP3	38GHz		20		dBm

Notes

All parameters measured on wafer

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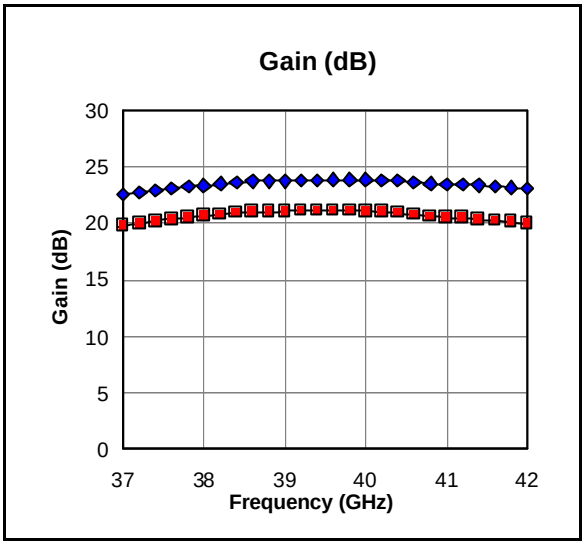
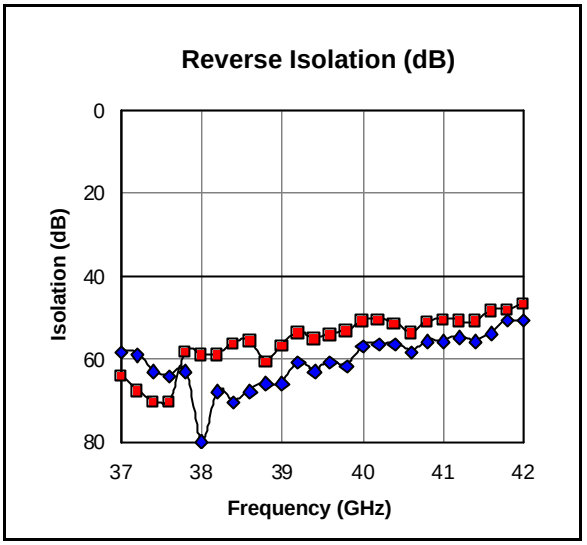
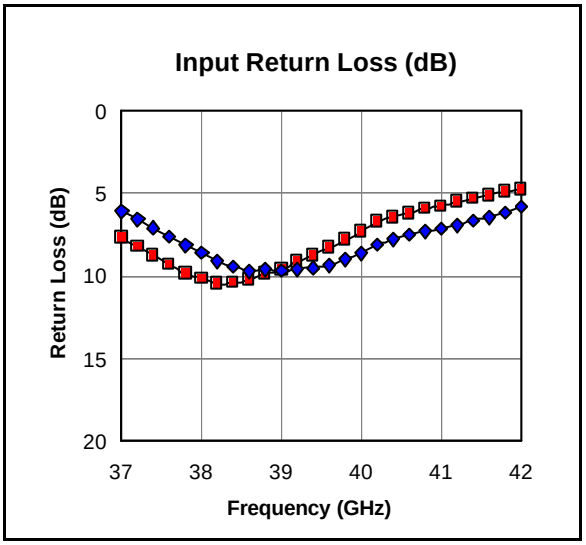
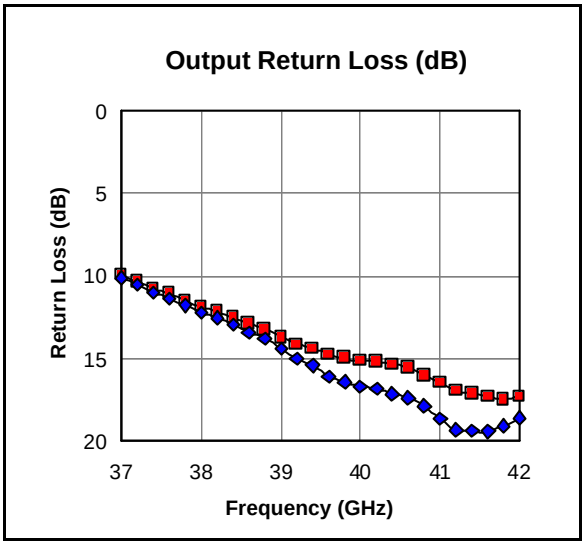
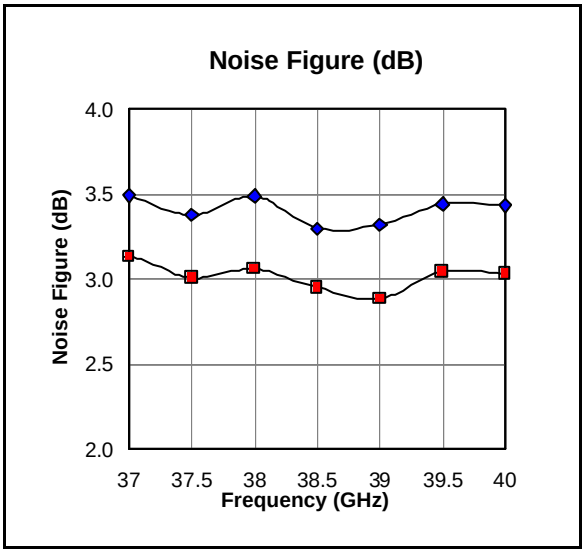
RFOW Performance (Vd Id1,Id2,Id3) (2V,12mA,12mA,20mA) (2V,20mA,20mA,20mA)











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Typical S-parameters (RFOW) (Vd=2V ,Id1 & 2=12mA, Id3=20mA)

Frequency	S11		S21		S12		S22	
(GHz)	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
37	0.50	33.4	13.46	11.5	0.0012	-38.9	0.31	132.7
37.2	0.47	32	13.74	5.4	0.0011	-50	0.30	130.2
37.4	0.44	31	13.99	-0.9	0.0007	12.2	0.28	128.6
37.6	0.42	29.5	14.26	-7.5	0.0006	-29.3	0.27	127.4
37.8	0.39	30	14.50	-14.1	0.0007	-76.3	0.26	126.2
38	0.37	30.8	14.68	-20.8	0.0001	177.4	0.24	125.1
38.2	0.35	32.2	14.95	-27.6	0.0004	35.4	0.24	125
38.4	0.34	34.4	15.10	-34.4	0.0003	-1.1	0.22	123.2
38.6	0.33	37.1	15.31	-41	0.0004	25.4	0.21	122.4
38.8	0.33	39.6	15.31	-48.1	0.0005	41.6	0.20	120.3
39	0.33	41.5	15.31	-54.8	0.0005	48.3	0.19	119.2
39.2	0.33	42.8	15.43	-61.2	0.0009	70.1	0.18	118.4
39.4	0.33	45.1	15.52	-67.9	0.0007	86.6	0.17	117.8
39.6	0.34	47.2	15.58	-74.4	0.0009	98.6	0.16	118.7
39.8	0.35	46.6	15.59	-81.2	0.0008	121.2	0.15	119.9
40	0.37	47.5	15.56	-88.1	0.0014	96.5	0.15	121.6
40.2	0.39	47.3	15.51	-94.8	0.0015	81.9	0.14	122.4
40.4	0.41	46.7	15.44	-101.6	0.0015	61.9	0.14	122.3
40.6	0.42	45.1	15.21	-108.3	0.0012	89.3	0.14	121.8
40.8	0.43	43.6	14.99	-114.6	0.0016	91.7	0.13	124
41	0.44	43.4	14.81	-120.4	0.0016	86.3	0.12	123.1
41.2	0.45	41.6	14.79	-126.5	0.0018	95.6	0.11	127
41.4	0.47	40.3	14.74	-132.7	0.0016	92.7	0.11	131.5
41.6	0.48	37.5	14.55	-139.2	0.002	98.7	0.11	134.5
41.8	0.49	35	14.33	-145.5	0.0029	73.5	0.11	139
42	0.51	31.9	14.26	-151.8	0.0029	59.3	0.12	141

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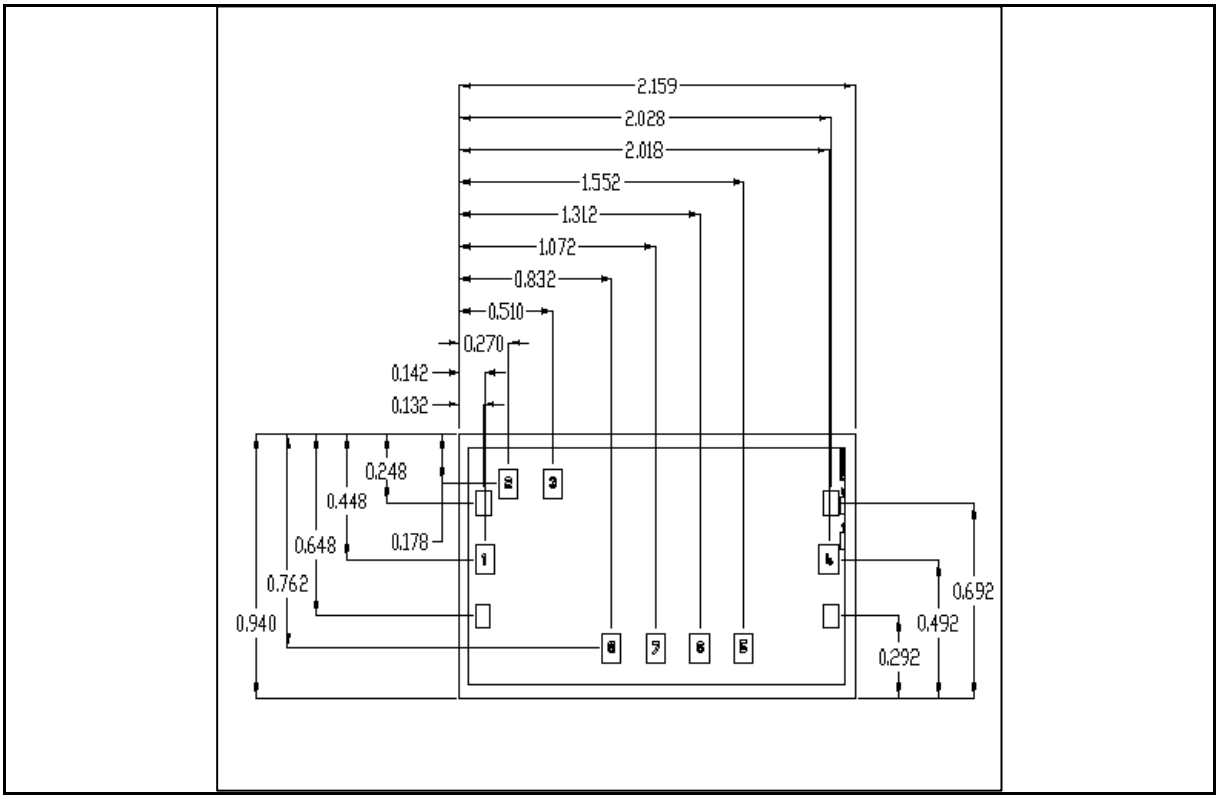
Chip Outline



Die size: 2.16 x 0.94mm
RF bond pads (1 & 4): 120µm x 120µm
All other bond pads: 120µm x 120µm
Die Thickness: 100µm

Pad Details

Pad	Function
1	RF Input
2	N/C
3	Vdd
4	RF Output
5	Vg3
6	N/C
7	Vg2
8	Vg1

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Handling and Assembly Information

Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Dice are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

GaAs Products from Caswell Technology's pHEMT Foundry process are 100µm thick and have through GaAs vias to enable grounding to the circuit. Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die.

The surface to which the die are to be attached should be cleaned with a proprietary de-greasing cleaner.

Conductive epoxy mounting is recommended. Recommended epoxies are Ablestick 84-1LMI or 84-1LMIT cured at 150°C for 1 hour in a nitrogen atmosphere. The epoxy should be applied sparingly to avoid encroachment of the epoxy on to the top surface of the die. An epoxy fillet should be visible around the total die periphery.

Eutectic mounting can be used and entails the use of a gold-tin (AuSn) preform, approximately 0.001″ thick, placed between the die and the attachment surface. The preferred method of mounting is the use of a machine such as a Mullins 8-140 die bonder. This utilises a heated collet and workstation with a facility for applying a scrubbing action to ensure total wetting and avoid the formation of voids. Dry nitrogen gas is directed across the work piece.

The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280°C (Note: Gold Germanium with a higher melting temperature should be avoided, in particular for MMICs). The work station temperature should be 310°C ± 10°C. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. The strength of the bonding formed by this method will result in fracture of the die, rather than the bond under die strength testing.

The P35-5117-000-200 amplifier die has gold bond pads. The recommended wire bonding procedure uses 25µm (0.001") 99.99% pure gold wire with 0.5-2% elongation. Thermo-compression wedge bonding is preferred though thermosonic wire bonding may be used providing the ultrasonic content of the bond is minimised. A work station temperature of 260°C ± 10°C with a wedge tip temperature of 120°C ± 10°C is recommended. The wedge force should be 45 ± 5 grams. Bonds should be made from the bond pads on the die to the package or substrate.

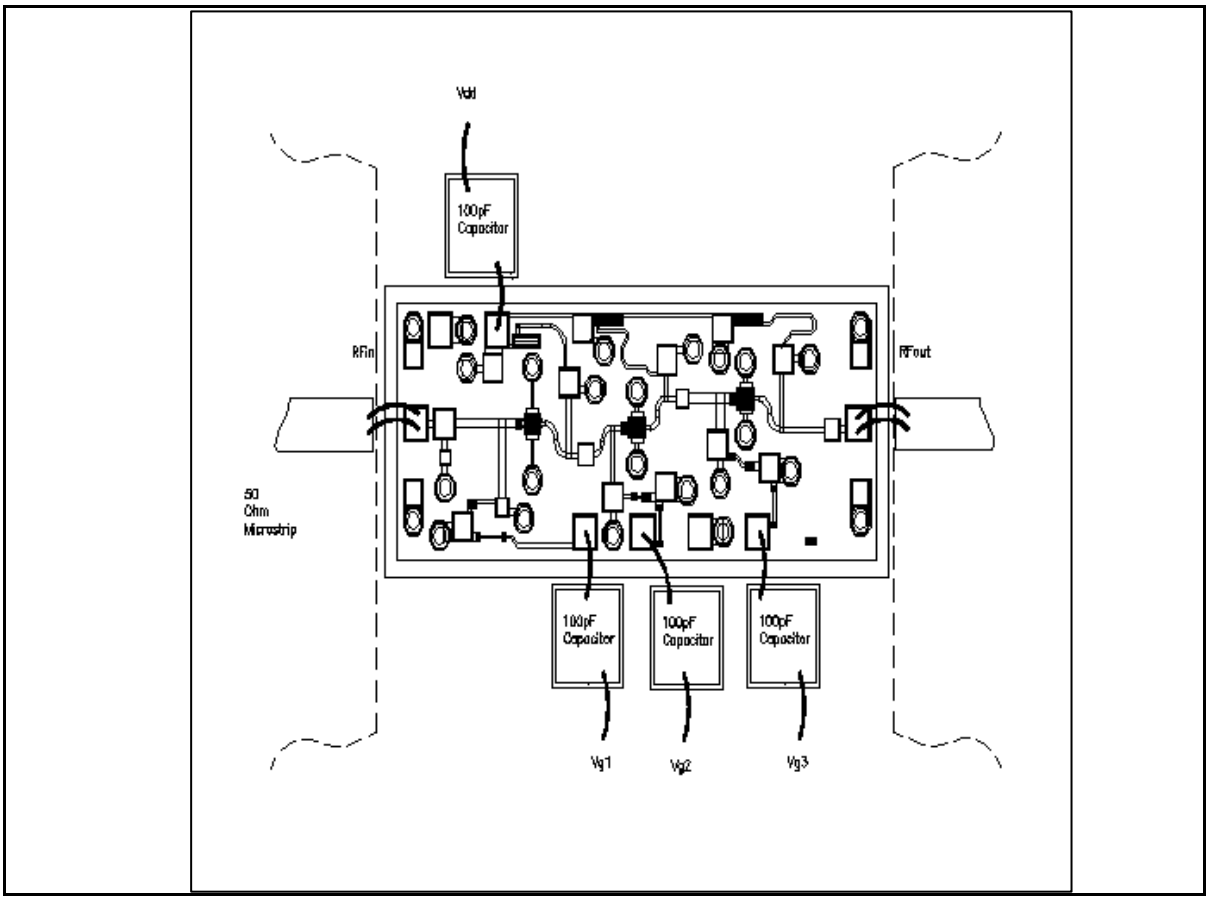
The RF bond pads at the input and output are 120µm x 120µm; all other bond pads are 120µm x 120µm.

The P35-5117-000-200 has been designed to include the inductance of two 25µm bond wires at both the input and output, facilitating the integration of the die into a 50Ω environment, these should be kept to a minimum length.

Operating and Biasing of the P35-5117-000-200

The P35-5117-000-200 is a three-stage low noise amplifier. The drain biases for all three stages (Vd1, Vd2 & Vd3) are linked on chip and 2 volts should be connected to Vdd. The gate voltages (Vg1, Vg2 & Vg3) are set to give 12mA of drain current in each of the first two stages and 20mA in the third stage drain. The separate gate voltage supplies for all stages can be combined into single supply (Vgg). DC bias supplies should be decoupled to ground using 100pF chip capacitors placed close to the chip with short bondwires to the amplifier bond pads.

Typical bonding detail



Absolute maximum Ratings

Max Vdd	+5V
Max Vgg	-2V
Max channel temperature	150°C
Storage temperature	-65°C to +150°C

Ordering Information

P35-5117-000-200