

LH538500A

**CMOS 8M (1M × 8 / 512K × 16)
Mask-Programmable ROM**

FEATURES

- 1,048,576 × 8 bit organization
(Byte mode)
- 524,288 × 16 bit organization
(Word mode)
- BYTE input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Power consumption:
Operating: 275 mW (MAX.)
Standby: 550 μW (MAX.)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
42-pin, 600-mil DIP
44-pin, 600-mil SOP
44-pin, 14 × 14 mm² QFP
64-pin, 14 × 20 mm² QFP
48-pin, 12 × 18 mm² TSOP (Type I)
- X16 word-wide pinout

DESCRIPTION

The LH538500A is a mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by BYTE input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

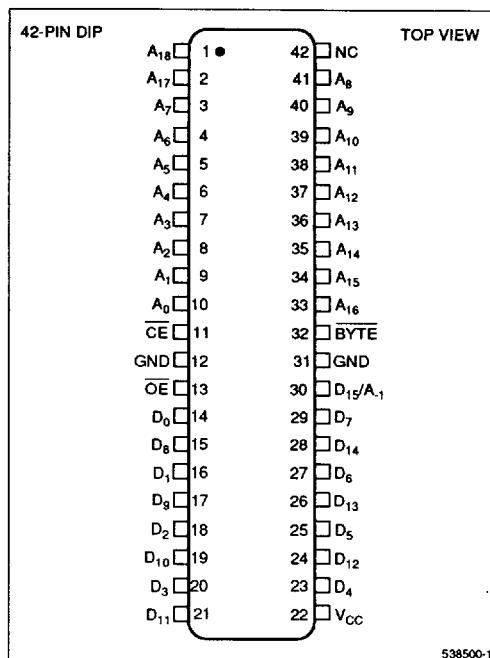


Figure 1. Pin Connections for DIP Package

SHARP CORP

61E D 8180798 0009942 123 SRPJ

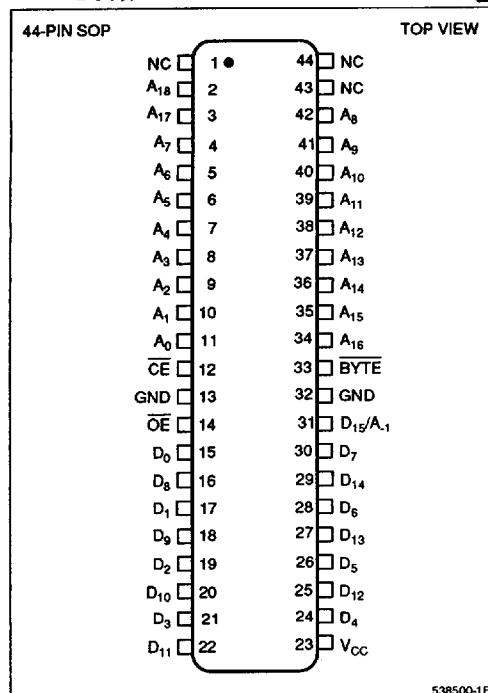


Figure 2. Pin Connections for SOP Package

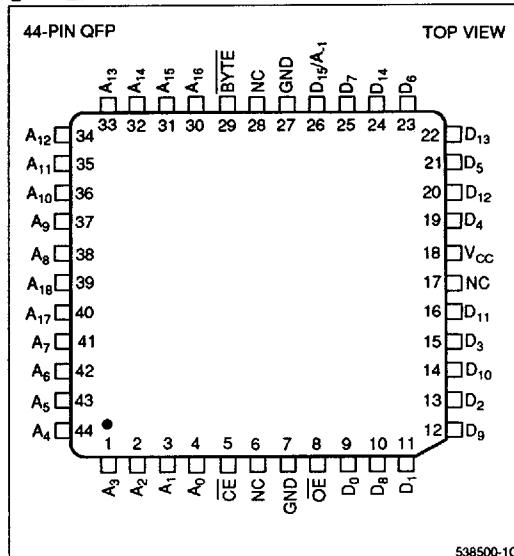


Figure 3. Pin Connections for 44-Pin QFP Package

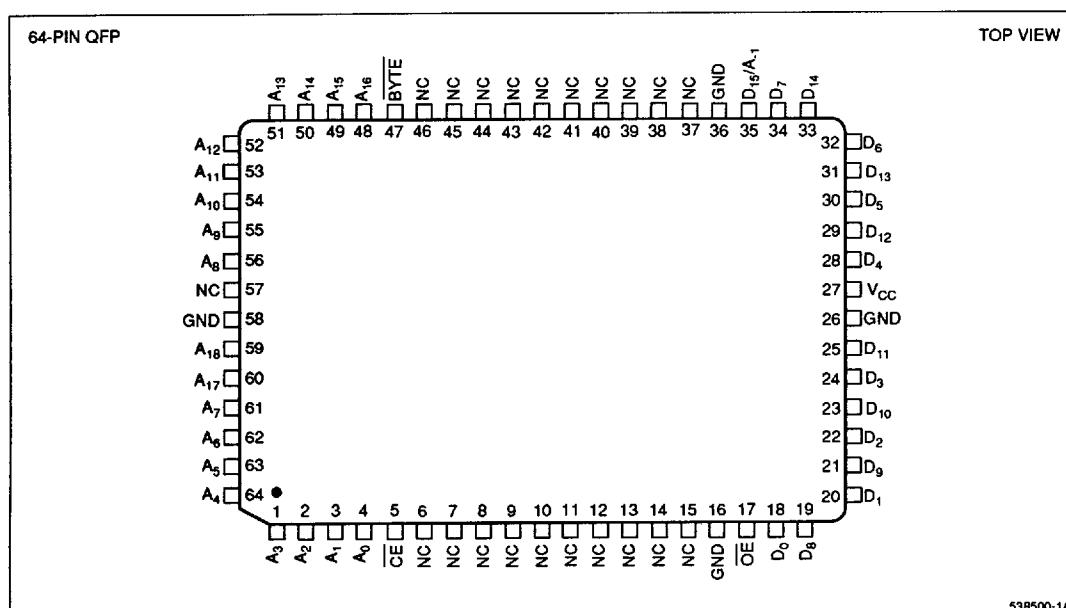


Figure 4. Pin Connections for 64-Pin QFP Package

SHARP CORP

61E D ■ 8180798 0009943 06T ■ SRPJ

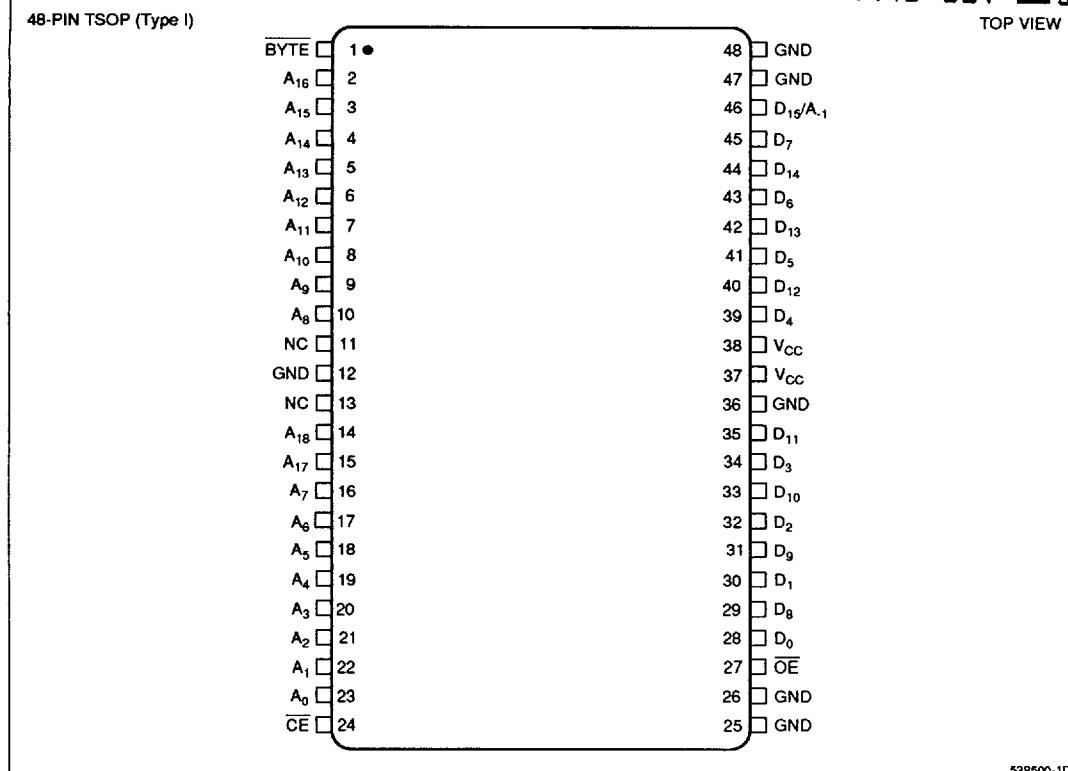


Figure 5. Pin Connections for TSOP Package

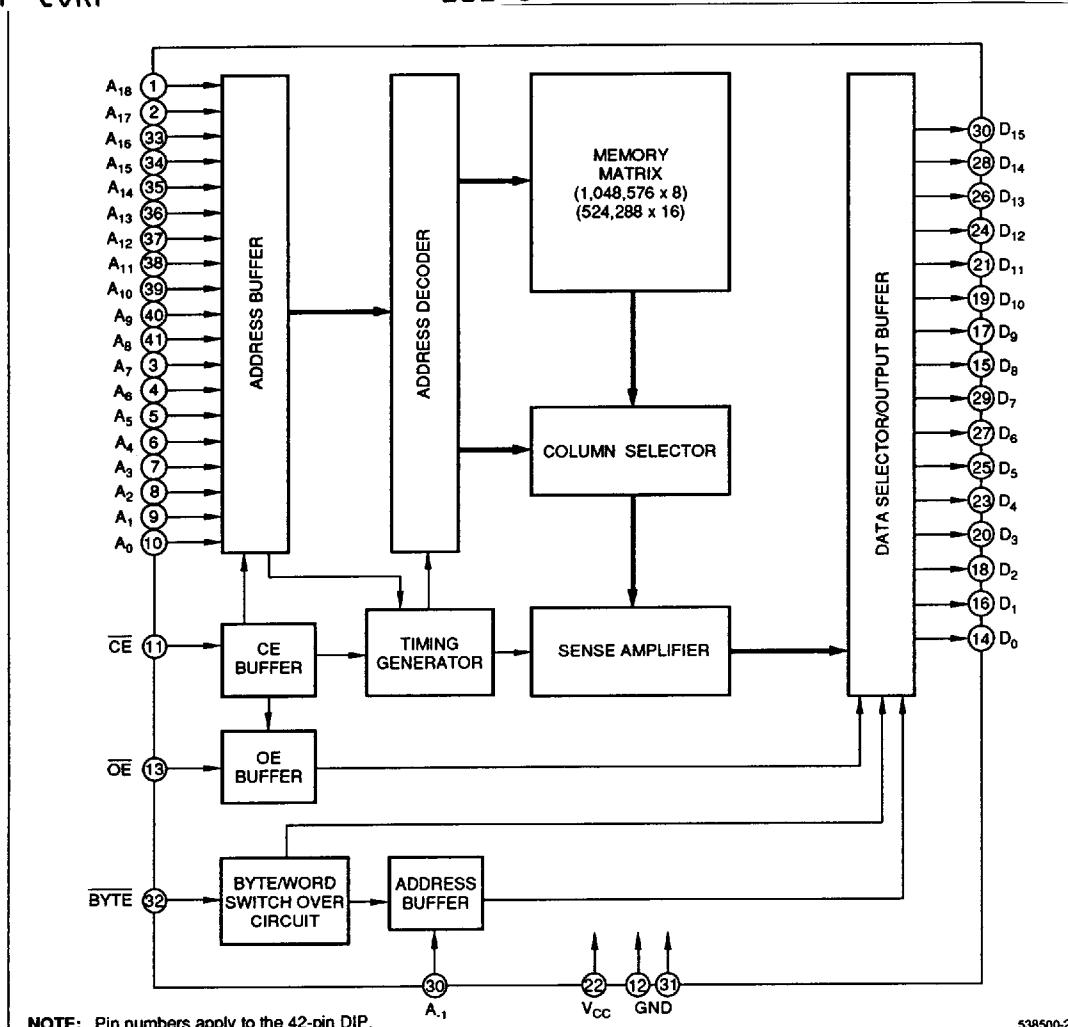


Figure 6. LH538500A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₁	Address input (Byte mode)	1
A ₀ - A ₁₈	Address input	
D ₀ - D ₁₅	Data output	
CE	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE	Output Enable input	
BYTE	Byte/word switch	
V _{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D₁₅/A₁ pin becomes LSB address input (A₋₁) when the bit configuration is set to byte mode, and data output (D₁₅) when in word mode. BYTE input pin selects bit configuration.

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61E D ■ 8180798 0009945 932 ■ SRPJ

TRUTH TABLE

CE	OE	BYTE *	A-1	MODE	D ₀ - D ₇	D ₈ - D ₁₅	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I _{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I _{CC})	
L	L	H	Input inhibit	Word	D ₀ - D ₇	D ₈ - D ₁₅	Operating (I _{CC})	
L	L	L	L	Byte	D ₀ - D ₇	High-Z	Operating (I _{CC})	
L	L	L	H	Byte	D ₈ - D ₁₅	High-Z	Operating (I _{CC})	

NOTE:

1. X = H or L

* BYTE input state must be set to H or L and must not be changed during operation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V	
Output voltage	V _{OUT}	-0.3 to V _{CC} +0.3	V	
Operating temperature	T _{OPR}	0 to +70	°C	
Storage temperature	T _{STG}	-55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'Low' voltage	V _{IL}		-0.3	0.8	V	
Input 'High' voltage	V _{IH}		2.2	V _{CC} +0.3	V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA		0.4	V	
Output 'High' voltage	V _{OH}	I _{OH} = -400 μA	2.4		V	
Input leakage current	I _{LI}	V _{IN} = 0 V or V _{CC}		10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V or V _{CC}		10	μA	1
Operating current	I _{CC1}	t _{RC} = 150 ns		50	mA	2
	I _{CC2}	t _{RC} = 1 μs		40		
Standby current	I _{SB1}	CE = V _{IH}		3	mA	
	I _{SB2}	CE = V _{CC} - 0.2 V		100	μA	

NOTES:

1. CE/OE = V_{IH}
 2. V_{IN} = V_{IH}/V_{IL}, CE = V_{IL}, outputs open

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AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t _{RC}	150		ns	
Address access time	t _{AA}		150	ns	
Chip enable time	t _{ACE}		150	ns	
Output enable time	t _{OE}		70	ns	
Output hold time	t _{OH}	5		ns	
CE to output in High-Z	t _{CHZ}		70	ns	1
OE to output in High-Z	t _{OHZ}		70	ns	

NOTE:

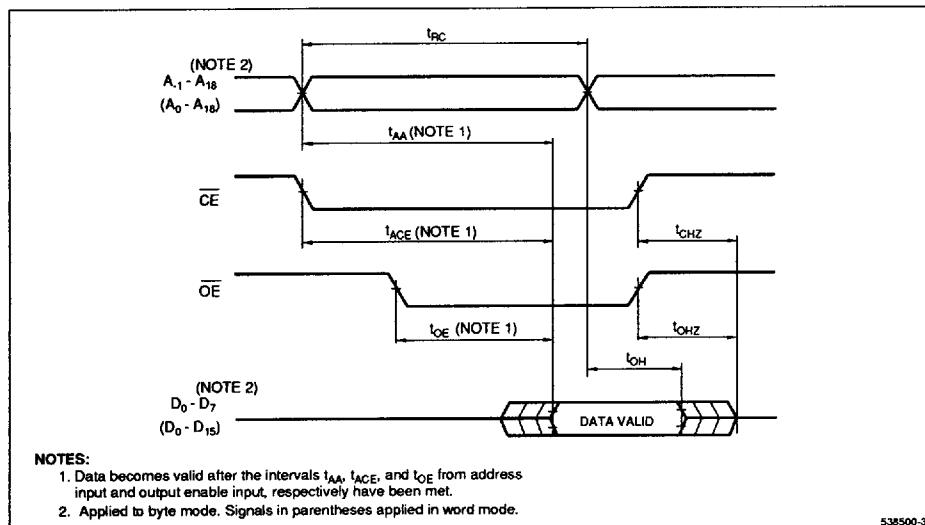
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1 TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C _{IN}			10	pF
Output capacitance	C _{OUT}			10	pF

**Figure 7. Timing Diagram****CAUTION**

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

**SHARP CORP
ORDERING INFORMATION**

61E D ■ 8180798 0009947 705 ■ SRPJ

LH538500A
Device TypeX
Package- ##
Speed

15 150 Access Time (ns)

D 42-pin, 600-mil DIP (DIP42-P-600)

Z 44-pin, 14 x 14 mm² QFP (QFP44-P-1414)M 64-pin, 14 x 20 mm² QFP (QFP64-P-1420)

N 44-pin, 600-mil SOP (SOP44-P-600)

T 48-pin, 12 x 18 mm² TSOP (Type I) (TSOP48-P-1218)

CMOS 8M (1M x 8 or 512K x 16) Mask Programmable ROM

Example: LH538500AD-15 (CMOS 8M Mask Programmable ROM, 150 ns, 42-pin, 600-mil DIP)

538500-4