LH534500A

CMOS 4M (512K × 8 / 256K × 16)
Mask-Programmable ROM

FEATURES

- Memory organization selection:
  524,288 × 8 bit (byte mode)
  262,144 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- Automatic power down mode
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  44-pin, 14 × 14 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH534500A is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

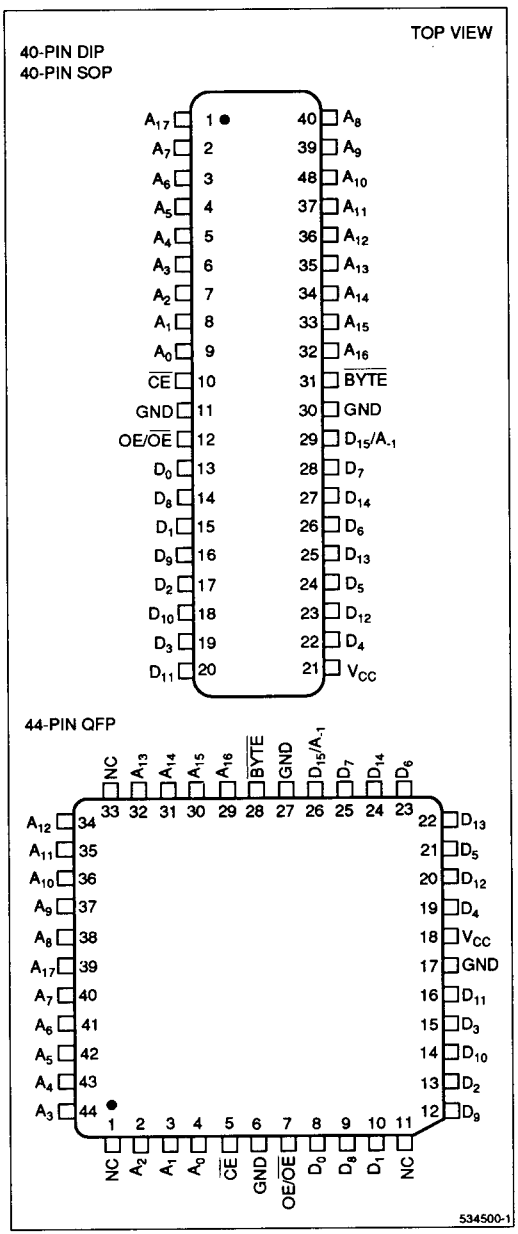


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

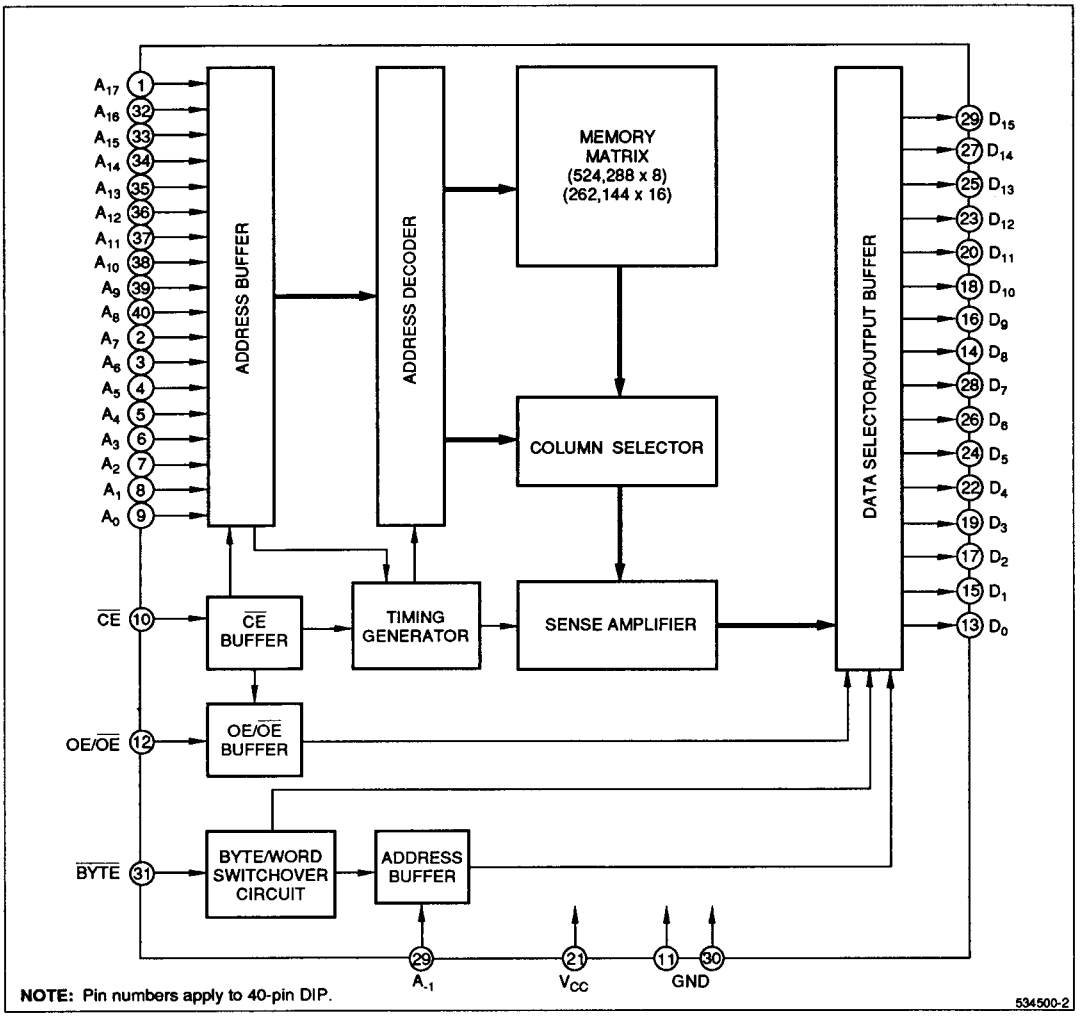


Figure 2. LH534500A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Chip Enable input	2
$\overline{BYTE}$	Byte/word mode switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. Active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	L/H	X	X	Non selected	High-Z		Operating (I_{CC})
L	H/L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	H/L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	H/L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:

X = High or Low

The input state of $\overline{BYTE}$ must not be changed during operation. The $\overline{BYTE}$ pin must be set to either High or Low.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			5	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:

1. OE = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable delay time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

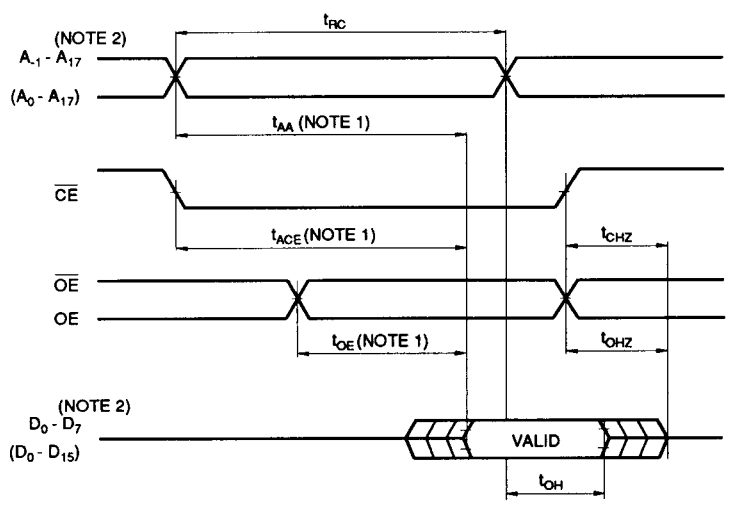
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input, chip enable, and output enable, respectively have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

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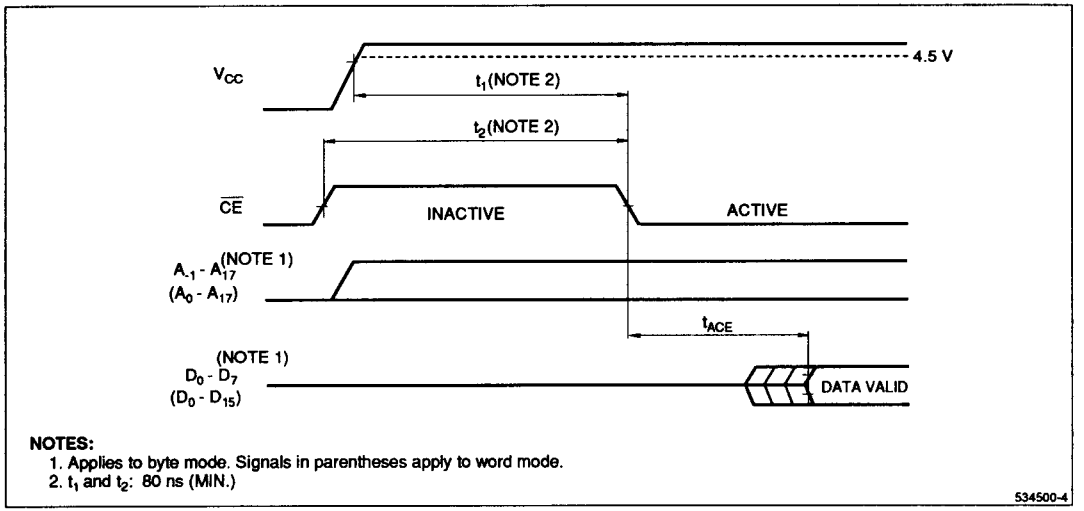
Figure 3. Timing Diagram



NOTES:
1. Applies to byte mode. Signals in parentheses apply to word mode.
2. t_1 and t_2: 80 ns (MIN.)

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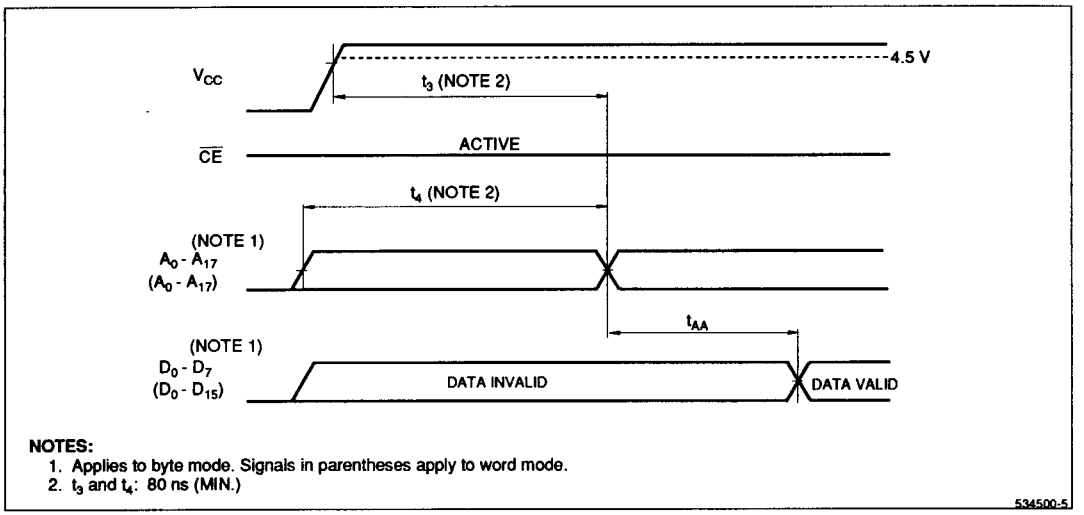
Figure 4. Timing Diagram (Power On With $\overline{CE}$ Inactive)



NOTES:
1. Applies to byte mode. Signals in parentheses apply to word mode.
2. t_3 and t_4: 80 ns (MIN.)

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Figure 5. TIming Diagram (Power On With $\overline{CE}$ Active)

ORDERING INFORMATION