

Complementary Silicon Power Transistors

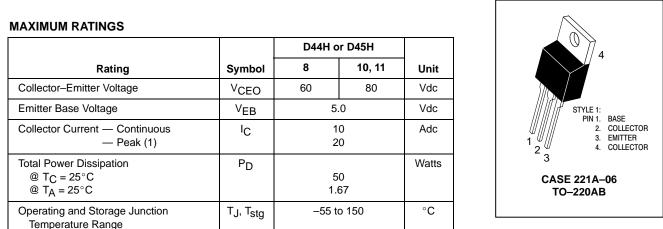
... for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage V_{CE(sat)} = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

NPN D44H Series* PNP D45H Series*

*ON Semiconductor Preferred Device

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60, 80 VOLTS



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	TL	275	°C

⁽¹⁾ Pulse Width \leq 6.0 ms, Duty Cycle \leq 50%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain (V _{CE} = 1.0 Vdc, I _C = 2.0 Adc)	D44H10 D45H10	hFE	35	_	_
	D44H8,11 D44H8,11		60	_	
(V _{CE} = 1.0 Vdc, I _C = 4.0 Adc)	D44H10 D45H10		20	_	
	D44H8,11 D45H8,11		40	_	

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

D44H Series D45H Series

ELECTRICAL CHARACTERISTICS ($T_C = 25$ °C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Collector Cutoff Current (VCE = Rated VCEO, VBE = 0)		ICES	_	_	10	μΑ
Emitter Cutoff Current (VEB = 5.0 Vdc)		I _{EBO}	_	_	100	μΑ
ON CHARACTERISTICS						
Collector–Emitter Saturation Voltage (I _C = 8.0 Adc, I _B = 0.4 Adc) (I _C = 8.0 Adc, I _B = 0.8 Adc)	D44H/D45H8,11 D44H/D45H10	VCE(sat)	_	_	1.0 1.0	Vdc
Base–Emitter Saturation Voltage (I _C = 8.0 Adc, I _B = 0.8 Adc)		V _{BE(sat)}	_	_	1.5	Vdc
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V _{CB} = 10 Vdc, f _{test} = 1.0 MHz)	D44H Series D45H Series	C _{cb}		130 230	_ _	pF
Gain Bandwidth Product (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f = 20 MHz)	D44H Series D45H Series	fΤ	_	50 40		MHz
SWITCHING TIMES						
Delay and Rise Times (I _C = 5.0 Adc, I _{B1} = 0.5 Adc)	D44H Series D45H Series	t _d + t _r	_	300 135		ns
Storage Time ($I_C = 5.0$ Adc, $I_{B1} = I_{B2} = 0.5$ Adc)	D44H Series D45H Series	t _S	_	500 500		ns
Fall Time (I _C = 5.0 Adc, I _{B1} = 102 = 0.5 Adc)	D44H Series D45H Series	tf		140 100	_ _	ns

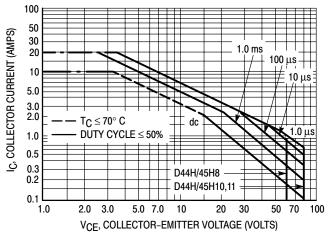
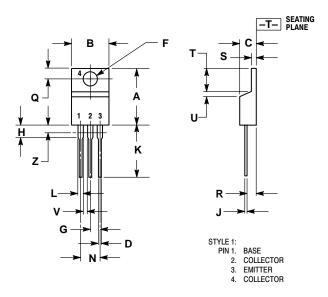


Figure 1. Maximum Rated Forward Bias Safe Operating Area

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PACKAGE DIMENSIONS

TO-220 **CASE 221A-09 ISSUE AA**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.570	0.620	14.48	15.75	
В	0.380	0.405	9.66	10.28	
c	0.160	0.190	4.07	4.82	
D	0.025	0.035	0.64	0.88	
F	0.142	0.147	3.61	3.73	
G	0.095	0.105	2.42	2.66	
Н	0.110	0.155	2.80	3.93	
7	0.018	0.025	0.46	0.64	
K	0.500	0.562	12.70	14.27	
L	0.045	0.060	1.15	1.52	
N	0.190	0.210	4.83	5.33	
Q	0.100	0.120	2.54	3.04	
R	0.080	0.110	2.04	2.79	
S	0.045	0.055	1.15	1.39	
Т	0.235	0.255	5.97	6.47	
5	0.000	0.050	0.00	1.27	
٧	0.045		1.15		
Z		0.080		2.04	

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