

# LH5116

CMOS 16K (2K × 8) Static RAM

## FEATURES

- 2,048 × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:  
Operating: 220 mW (MAX.)  
Standby: 5.5  $\mu$ W (MAX.)
- Single +5 V power supply
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available  
LH5116H: -40 to +85°C
- Packages:  
24-pin, 600-mil DIP  
24-pin, 300-mil SK-DIP  
24-pin, 450-mil, SOP
- Compatible with 16K EPROM and mask ROM pinout

## DESCRIPTION

The LH5116 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It features high speed access in read mode using output enable ( $t_{OE}$ ).

## PIN CONNECTIONS

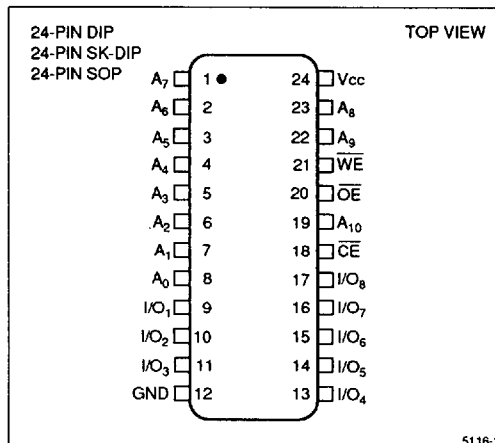


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

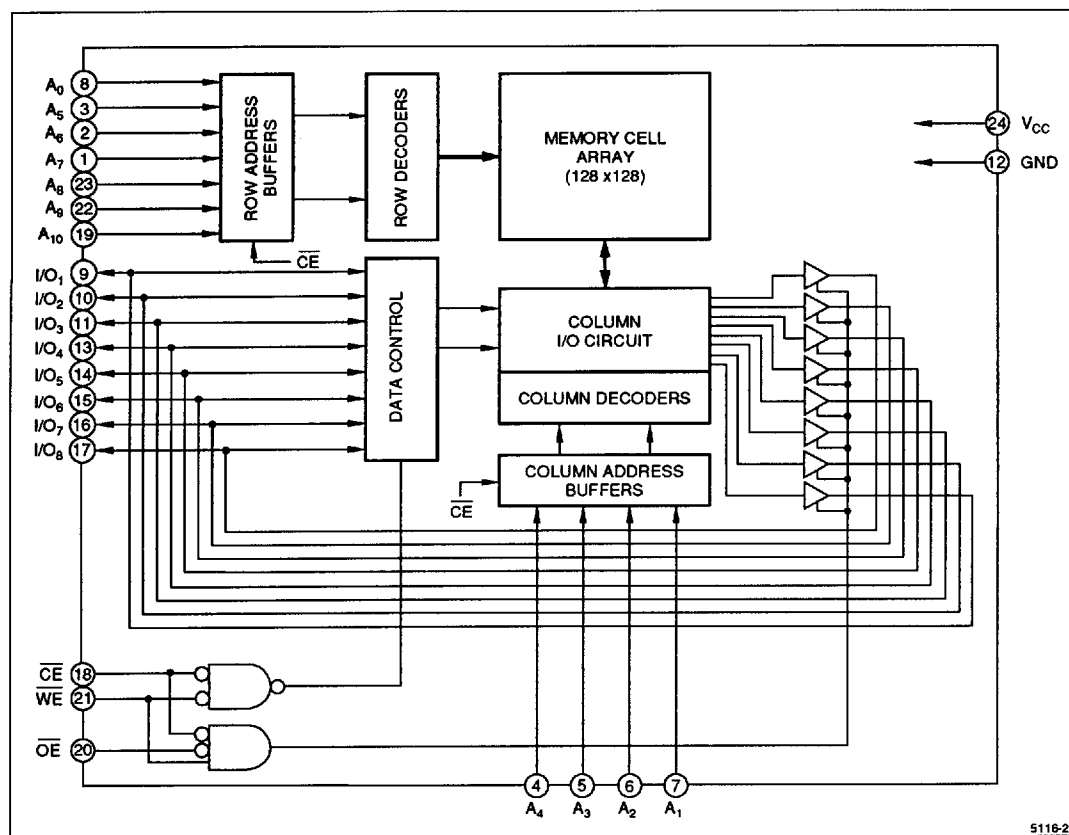


Figure 2. LH5116 Block Diagram

## PIN DESCRIPTION

| SIGNAL                           | PIN NAME            |
|----------------------------------|---------------------|
| A <sub>0</sub> - A <sub>10</sub> | Address input       |
| $\overline{CE}$                  | Chip Enable input   |
| $\overline{OE}$                  | Output Enable input |
| $\overline{WE}$                  | Write Enable input  |

| SIGNAL                              | PIN NAME          |
|-------------------------------------|-------------------|
| I/O <sub>1</sub> - I/O <sub>8</sub> | Data input/output |
| V <sub>CC</sub>                     | Power supply      |
| GND                                 | Ground            |

## TRUTH TABLE

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | MODE            | I/O <sub>1</sub> - I/O <sub>8</sub> | SUPPLY CURRENT               | NOTE |
|-----------------|-----------------|-----------------|-----------------|-------------------------------------|------------------------------|------|
| L               | X               | L               | Write           | D <sub>IN</sub>                     | Operating (I <sub>CC</sub> ) | 1    |
| L               | L               | H               | Read            | D <sub>OUT</sub>                    | Operating (I <sub>CC</sub> ) |      |
| H               | X               | X               | Deselect        | High-Z                              | Standby (I <sub>SB</sub> )   | 1    |
| L               | H               | X               | Outputs disable | High-Z                              | Operating (I <sub>CC</sub> ) | 1    |

## NOTE:

1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER             | SYMBOL           | RATING                        | UNIT | NOTE |
|-----------------------|------------------|-------------------------------|------|------|
| Supply voltage        | V <sub>CC</sub>  | -0.3 to +7.0                  | V    | 1    |
| Input voltage         | V <sub>IN</sub>  | -0.3 to V <sub>CC</sub> + 0.3 | V    | 1    |
| Operating temperature | T <sub>opr</sub> | 0 to +70                      | °C   | 2    |
|                       |                  | -40 to +85                    |      | 3    |
| Storage temperature   | T <sub>stg</sub> | -55 to +150                   | °C   |      |

## NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5116/D/NA
3. Applied to the LH5116H/HD/HN

RECOMMENDED OPERATING CONDITIONS <sup>1</sup>

| PARAMETER      | SYMBOL          | MIN. | TYP. | MAX.                  | UNIT |
|----------------|-----------------|------|------|-----------------------|------|
| Supply voltage | V <sub>CC</sub> | 4.5  | 5.0  | 5.5                   | V    |
| Input voltage  | V <sub>IH</sub> | 2.2  |      | V <sub>CC</sub> + 0.3 | V    |
|                | V <sub>IL</sub> | -0.3 |      | 0.8                   | V    |

## NOTE:

1. T<sub>A</sub> = 0 to 70°C (LH5116/D/NA), T<sub>A</sub> = -40 to +85°C (LH5116H/HD/HN)

DC CHARACTERISTICS <sup>1</sup> (V<sub>CC</sub> = 5 V ± 10%)

| PARAMETER              | SYMBOL           | CONDITIONS                                                                           | MIN. | TYP. | MAX. | UNIT | NOTE |
|------------------------|------------------|--------------------------------------------------------------------------------------|------|------|------|------|------|
| Output 'LOW' voltage   | V <sub>OL</sub>  | I <sub>OL</sub> = 2.1 mA                                                             |      |      | 0.4  | V    |      |
| Output 'HIGH' voltage  | V <sub>OH</sub>  | I <sub>OH</sub> = -1.0 mA                                                            | 2.4  |      |      | V    |      |
| Input leakage current  | I <sub>LI</sub>  | V <sub>IN</sub> = 0 V to V <sub>CC</sub>                                             |      |      | 1.0  | μA   |      |
| Output leakage current | I <sub>LO</sub>  | $\overline{CE} = V_{IH}$ , V <sub>I/O</sub> = 0 V to V <sub>CC</sub>                 |      |      | 1.0  | μA   |      |
| Operating current      | I <sub>CC1</sub> | Outputs open ( $\overline{OE} = V_{CC}$ )                                            |      | 25   | 30   | mA   | 2    |
|                        | I <sub>CC2</sub> | Outputs open ( $\overline{OE} = V_{IH}$ )                                            |      | 30   | 40   | mA   | 3    |
| Standby current        | I <sub>SB</sub>  | $\overline{CE} \geq V_{CC} - 0.2$ V<br>All other input pins = 0 V to V <sub>CC</sub> |      |      | 1.0  | μA   |      |
|                        |                  |                                                                                      |      |      | 0.2  |      | 4    |

## NOTES:

1. T<sub>A</sub> = 0 to 70°C (LH5116/D/NA), T<sub>A</sub> = -40 to +85°C (LH5116H/HD/HN)
2.  $\overline{CE} = 0$  V; all other input pins = 0 V to V<sub>CC</sub>
3.  $\overline{CE} = V_{IL}$ ; all other input pins = V<sub>IL</sub> to V<sub>IH</sub>
4. T<sub>A</sub> = 25°C

AC CHARACTERISTICS <sup>1</sup>(1) READ CYCLE (V<sub>CC</sub> = 5 V ± 10%)

| PARAMETER                              | SYMBOL           | MIN. | TYP. | MAX. | UNIT | NOTE |
|----------------------------------------|------------------|------|------|------|------|------|
| Read cycle time                        | t <sub>RC</sub>  | 100  |      |      | ns   |      |
| Address access time                    | t <sub>AA</sub>  |      |      | 100  | ns   |      |
| Chip enable access time                | t <sub>ACE</sub> |      |      | 100  | ns   |      |
| $\overline{CE}$ Low to output in Low-Z | t <sub>CLZ</sub> | 10   |      |      | ns   | 1    |
| Output enable access time              | t <sub>OE</sub>  |      |      | 40   | ns   |      |
| Output enable Low to output in Low-Z   | t <sub>OLZ</sub> | 10   |      |      | ns   | 1    |
| Chip disable to output in High-Z       | t <sub>CHZ</sub> | 0    |      | 40   | ns   | 1    |
| Output disable to output in High-Z     | t <sub>OHZ</sub> | 0    |      | 40   | ns   | 1    |
| Output hold time                       | t <sub>OH</sub>  | 10   |      |      | ns   |      |

## NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C<sub>LOAD</sub> = 5 pF.

(2) WRITE CYCLE <sup>1</sup> ( $V_{CC} = 5\text{ V} \pm 10\%$ )

| PARAMETER                               | SYMBOL    | MIN. | TYP. | MAX. | UNIT | NOTE |
|-----------------------------------------|-----------|------|------|------|------|------|
| Write cycle time                        | $t_{WC}$  | 100  |      |      | ns   |      |
| Chip enable to end of write             | $t_{CW}$  | 80   |      |      | ns   |      |
| Address valid time                      | $t_{AW}$  | 80   |      |      | ns   |      |
| Address setup time                      | $t_{AS}$  | 0    |      |      | ns   |      |
| Write pulse width                       | $t_{WP}$  | 60   |      |      | ns   |      |
| Write recovery time                     | $t_{WR}$  | 10   |      |      | ns   |      |
| Output active from end of write         | $t_{OW}$  | 10   |      |      | ns   | 2    |
| $\overline{WE}$ Low to output in High-Z | $t_{WHZ}$ |      |      | 30   | ns   | 2    |
| Data valid to end of write              | $t_{DW}$  | 30   |      |      | ns   |      |
| Data hold time                          | $t_{DH}$  | 10   |      |      | ns   |      |
| Output enable to output in High-Z       | $t_{OHZ}$ |      |      | 40   | ns   | 2    |
| Output active from end of write         | $t_{OW}$  | 10   |      |      | ns   | 2    |

## NOTES:

- $T_A = 0$  to  $+70^\circ\text{C}$  (LH5116/D/NA),  $T_A = -40$  to  $+85^\circ\text{C}$  (LH5116H/HD/HN)
- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 500$  mV transition from steady state levels into the test load.  $C_{LOAD} = 5$  pF.

## AC TEST CONDITIONS

| PARAMETER               | MODE           |
|-------------------------|----------------|
| Input voltage amplitude | 0.8 V to 2.2 V |
| Input rise/fall time    | 10 ns          |
| Timing reference level  | 1.5 V          |
| Output load condition   | 1TTL + 100 pF  |

DATA RETENTION CHARACTERISTICS <sup>1</sup>

| PARAMETER                      | SYMBOL     | CONDITIONS                                                                 | MIN.     | TYP. | MAX.       | UNIT          | NOTE |
|--------------------------------|------------|----------------------------------------------------------------------------|----------|------|------------|---------------|------|
| Data retention voltage         | $V_{CCDR}$ | $\overline{CE} \geq V_{CCRC} - 0.2\text{V}$                                | 2.0      |      |            | V             |      |
| Data retention current         | $I_{CCDR}$ | $\overline{CE} \geq V_{CCDR} - 0.2\text{V}$ ,<br>$V_{CCDR} = 3.0\text{ V}$ |          |      | 1.0<br>0.2 | $\mu\text{A}$ | 2    |
| Chip disable to data retention | $t_{CDR}$  |                                                                            | 0        |      |            | ns            |      |
| Recovery time                  | $t_R$      |                                                                            | $t_{RC}$ |      |            | ns            | 3    |

## NOTES:

- $T_A = 0$  to  $+70^\circ\text{C}$  (LH5116/D/NA),  $T_A = -40$  to  $+85^\circ\text{C}$  (LH5116H/HD/HN)
- $T_A = 25^\circ\text{C}$
- $t_{RC}$  = Read cycle time

CAPACITANCE <sup>1</sup> ( $f = 1\text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ )

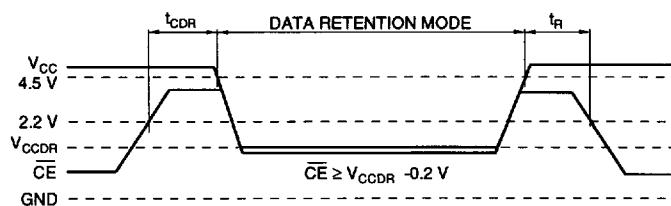
| PARAMETER                | SYMBOL   | CONDITIONS            | MIN. | TYP. | MAX. | UNIT |
|--------------------------|----------|-----------------------|------|------|------|------|
| Input capacitance        | $C_{IN}$ | $V_{IN} = 0\text{ V}$ |      |      | 7    | pF   |
| Input/output capacitance | $C_{IO}$ | $V_{IO} = 0\text{ V}$ |      |      | 10   | pF   |

## NOTE:

- This parameter is sampled and not production tested.

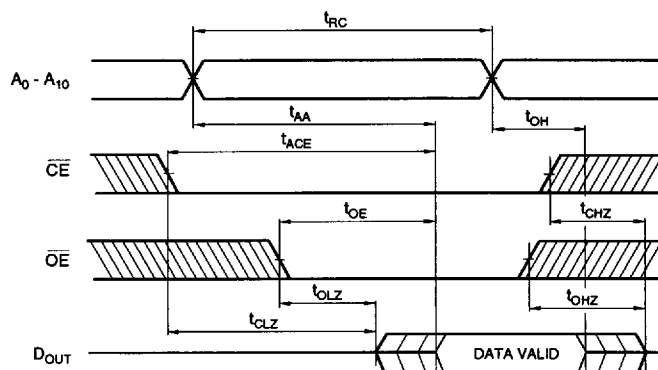
SHARP CORP

61E D ■ 8180798 0009682 067 ■ SRPJ



5116-6

Figure 3. Low Voltage Data Retention

NOTE:  $\overline{WE}$  = "HIGH"

5116-3

Figure 4. Read Cycle

SHARP CORP

61E D

8180798 0009683 TT3 SRPJ

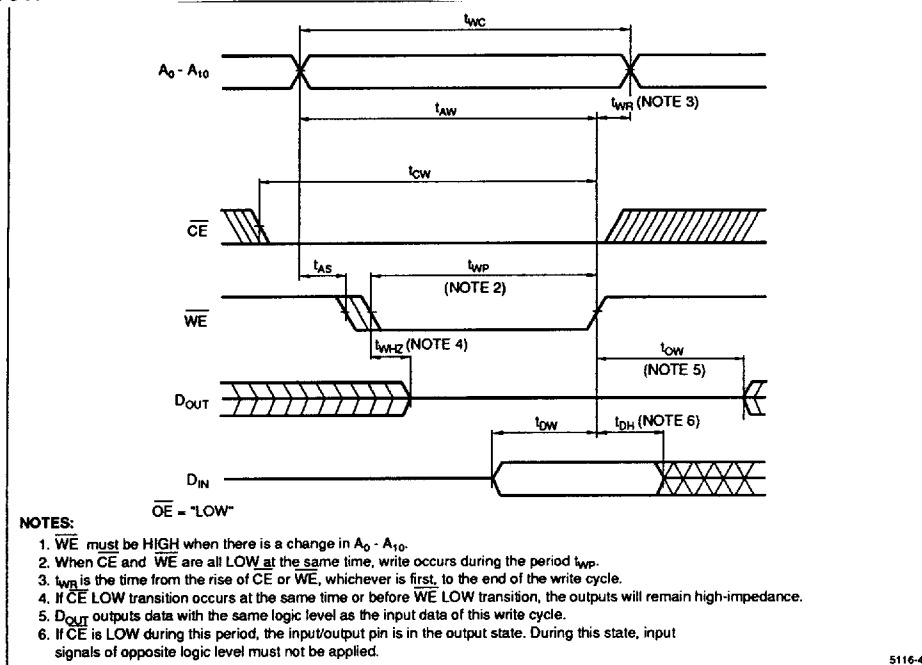


Figure 5. Write Cycle 1

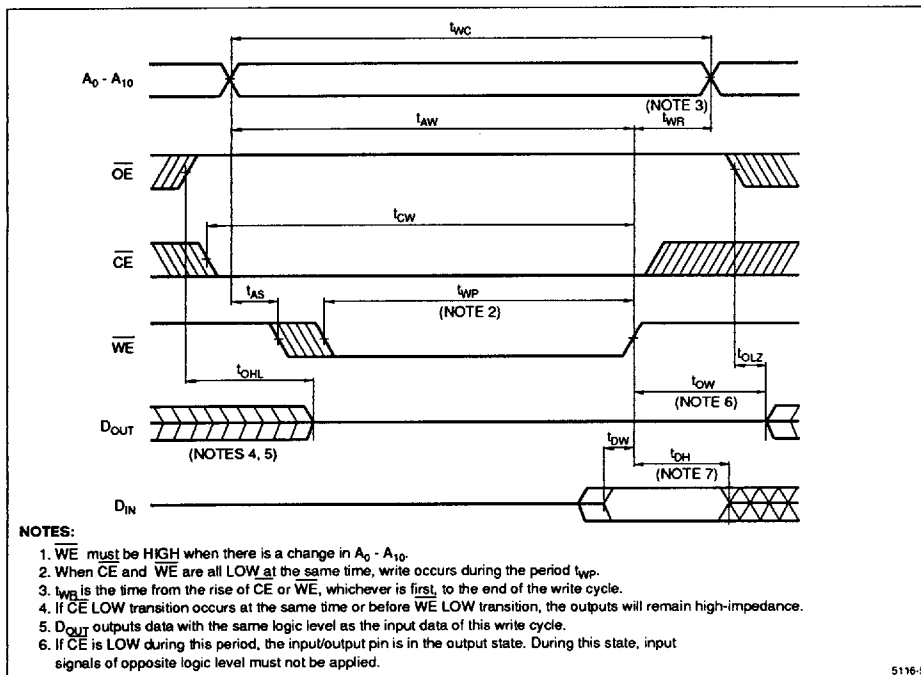
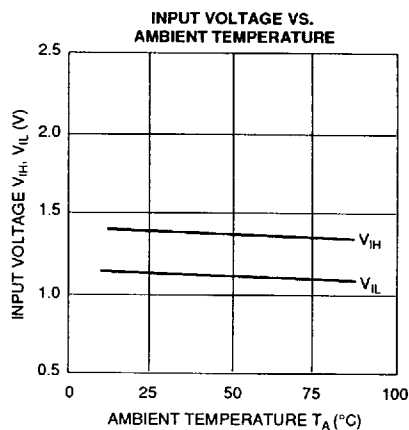
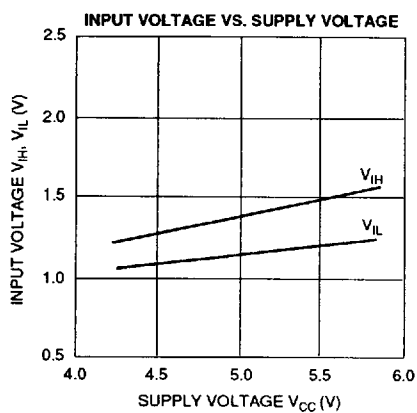
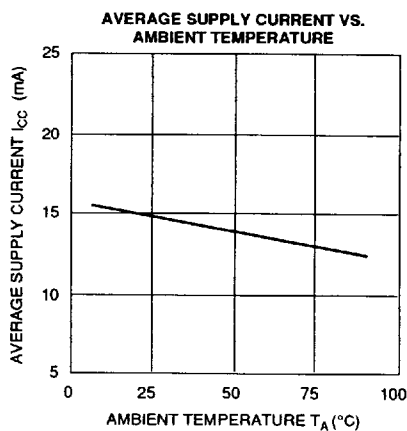
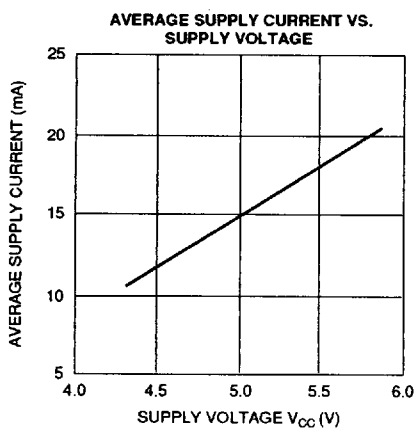
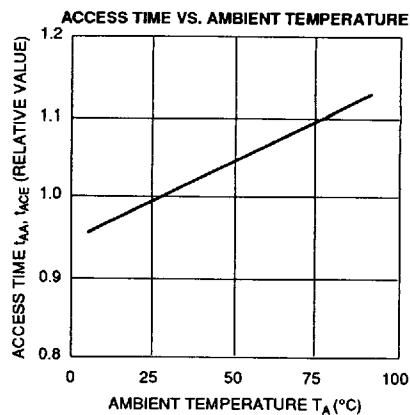
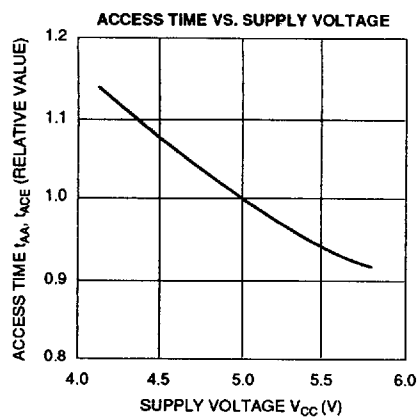


Figure 6. Write Cycle 2 (Note 1)

SHARP CORP

61E D ■ 8180798 0009684 93T ■ SRPJ



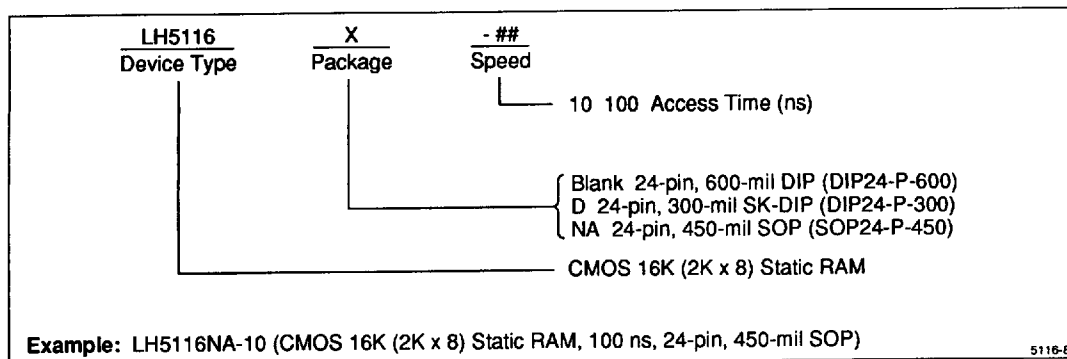
5116-7

Figure 7. Electrical Characteristic Curves  
( $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified)

SHARP CORP

L1E D

8180798 0009685 876 SRPJ

ORDERING INFORMATION (T<sub>A</sub> = 0°C to 70°C)ORDERING INFORMATION (T<sub>A</sub> = -40°C to +85°C)