Dual-Slot PCMCIA/CardBus Power Controller

Features

- **Backward Compatible with G570**
- **Fully Integrated V_{CC} and V_{pp} Switching for Dual Slot PC Card™ Interface**
- **3-Lead Serial Interface Compatible With CardBus™ Controllers**
- **3.3V Low Voltage Mode**
- **Meets PC Card Standards**
- **RESET for System Initialization of PC Cards**
- **12V Supply Can Be Disabled Except During 12V Flash Programming**
- **Short Circuit and Thermal Protection**
- **30 Pin SSOP**
- **Compatible With 3.3V, 5V and 12V PC Cards**
- **Low $R_{DS(on)}$ (180-mΩ 5V V_{CC} Switch; 130 mΩ 3.3V V_{CC} Switch)**
- **Break-Before-Make Switching**
- **Internal power-On Reset**
- **Standby mode: 60mA current limit (TYP)**

Application

- **Notebook PC**
- **Electronic Dictionary**
- **POS**

Description

The G574 PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit (IC). The circuit allows the distribution of 3.3V, 5V, and/or 12V card power by means of the Serial interface. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability.

The G574 features a 3.3V low voltage mode that allows for 3.3V switching without the need for 5V supply. This facilitates low power system designs such as sleep mode and pager mode where only 3.3V is available.
The G574 incorporates a reset function, selectable by one of two inputs, to help alleviate system errors. The reset function enables PC card initialization concurrent with host platform initialization, allowing a system reset. Reset is accomplished by grounding the V_{CC} and V_{PP} (flash-memory programming voltage) outputs, which discharges residual card voltage.

This device also has the ability to program the xVpp outputs independent of the xVCC outputs. A standby mode that changes all output-current limits to 50mA (typical) has been incorporated.

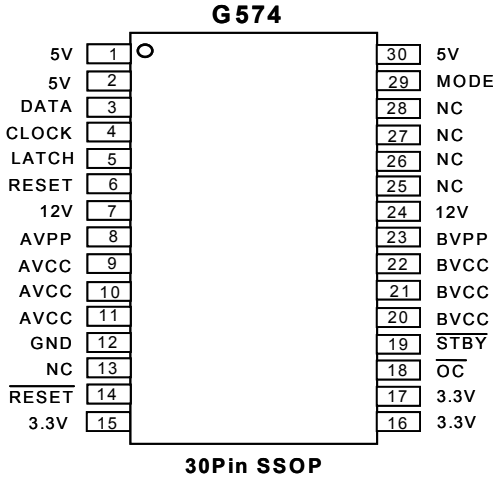
End equipment for the G574 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras and bar-code scanners.

The G574 is backward-compatible with the G570.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
G574SA	-40°C to +85°C	30 SSOP

Pin Configuration



Absolute maximum ratings over operating free-air temperature (unless otherwise noted)*

Input voltage range for card power:
$V_{I(3.3V)}$.....-0.3V to 6V
$V_{I(5V)}$.....-0.3V to 6V
$V_{I(12V)}$..... -0.3V to 14V
Logic input voltage.....-0.3V to 6V
Output current (each card):
$I_{O\ (xVCC)}$.....internally limited
$I_{O(xVPP)}$.....internally limited

Operating virtual junction temperature range, T_J
.....-40°C to 125°C
Operating free-air temperature range, T_A
.....-40°C to 85°C
Storage temperature range, T_{STG}.....-55°C to 150°C
Thermal resistance θ_{JA}
SSOP 30.....122°C/W
Power dissipation P_D ($T_A \leq +25°C$)
SSOP 30.....1024mW
ESD.....Note1

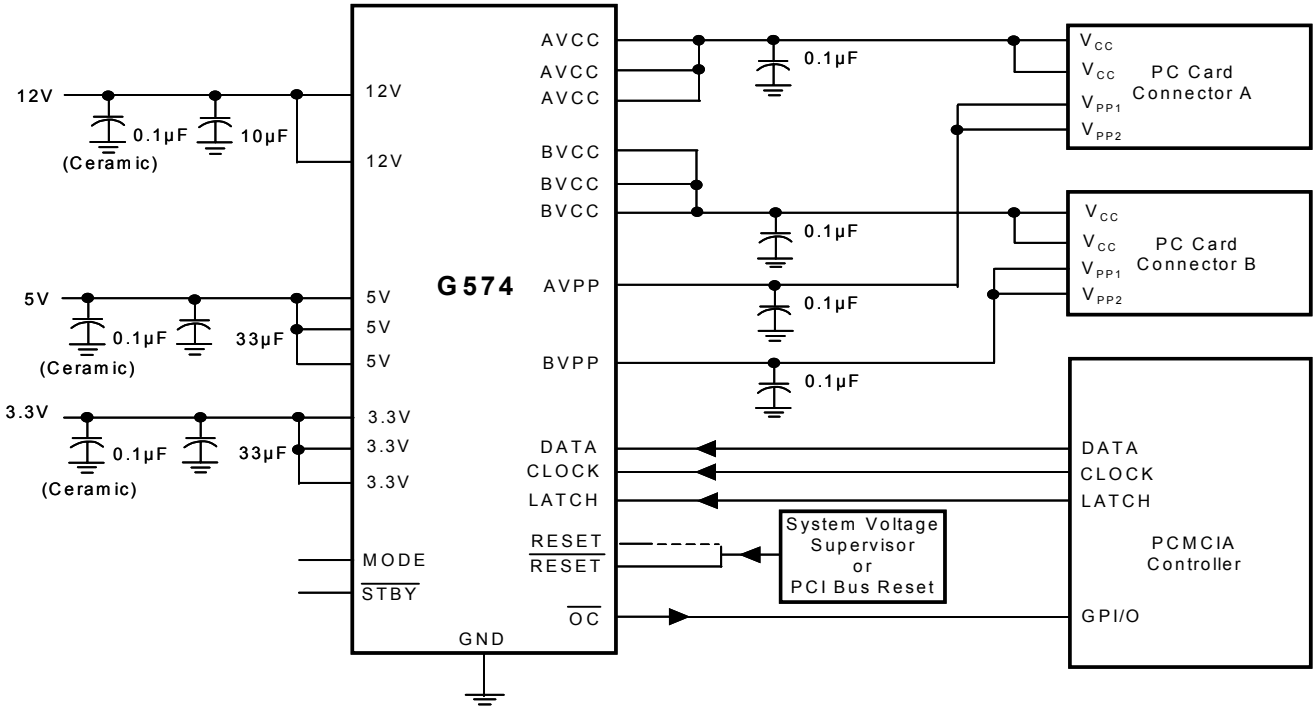
*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum-rated conditions for extended periods may affect device reliability.

Note 1: ESD (electrostatic discharge) sensitive device. Proper ESD precautions are recommended to avoid performance degradation or less of functionality.

Recommended Operating Conditions

		Min	Max	Unit
Input voltage range, V_I	$V_{I\ (5V)}$	2.7	5.25	V
	$V_{I\ (3.3V)}$	2.7	5.25	V
	$V_{I\ (12V)}$		13.5	V
Output current	$I_{O\ (xVCC)}$ at 25°C		1	A
	$I_{O\ (xVPP)}$ at 25°C		150	mA
Clock frequency		0	2.5	MHz
Operating virtual junction temperature, T_J		-40	125	°C

Typical PC Card Power-Distribution Application



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
3.3V	15,16,17	I	3.3V V_{CC} input for card power
5V	1,2,30	I	5V V_{CC} input for card power and/or chip power
12V	7,24	I	12V V_{PP} input for card power
AVCC	9,10,11	O	Switched output that delivers 0V, 3.3V, 5V or high impedance to card
AVPP	8	O	Switched output that delivers 0V, 3.3V, 5V, 12V or high impedance to card
BVCC	20,21,22	O	Switched output that delivers 0V, 3.3V, 5V or high impedance
BVPP	23	O	Switch output that delivers 0V, 3.3V, 5V, 12V or high impedance
GND	12		Ground
MODE	29	I	G570 operation when floating or pulled low; must be pulled high externally for G574 operation. MODE is internally pulled low with a 150kΩ pulldown resistor.
$\overline{OC}$	18	O	Logic-level overcurrent. reports output that goes low when an overcurrent condition exists
RESET	6	I	Logic-level reset input active high. Do not connect if $\overline{RESET}$ pin is used. RESET is internally pulled low with a 150kΩ pulldown resistor.
$\overline{RESET}$	14	I	Logic-level reset input active low. Do not connect if RESET pin is used. The pin is internally pulled high with a 150kΩ pullup resistor to 5V, if 5V V_{CC} exists. And pulled to 3.3V, if 3.3V V_{CC} exists only.
$\overline{STBY}$	19		Logic-level active low input sets the G574 to standby mode and sets all current limits to 50mA. The pin is internally pulled high with a 150kΩ pullup resistor to 5V, if 5V V_{CC} exists. And pulled to 3.3V, if 3.3V V_{CC} exists only.
CLOCK	4	I	Logic level clock for serial data word
DATA	3	I	Logic level serial data word
LATCH	5	I	Logic level latch for serial data word
NC	13,25,26, 27,28		No internal connection

Electrical Characteristics

(T_A=T_J=25°C, $V_{I(5V)}$=5V, $V_{I(3.3V)}$=3.3V, $V_{I(12V)}$=12V, $\overline{STBY}$ floating, all outputs unloaded (unless otherwise noted)

DC Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switch resistance*	5V to xVCC				150	180	mΩ
	3.3V to xVCC		$V_{I(5V)}$ = 5V, $V_{I(3.3V)}$ =3.3V		100	130	
	3.3V to xVCC		$V_{I(5V)}$ = 0V, $V_{I(3.3V)}$ =3.3V		110	150	
	5V to xVPP				3	4	Ω
	3.3V to xVPP				2.9	4	
	12V to xVPP				1.3	2	
	3.3V/5V to xVCC		$\overline{STBY}$ = low, I_O = 30mA		1.2	2	Ω
	3.3V/5V to xVPP				12	12.5	
	12V to xVPP				5	6.5	
$V_{O(xVPP)}$ Clamp low voltage			I_{PP} at 10mA		0.18	0.8	V
$V_{O(xVCC)}$ Clamp low voltage			I_{CC} at 10mA		0.13	0.8	V
I_{IKG} Leakage current	I_{PP} high impedance State		T_A = 25°C		0.3	1	μA
	I_{CC} high-impedance State		T_A = 25°C		0.3	1	
I_I Input current⊙	Normal operation and in reset mode	$I_{I(3.3V)}$	$V_{O(xVCC)}$ = $V_{O(xVCC)}$ = 5V		6	15	μA
		$I_{I(5V)}$			110	150	
		$I_{I(12V)}$			5	15	
		$I_{I(3.3V)}$	$V_{I(5V)}$ = 0, $V_{O(xVCC)}$ = 3.3V $V_{O(xVPP)}$ = 12V		82	150	μA
		$I_{I(5V)}$			0		
		$I_{I(12V)}$			17	45	
	Shutdown mode	$I_{I(3.3V)}$	$V_{O(xVCC)}$ = Hi-Z, $V_{O(xVPP)}$ = Hi-Z			1	μA
		$I_{I(5V)}$			2	10	
		$I_{I(12V)}$				1	
I_{OS} Short-circuit* Output current Limit	$I_{O(xVCC)}$		Output powered into a short to GND	0.8		2.2	A
	$I_{O(xVPP)}$			120		450	mA
	Standby mode, 3.3V to xVCC		T_J = 25°C Output powered into a short to GND $\overline{STBY}$ =0V		55	120	mA
	Standby mode, 5V to xVCC				70	120	
	Standby mode, 3.3V to xVPP				44	120	
	Standby mode, 5V to xVPP				78	120	
	Standby mode, 12V to xVPP				60	110	
Thermal shutdown※	Trip point, TJ				155		°C
	Hysteresis				10		

* Pulse-testing techniques are used to maintain junction temperature close to ambient temperatures; thermal effects must be taken into account separately.

⊙Input currents do not include logic input currents (presented in electrical characteristics for logic section); clock is inactive.

※Specified by design, not tested in production.

Logic Section

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Logic input current	I_I (RESET) or ($\overline{RESET}$)*	$V_{I(RESET)}$ = 5V or $V_{I(\overline{RESET})}$ = 0V		35	50	μA
		$V_{I(RESET)}$ = 0V or $V_{I(\overline{RESET})}$ = 5V			1	
	I_I (MODE)*	$V_{I(MODE)}$ = 5V		35	50	
		$V_{I(MODE)}$ = 0V			1	
	I_I ($\overline{STBY}$)*	$V_{I(\overline{STBY})}$= 5V			1	
		$V_{I(\overline{STBY})}$= 0V		35	50	
	I_I(CLOCK) or I_I(DATA) or I_I (LATCH)				1	
Logic input high level			2			V
Logic input low level			2		0.8	V
Logic output high level, $\overline{OC}$		$V_{I(5V)}$ = 5V, I_O = 1mA	$V_{I(5V)}$−0.4			V
		$V_{I(5V)}$ = 0V, I_O = 1mA	$V_{I(3.3V)}$−0.4			
Logic output low level, $\overline{OC}$		I_O = 1mA			0.4	V

*RESET and MODE have internal 150kΩ pulldown resistors; $\overline{RESET}$ and $\overline{STBY}$ have internal 150kΩ pullup resistors.

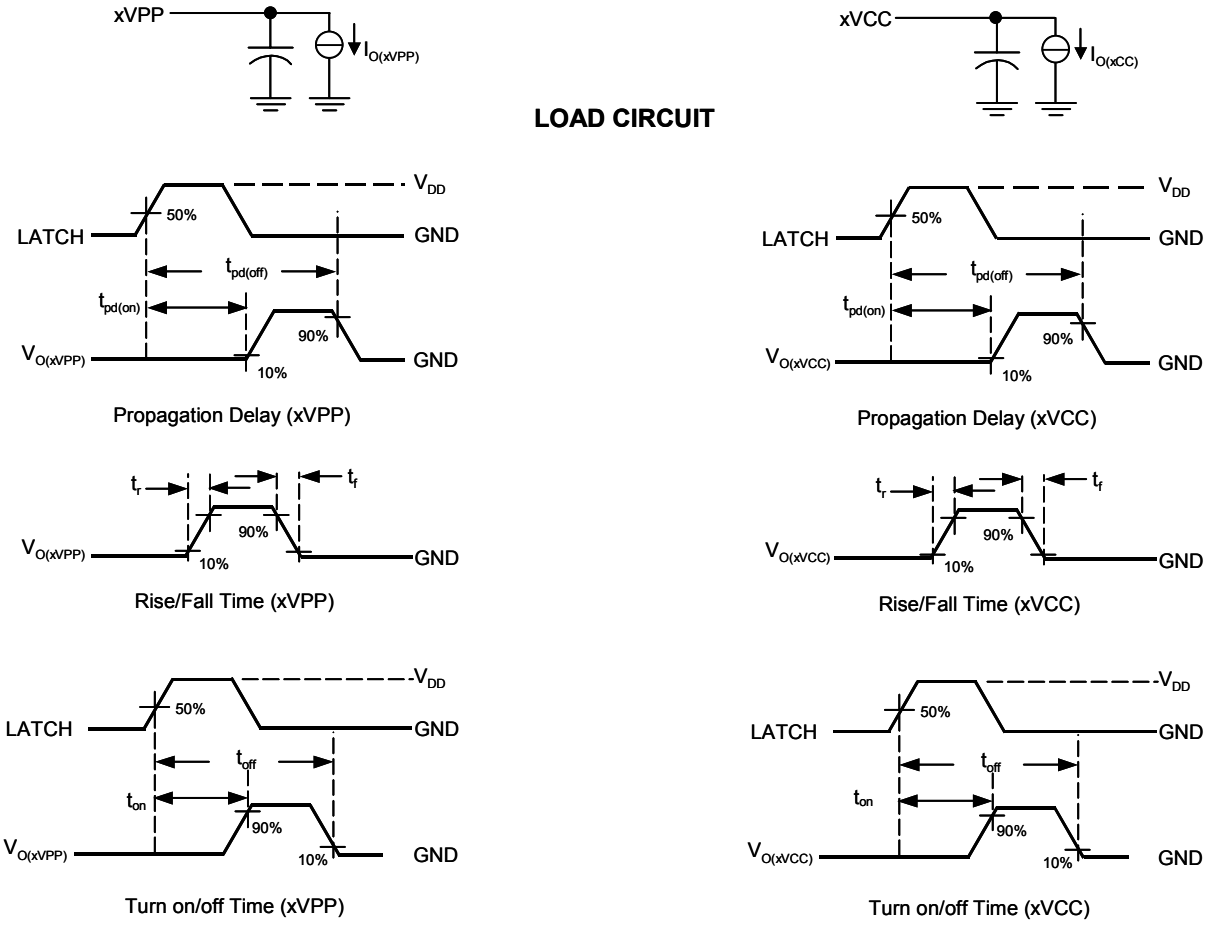
Switching Characteristics *, **

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
t_r	Output rise time	$V_{O\ (xVCC)}$			2		ms
		$V_{O\ (xVPP)}$ (12V)			0.04		
		$V_{O\ (xVPP)}$ (3.3V or 5V)			0.4		
t_f	Output fall time	$V_{O\ (xVCC)}$			0.01		ms
		$V_{O\ (xVPP)}$			0.01		
t_{pd}	Propagation delay (see Figure 1)	LATCH ↑ to $V_{O(xVPP}$(12V)	$t_{pd(on)}$		0.2		ms
			$t_{pd(off)}$		1.8		
		LATCH ↑ to $V_{O(xVPP=xVCC)}$ (3.3V), $V_{I(5V)}$ = 5V	$t_{pd(on)}$		1.7		ms
			$t_{pd(off)}$		2.2		
		LATCH ↑ to $V_{O(xVPP=xVCC)}$ (5V)	$t_{pd(on)}$		1.7		ms
			$t_{pd(off)}$		2.2		
		LATCH ↑ to $V_{O(xVCC)}$ (3.3V), $V_{I(5V)}$ = 5V	$t_{pd(on)}$		2.4		ms
			$t_{pd(off)}$		8.5		
		LATCH ↑ to $V_{O(xVCC)}$ (5V)	$t_{pd(on)}$		1		ms
			$t_{pd(off)}$		8.5		
		LATCH ↑ to $V_{O(xVCC)}$ (3.3V), $V_{I(5V)}$ = 0V	$t_{pd(on)}$		2.6		ms
			$t_{pd(off)}$		8.2		

* Refer to Parameter Measurement Information

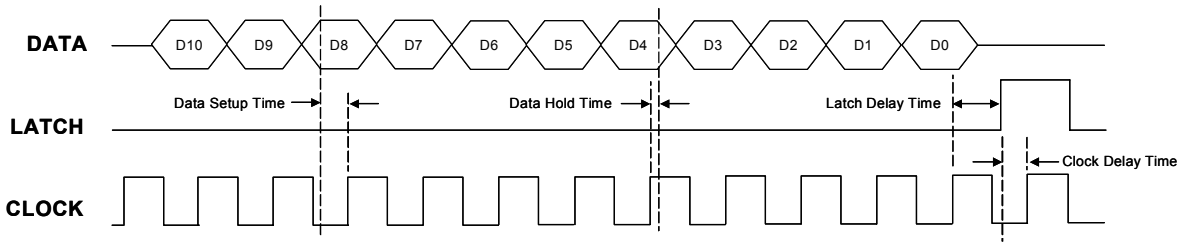
**Switching Characteristics are with C_L = 0.1µF

Parameter Measurement Information



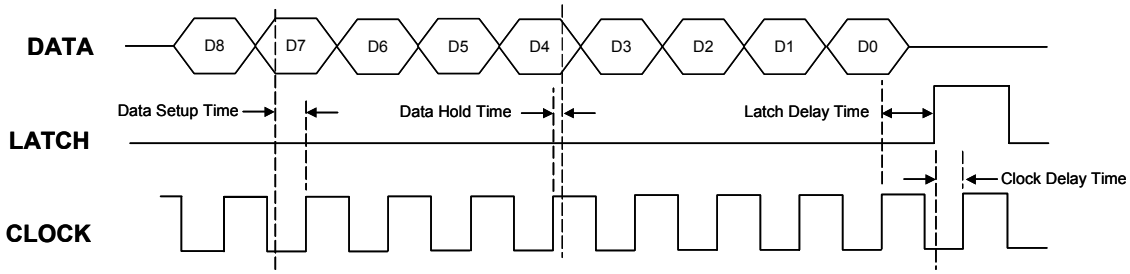
VOLTAGE WAVEFORMS

Figure 1. Test Circuits and Voltage Waveforms



Note: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D10, see the control logic table.

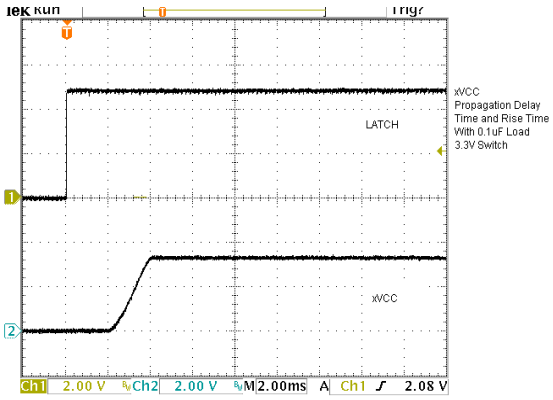
Figure 2. Serial-Interface Timing for Independent xVPP Switching When MODE=5V or 3.3V

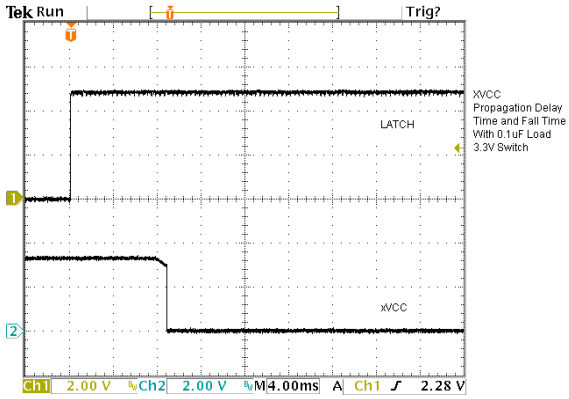


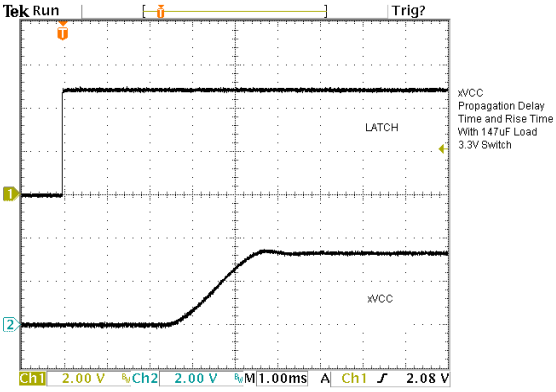
Note: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D8, see the control logic table.

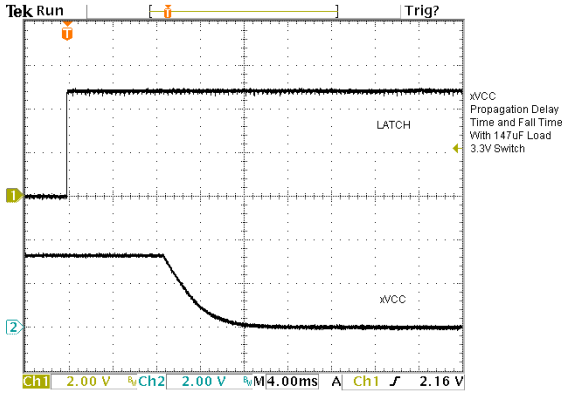
Figure 3. Serial-Interface Timing When MODE = 0V or Floating

Switching Characteristics

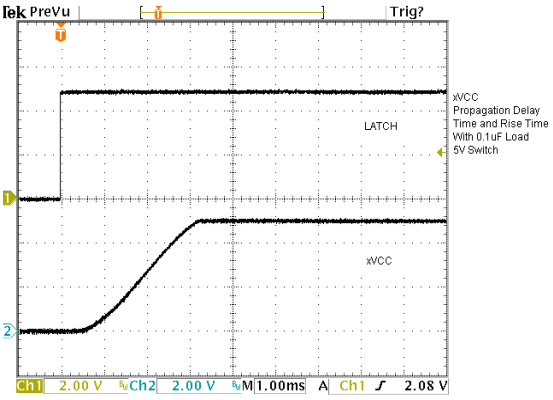


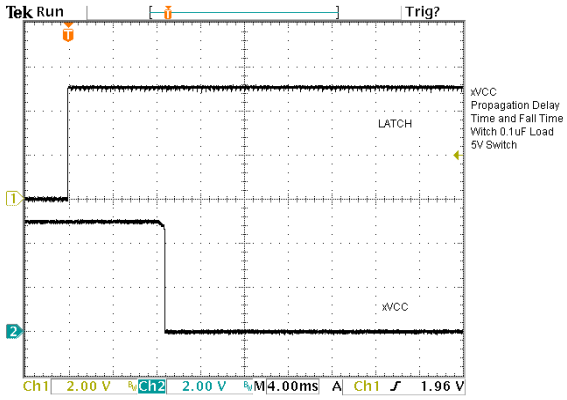


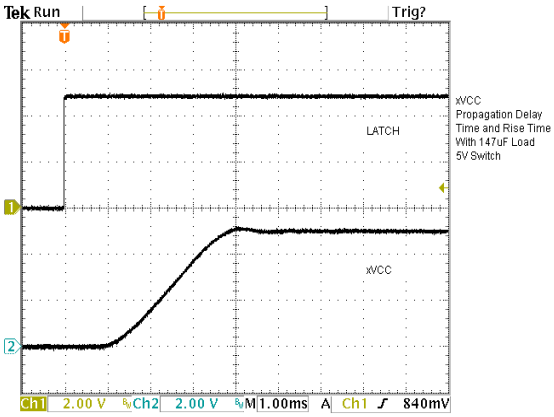


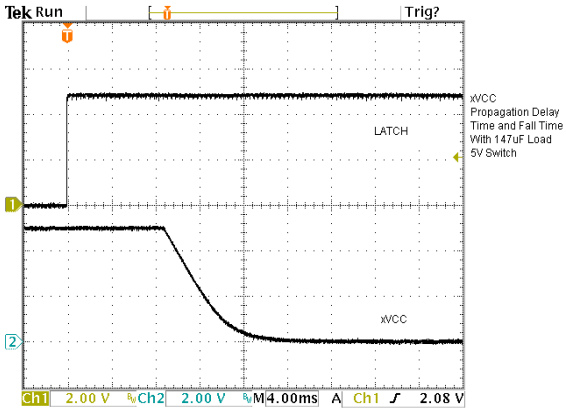


Switching Characteristics

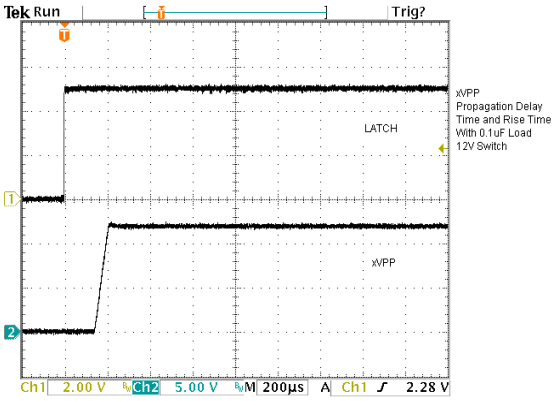


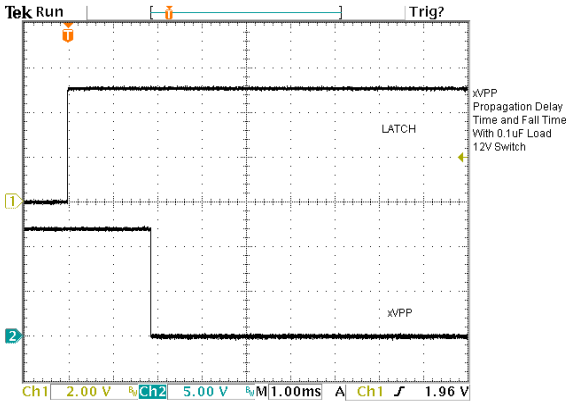


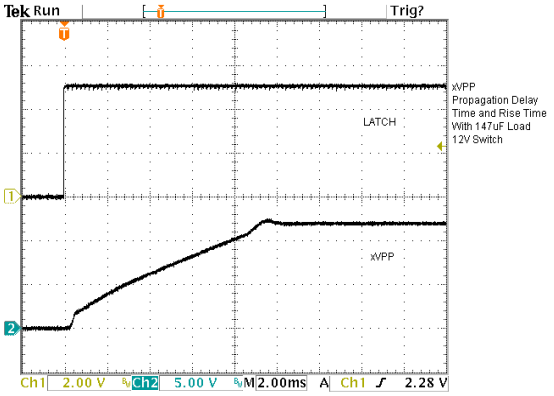


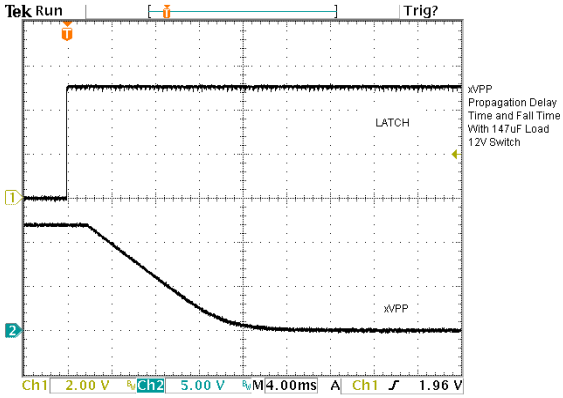


Switching Characteristics

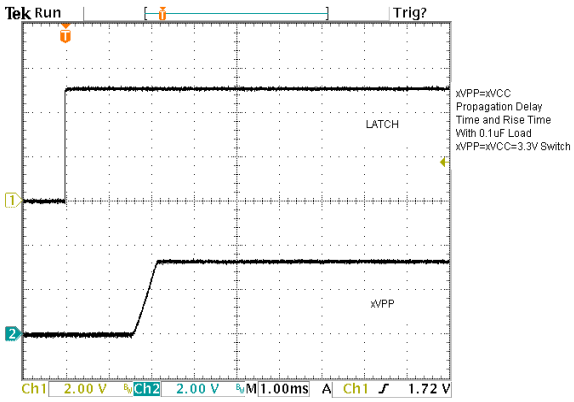


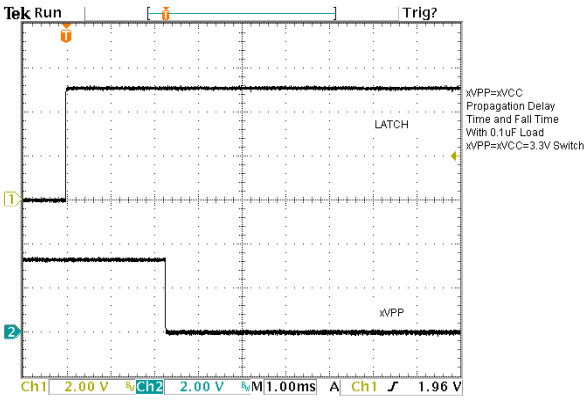


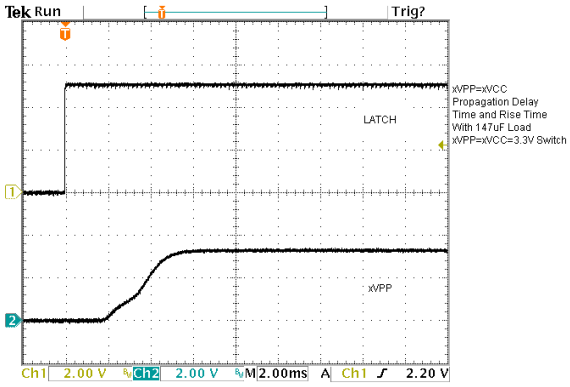


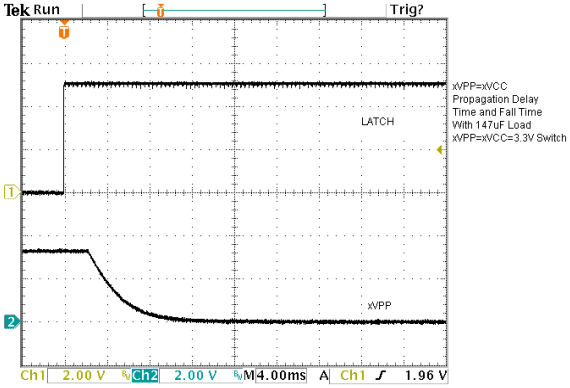


Switching Characteristics

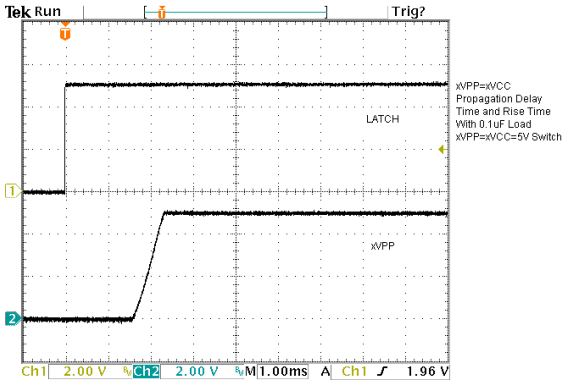


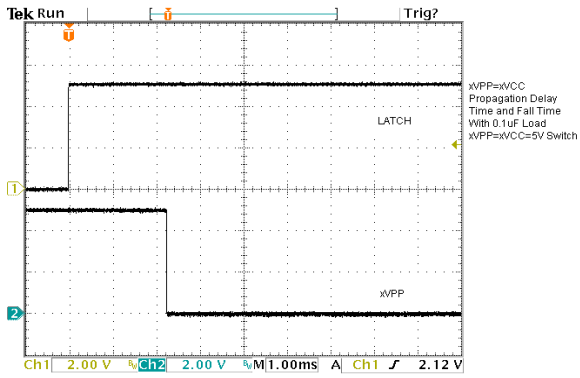


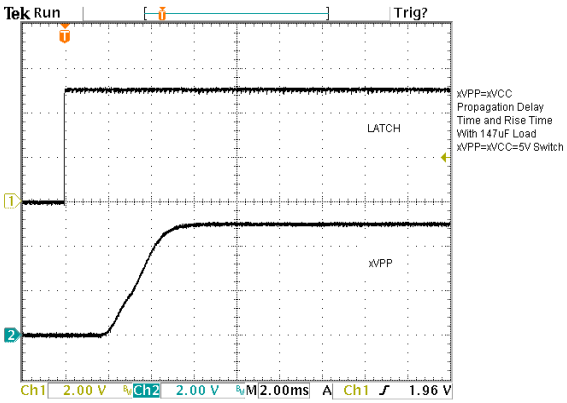


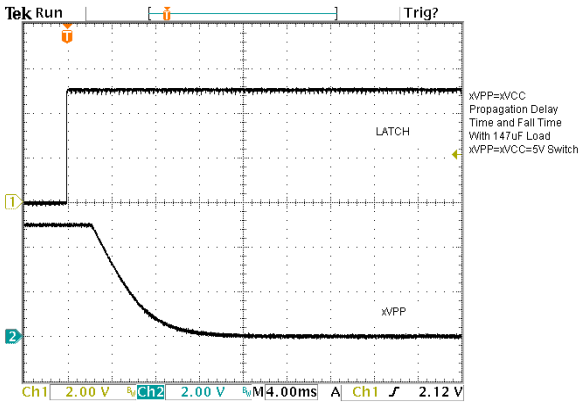


Switching Characteristics






Tek Run
Trig?
LATCH
xVPP
xVPP=xVCC
Propagation Delay
Time and Rise Time
With 147uF Load
xVPP=xVCC=5V Switch
Ch1 2.00 V
Ch2 2.00 V
M2.00ms
A Ch1 1.96 V


Tek Run
Trig?
LATCH
xVPP
xVPP=xVCC
Propagation Delay
Time and Fall Time
With 147uF Load
xVPP=xVCC=5V Switch
Ch1 2.00 V
Ch2 2.00 V
M4.00ms
A Ch1 2.12 V

Application Information

Overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold; modems, wireless LANs, Global Positioning Satellite (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA was established, comprised of members from leading computer, software, PC Card, and semiconductor manufactures. One key goal was to realize the “plug-and play” concept. Cards and hosts from different vendors should be compatible—able to communicate with one another transparently.

PC Card Power Specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{PP}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{PP} terminals were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{PP} terminals.

Overcurrent and Over-Temperature Protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB-trace damage. Even systems robust enough to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. Most hosts include fuses for protection. However, the reliability of fused systems is poor, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The G574 takes a two-pronged approach to overcurrent protection. First, instead of fuses, sense FETs monitor each of the power outputs. Excessive current generates an error signal that linearly limits the output current, preventing host damage or failure. Sense FETs, unlike sense resistors or polyfuses, have an added advantage in that they do not add to the series resistance of the switch and thus produce no additional voltage losses. Second, when an overcurrent condition is detected, the G574 asserts a signal at $\overline{OC}$ that can be monitored by the microprocessor to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region.

12V Supply Not Required

Most PC Card switches use the externally supplied 12V V_{PP} power for switch-gate drive and other chip functions, which requires that power be present at all times. The G574 offers considerable power savings by using an internal charge pump to generate the required higher voltages from 5V or 3.3V input; therefore, the external 12V supply can be disable except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the 12V input if the 12V input is not used. Additional power savings are realized by the G574 during a software shutdown in which quiescent current drops to a typical of 2μA.

3.3V Low Voltage Mode

The G574 operates in 3.3V low voltage mode when 3.3V is the only available input voltage ($V_{I(5V)}$=0, $V_{I(12V)}$=0).This allows host and PC Cards to be operated in low power 3.3V only modes such as sleep modes or pager modes. Note that in this operation mode, the G574 derives its bias current from the 3.3V input pin and only 3.3V can be delivered to the Card. The 3.3V switch resistance increases, but the added switch resistance should not be critical, because only a small amount of current is delivered in this mode.

Voltage Transitioning Requirement

PC Cards, like portables, are migrating from 5V to 3.3V to minimize power consumption, optimize board space, and increase logic speeds. The G574 is designed to meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3V/5V systems by first powering the card with 5V, then polling it to determine its 3.3V compatibility. The PCMCIA specification requires that the capacitors on 3.3V compatible cards be discharged to below 0.8 V before applying 3.3V power. This ensures that sensitive 3.3V circuitry is not subjected to any residual 5V charge and functions as a power reset. The G574 offer a selectable V_{CC} and V_{PP} ground state, in accordance with PCMCIA 3.3V/5V switching specifications, to fully discharge the card capacitors while switching between V_{CC} voltage.

Shutdown Mode

In the shutdown mode, which can be controlled by bit D8 of the input serial DATA word, each of he xVCC and xVPP outputs is forced to a high-inpedance state. In this mode, the chip quiescent current is limited to 2µA or less to conserve battery power.

Standby Mode

The G574 can be put in standby mode by pulling $\overline{\text{STBY}}$ low to conserve power during low-power operation. In this mode, all of the power outputs (xVCC and xVPP) will have a nominal current limit of 50mA. $\overline{\text{STBY}}$ has an internal 150 kΩ pullup resistor. The output-switch status of the device must be set, allowing the output capacitors to charge, prior to enabling the standby mode. Changing the setting of the output switches with the device in standby mode may cause an overcurrent response to be generated.

Mode

The mode pin programs the switches in either G574 or G570 mode. An internal 150 kΩ pulldown resistor is connected to the pin. Floating or pulling the mode pin low sets the switches in G570 mode; pulling the mode pin high sets the switches in G574 mode. In G570mode, xVPP outputs are dependent on xVCC outputs. In G574 mode, xVPP is programmed independent of xVCC. Refer to G574 control-logic tables for more information.

Output Ground Switches

Several PCMCIA power distribution switches on the market do not have an active grounding FET switch. These devices do not meet the PC Card specification requiring a discharge of V_{CC} within 100ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high impedance isolation by power management schemes. A method commonly shown to alleviate this problem is to add to the switch output an external 100kΩ resistor in parallel with the PC Card. Considering that this is the only discharge path to ground, a timing analysis show that the RC time constant delays the required discharge time to more than 2 seconds. The only way to ensure timing compatibility with PC Card standards is to use a power-distribution switch that has an internal ground switch, like that of the G574, or add an external ground FET to each of the output lines with the control logic necessary to select it.

In summary, the G574 is a complete single-chip dual-slot PC Card power interface. It meets all currently defined PCMCIA specifications for power delivery in 5V, 3.3V, and mixed systems, and offers a serial control interface. The G574 offers functionality, power savings, overcurrent and thermal protection, and fault reporting in one 30 pin SSOP surface-mount package for maximum value added to new portable designs.

Power Supply Considerations

The G574 has multiple pins for each of its 3.3V, 5V, and 12V power inputs and for switched V_{CC} outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. Both 12V inputs must be connected for proper V_{PP} switching; it is recommended that all input and output power pins be paralleled for optimum operation.

Although the G574 is fairly immune to power input fluctuations and noise, it is generally considered good design practice to bypass power supplies typically with a 1µF electrolytic or tantalum capacitor paralleled by a 0.047µF to 0.1µF ceramic capacitor. It is strongly recommended that the switched V_{CC} and V_{PP} outputs be bypassed with a 0.1µF or larger capacitor; doing so improves the immunity of the G574 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the G574 and the load. High switching currents can produce large negative-voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below –0.3V.

RESET or $\overline{\text{RESET}}$ Inputs

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying a low impedance to the xV_{CC} and xV_{PP} terminals to ground. A low impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The RESET or $\overline{\text{RESET}}$ input will closes internal switches S1, S4, S7, and S11 with all other switches left open (see G574 control logic table). The G574 remains in the low impedance output state until the signal is deasserted and further data is clocked in and latched. RESET or $\overline{\text{RESET}}$ are provided for direct compatibility with systems that use either an active-low or active-high reset voltage supervisor. The unused pin is internally pulled up or down and should be left unconnected.

Overcurrent and Thermal Protection

The G574 uses sense FETs to check for overcurrent conditions in each of the V_{CC} and V_{PP} outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The OC indicator, normally a logic high, is a logic low when any overcurrent condition is detected, providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the G574 controls the rise time of the V_{CC} and V_{PP} outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10A to 15A may flow into the short before the current limiting of the G574 engages. If the V_{CC} or V_{PP} outputs are driven below ground, the G574 may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the V_{CC} outputs is designed to activate, if powered up, into a short in the range of 0.8A to 2.2A. The V_{PP} outputs limit from 120mA to 450mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power-dissipation ratings are exceeded. Thermal limiting disables all power outputs (both A and B slots) until the device has cooled.

Logic Input and Outputs

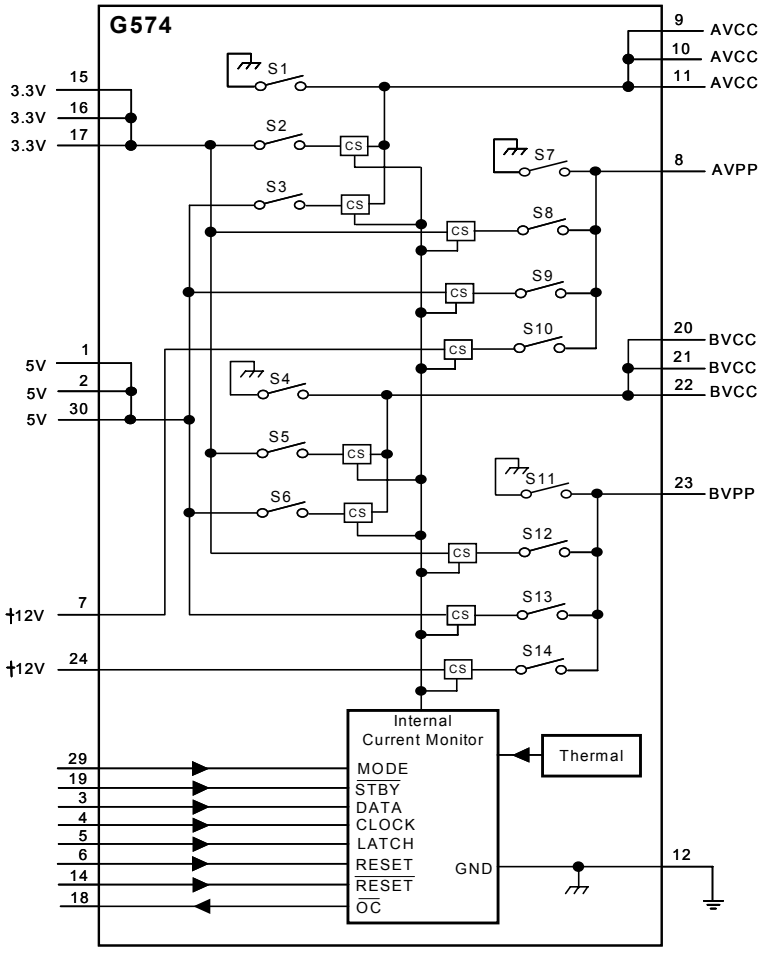
The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive leading edge of the clock (see Figure 2 and 3). The bit (D0 through D10 serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive leading edge of the block.

The shutdown bit of the data word places all V_{CC} and V_{PP} outputs in a high-impedance state and reduces chip quiescent current to 2µA to conserve battery power.

The G574 serial interface is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{OC}$) is provided to indicate an overcurrent condition in any of the V_{CC} or V_{PP} outputs as previously discussed.

Functional Block Diagram



†Both 12V pins must be connected together.

G574 control logic

G574 mode (MODE pulled high)

xVPP

	AVPP CONTROL SIGNALS			OUTPUT	BVPP CONTROL SIGNALS				OUTPUT
D8 ($\overline{SHDN}$)	D0	D1	D9	V_AVPP	D8 ($\overline{SHDN}$)	D4	D5	D10	V_BVPP
1	0	0	×	0V	1	0	0	×	0V
1	0	1	0	3.3V	1	0	1	0	3.3V
1	0	1	1	5V	1	0	1	1	5V
1	1	0	×	12V	1	1	0	×	12V
1	1	1	×	Hi-Z	1	1	1	×	Hi-Z
0	×	×	×	Hi-Z	0	×	×	×	Hi-Z

xVCC

	AVCC CONTROL SIGNALS		OUTPUT	BVCC CONTROL SIGNALS			OUTPUT
D8 ($\overline{SHDN}$)	D3	D2	V_AVCC	D8 ($\overline{SHDN}$)	D6	D7	V-BVCC
1	0	0	0V	1	0	0	0V
1	0	1	3.3V	1	0	1	3.3V
1	1	0	5V	1	1	0	5V
1	1	1	0V	1	1	1	0V
0	×	x	Hi-Z	0	×	x	Hi-Z

G570 mode (MODE floating or pulled low)

xVPP

	AVPP CONTROL SIGNALS		OUTPUT	BVPP CONTROL SIGNALS			OUTPUT
D8 ($\overline{SHDN}$)	D0	D1	V_AVPP	D8 ($\overline{SHDN}$)	D4	D5	V-BVPP
1	0	0	0V	1	0	0	0V
1	0	1	V_AVCC	1	0	1	V_BVCC
1	1	0	12V	1	1	0	12V
1	1	1	Hi-Z	1	1	1	Hi-Z
0	×	x	Hi-Z	0	×	x	Hi-Z

xVCC

	AVCC CONTROL SIGNALS		OUTPUT	BVCC CONTROL SIGNALS			OUTPUT
D8 ($\overline{SHDN}$)	D3	D2	V_AVCC	D8 ($\overline{SHDN}$)	D6	D7	V-BVCC
1	0	0	0V	1	0	0	0V
1	0	1	3.3V	1	0	1	3.3V
1	1	0	5V	1	1	0	5V
1	1	1	0V	1	1	1	0V
0	×	x	Hi-Z	0	×	x	Hi-Z

ESD Protection

The xV_{CC} and xV_{PP} outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1µF capacitors protects the devices from discharges up to 10 kV.

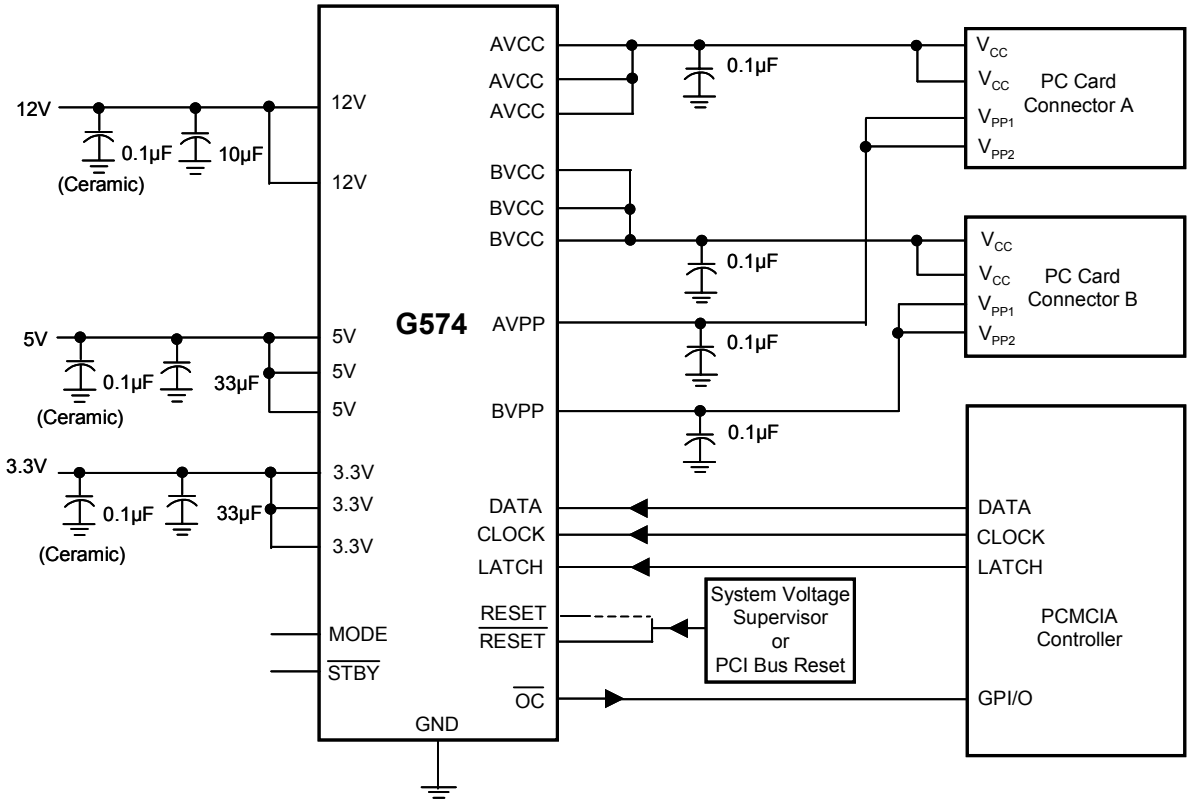
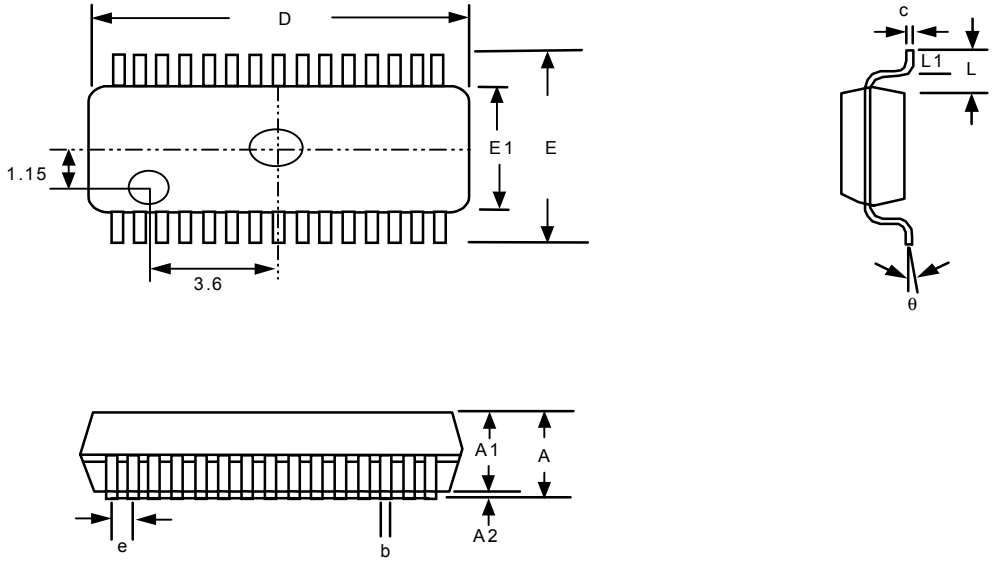


Figure 3. Detailed Interconnections and Capacitor Recommendations

G574 30Pin Package

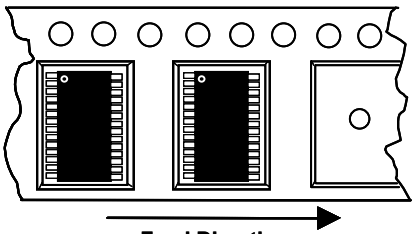


Note:

1. Dimensional tolerance ±0.10mm
2. Plating thickness 5~15μm
3. Dimensions "D" does not include burrs, however dimension including protrusions or gate burrs Shall be MAX. 0.20mm
4. Dimension "E1" does not include inter-lead flash or protrusion. Inter-lead flash or protrusion small not exceeds 0.25 per side.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.80	1.90	2.00	0.071	0.075	0.079
A1	1.75	1.80	1.85	0.069	0.071	0.073
A2	0.05	0.10	0.15	0.002	0.004	.006
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.10	0.15	0.20	0.004	0.006	0.008
D	10.10	10.15	10.20	0.398	0.400	.402
E	7.50	-----	7.90	0.295	-----	0.311
E1	5.20	5.25	5.30	0.205	0.207	0.209
L1	0.53	0.68	0.83	0.021	0.027	0.033
L	1.10	1.20	1.30	0.043	0.047	0.051
e		0.65 BSC			0.026BSC	
θ	1°	4°	7°	1°	4°	7°

Taping Specification



Feed Direction

Typical SSOP Package Orientation