

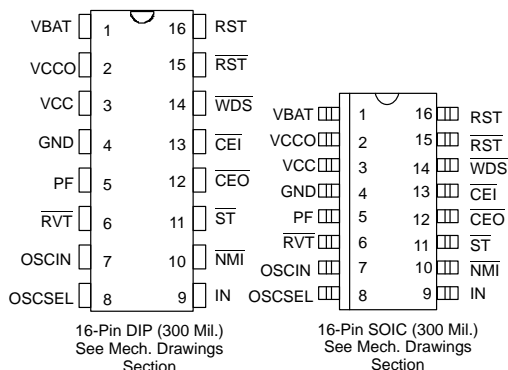
## FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Delays write protection until completion of the current memory cycle
- Consumes less than 200 nA of battery current
- Controls external power switch for high current applications
- Debounces pushbutton reset
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1238-5
- Provides orderly shutdown in microprocessor applications
- Pin-for-pin compatible with MAX691
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

## DESCRIPTION

The DS1238 MicroManager provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1238 also provides early warning detection of a user-defined threshold by driving a non-maskable inter-

## PIN ASSIGNMENT



## PIN DESCRIPTION

V <sub>BAT</sub>	– +3 Volt Battery Input
V <sub>CCO</sub>	– Switched SRAM Supply Output
V <sub>CC</sub>	– +5 Volt Power Supply Input
GND	– Ground
PF	– Power Fail
RVT	– Reset Voltage Threshold
OSCIN	– Oscillator In
OSCSEL	– Oscillator Select
IN	– Early Warning Input
NMI	– Non-Maskable Interrupt
ST	– Strobe Input
CEO	– Chip Enable Output
CEI	– Chip Enable Input
WDS	– Watchdog Status
RST	– Reset Output (active low)
RST	– Reset Output (active high)

rupt. External reset control is provided by a pushbutton reset debounce circuit connected to the RST pin. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog timeout. Oscillator control pins OSCSEL and OSCIN provide either external or internal clock timing for both the reset pulse width and the watchdog timeout period. The Watchdog Status and Reset Voltage Threshold are provided via WDS and RVT, respectively. A block diagram of the DS1238 is shown in Figure 1.

## PIN DESCRIPTION

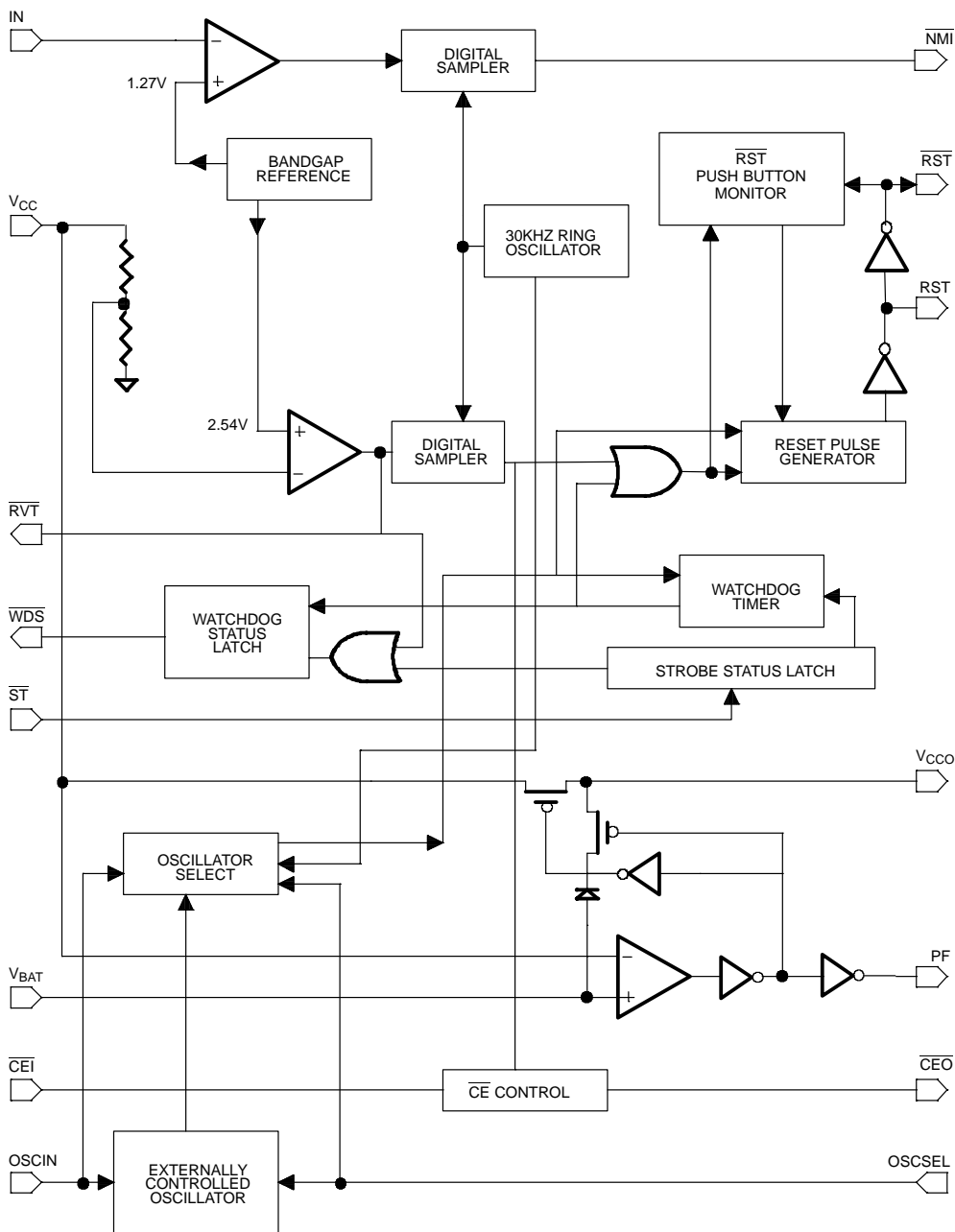
PIN NAME	DESCRIPTION
V <sub>BAT</sub>	+3V Battery Input provides nonvolatile operation of control functions.
V <sub>CCO</sub>	V <sub>CC</sub> output for nonvolatile SRAM applications.
V <sub>CC</sub>	+5V primary power input.
GND	System ground.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
R $\overline{V}T$	Reset Voltage Threshold. Indicates that V <sub>CC</sub> is below the reset voltage threshold.
OSCIN	Oscillator input or timing capacitor. See Table 1.
OSCSEL	Oscillator Select. Selects internal or external clock functions. See Table 1.
IN	Early warning power fail input. This voltage sense point may be tied (via resistor divider) to a user-selected voltage.
N $\overline{M}I$	Non-maskable interrupt. Output used in conjunction with the IN pin to indicate an impending power failure.
S $\overline{T}$	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.
C $\overline{E}O$	Chip enable output. Write protected. Used with nonvolatile SRAM applications.
C $\overline{E}I$	Chip enable input.
W $\overline{D}S$	Watchdog Status. Indicates that a watchdog timeout has occurred.
R $\overline{S}T$	Active low reset output.
RST	Active high reset output.

## POWER MONITOR

The DS1238 employs a band gap voltage reference and a precision comparator to monitor the 5-volt supply (V<sub>CC</sub>) in microprocessor-based systems. When an out-of-tolerance condition occurs, the R $\overline{V}T$ , RST, and R $\overline{S}T$  outputs are driven to the active state. The V<sub>CC</sub> trip point (V<sub>CC<sub>TP</sub></sub>) is set for 10% operation so that the R $\overline{V}T$ , RST and R $\overline{S}T$  outputs will become active as V<sub>CC</sub> falls below 4.5 volts (4.37 typical). The V<sub>CC<sub>TP</sub></sub> for the 5% op-

eration option (DS1238-5) is set for 4.75 volts (4.62 typical). The RST and R $\overline{S}T$  signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V<sub>CC</sub>. On power up, R $\overline{V}T$  will become inactive as soon as V<sub>CC</sub> rises above V<sub>CC<sub>TP</sub></sub>. However, the RST and R $\overline{S}T$  signals remain active for a minimum of 50 ms (100 ms typical) after V<sub>CC<sub>TP</sub></sub> is reached to allow the power supply and microprocessor to stabilize.

DS1238 FUNCTIONAL BLOCK DIAGRAM Figure 1



## WATCHDOG TIMER

The DS1238 provides a watchdog timer function which forces the  $\overline{WDS}$ ,  $RST$ , and  $\overline{RST}$  signals to the active state when the strobe input ( $\overline{ST}$ ) is not stimulated for a predetermined time period. This time period is described below in Table 1. The watchdog timeout period begins as soon as  $RST$  and  $\overline{RST}$  are inactive. If a high-to-low transition occurs at the  $\overline{ST}$  input prior to time out, the watchdog timer is reset and begins to time out again. The  $\overline{ST}$  input timing is shown in Figure 2. In order to guarantee that the watchdog timer does not timeout, a high-to-low transition on  $\overline{ST}$  must occur at or less than the minimum timeout of the watchdog as described in the AC Electrical Characteristics. If the watchdog timer is allowed to time out, the  $\overline{WDS}$ ,  $RST$ , and  $\overline{RST}$  outputs are driven to the active state.  $\overline{WDS}$  is a latched signal which indicates the watchdog status, and is activated as soon as the watchdog timer completes a full period as outlined in Table 1. The  $\overline{WDS}$  pin will remain low until one of three operations occurs. The first is to strobe the  $\overline{ST}$  pin with a falling edge, which will both set the  $\overline{WDS}$  as well as the watchdog timer count. The second is to leave the  $\overline{ST}$  pin open, which disables the watchdog. Lastly, the  $\overline{WDS}$  pin is active low whenever  $V_{CC}$  falls below  $V_{CCTP}$  and activates the  $\overline{RV\overline{T}}$  signal. The  $\overline{ST}$  input can be derived from microprocessor address, data, or control signals, as well as microcontroller port pins. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time out. The watchdog is disabled by leaving the  $\overline{ST}$  input open, or as soon as  $V_{CC}$  falls to  $V_{CCTP}$ .

## NON-MASKABLE INTERRUPT

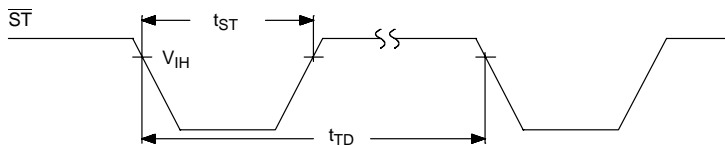
The DS1238 generates a non-maskable interrupt ( $\overline{NMI}$ ) for early warning of a power failure to the microprocessor. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply, or from a higher DC voltage level closer to the main system power

input. Since the IN trip point  $V_{TP}$  is 1.27 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1238 requires that the voltage at the IN pin be limited to  $V_{IH}$ . Therefore, the maximum allowable voltage at the supply being monitored ( $V_{MAX}$ ) can also be derived as shown in Figure 5. A simple approach to solving this equation is to select a value for R2 of high enough value to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between  $\overline{NMI}$  and  $RST$  or  $\overline{RST}$ .

When the supply being monitored decays to the voltage sense point, the DS1238 will force the  $\overline{NMI}$  output to an active state. Noise is removed from the  $\overline{NMI}$  power fail detection circuitry using built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33  $\mu$ s/cycle). Three consecutive samplings of out-of-tolerance supply (below  $V_{SENSE}$ ) must occur at the IN pin to active  $\overline{NMI}$ . Therefore, the supply must be below the voltage sense point for approximately 100  $\mu$ s or the comparator will reset. In this way, power supply noise is removed from the monitoring function preventing false trips. During a power-up, any IN pin levels below  $V_{TP}$  detected by the comparator are disabled from reaching the  $\overline{NMI}$  pin until  $V_{CC}$  rises to  $V_{CCTP}$ . As a result, any potential active  $\overline{NMI}$  will not be initiated until  $V_{CC}$  reaches  $V_{CCTP}$ .

Removal of an active low level on the  $\overline{NMI}$  pin is controlled by the subsequent rise of the IN pin above  $V_{TP}$ . The initiation and removal of the  $\overline{NMI}$  signal during power up depends on the relative voltage relationship between  $V_{CC}$  and the IN pin voltage. Note that a fast slewing power supply may cause the  $\overline{NMI}$  to be virtually non-existent on power up. This is of no consequence however, since an  $RST$  will be active. The  $\overline{NMI}$  voltage will follow  $V_{CC}$  down until  $V_{CC}$  decays to  $V_{BAT}$ . Once  $V_{CC}$  decays to  $V_{BAT}$ , the  $\overline{NMI}$  pin will enter a tri-state mode.

## $\overline{ST}$ INPUT TIMING Figure 2

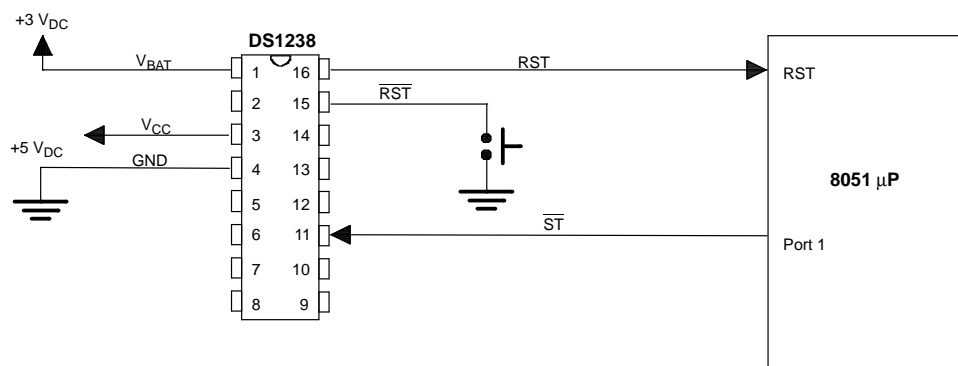


## OSCILLATOR CONTROLS Table 1

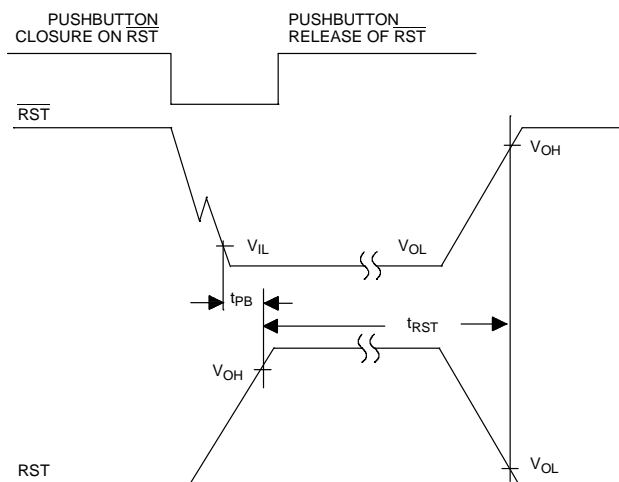
	OSCIN	OSCSSEL	Watchdog Timeout Period (typ)		Reset Active Duration
			First Period Following a Reset	Other Timeout	
External	Ext Clk	Low	20480 Clks	5120 Clocks	641 Clks
	Ext Cap	Low	$\cong \frac{2.2 \text{ sec}}{47 \text{ pf}} \times \text{Cpf}$	$\cong \frac{550 \text{ ms}}{47 \text{ pf}} \times \text{Cpf}$	$\cong \frac{69 \text{ ms}}{47 \text{ pf}} \times \text{Cpf}$
Internal	Low	Hi/Open	2.7 sec	170 ms	85 ms
	Hi/Open	Hi/Open	2.7 sec	2.7 sec	85 ms

Note that the OSCIN and OSCSEL pins are tri-stated when  $V_{CC}$  is below  $V_{BAT}$ .

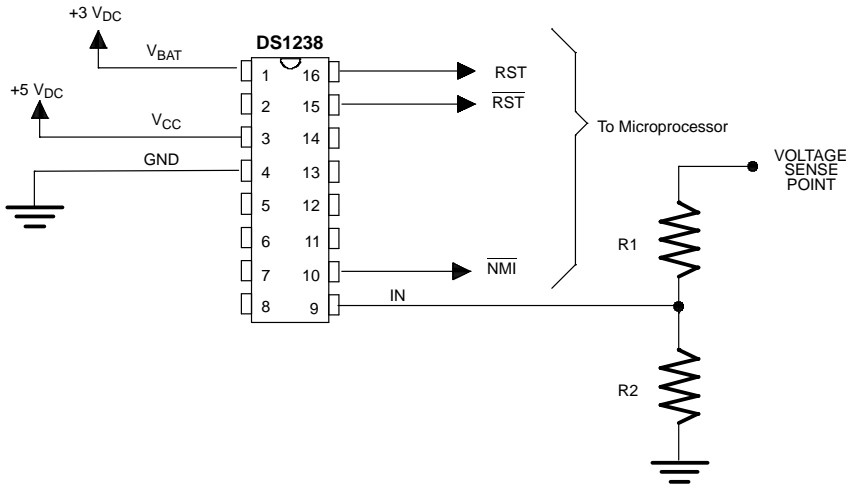
## POWER MONITOR, WATCHDOG TIMER, AND PUSHBUTTON RESET Figure 3



## PUSHBUTTON RESET TIMING Figure 4



**NON-MASKABLE INTERRUPT** Figure 5



$$V_{\text{SENSE}} = \frac{R1 + R2}{R2} \times 1.27$$

$$\text{MAXVOLTAGE} = \frac{V_{\text{SENSE}}}{1.27} \times 5.0 = \text{VMAX}$$

Example 1: 5 Volt Supply, R2 = 10K Ohms, VSENSE = 4.8 Volts

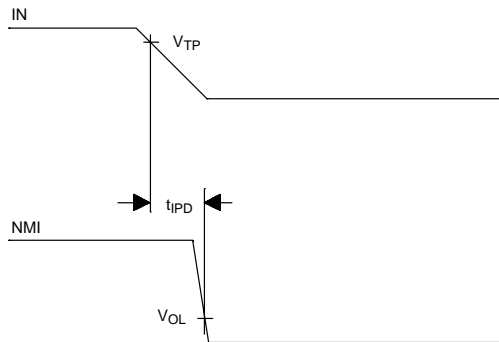
$$4.8 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1 = 27.8K \text{ Ohm}$$

Example 2: 12 Volt Supply, R2 = 10K Ohms, VSENSE = 9.0 Volts

$$9.0 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1 = 60.9K \text{ Ohm}$$

$$V_{\text{MAX}} = \frac{9.00}{1.27} \times 5.0 = 35.4 \text{ Volts}$$

**NMI FROM IN INPUT** Figure 6



## MEMORY BACKUP

The DS1238 provides all of the necessary functions required to battery back a static RAM. First, an internal switch is provided to supply SRAM power from the primary 5-volt supply ( $V_{CC}$ ) or from an external battery ( $V_{BAT}$ ), whichever is greater. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ( $\overline{CEO}$ ) to within 0.3 volts of  $V_{CC}$  or to within 0.7 volts of  $V_{BAT}$ . The output voltage diode drop from  $V_{BAT}$  (0.7 V) is necessary to prevent charging of the battery in violation of UL standards. Write protection occurs as  $V_{CC}$  falls below  $V_{CCTP}$  as specified. If  $\overline{CEI}$  is low at the time power fail detection occurs,  $\overline{CEO}$  is held in its present state until  $\overline{CEI}$  is returned high, or the period  $t_{CE}$  expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If  $\overline{CEO}$  is in an inactive state at the time of  $V_{CC}$  fail detection,  $\overline{CEO}$  will be unconditionally disabled within  $t_{CF}$ . During nominal supply conditions  $\overline{CEO}$  will follow  $\overline{CEI}$  with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

## FRESHNESS SEAL

In order to conserve battery capacity during storage and/or shipment of an end system, the DS1238 provides an internal freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will result in the tri-state of outputs  $V_{CCO}$ ,  $RST$ ,  $\overline{RST}$ , and  $\overline{CEO}$ . The  $\overline{WDS}$  output will be driven active low. The PF pin is not disabled by the

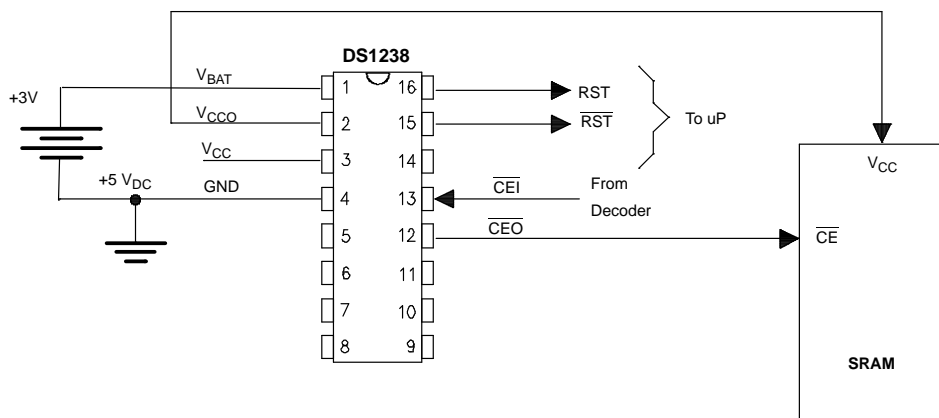
freshness mode and will continue to source power from the  $V_{BAT}$  pin whenever  $V_{CC}$  is below  $V_{BAT}$ . The freshness seal will be disconnected and normal operation will begin when  $V_{CC}$  is cycled and reapplied to a level above  $V_{BAT}$ .

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3-volt clock to TP1.

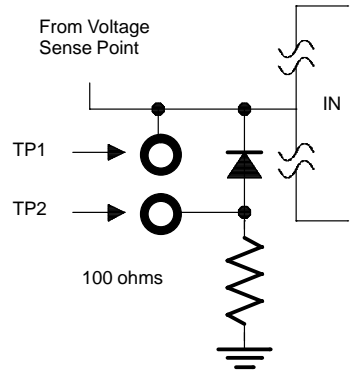
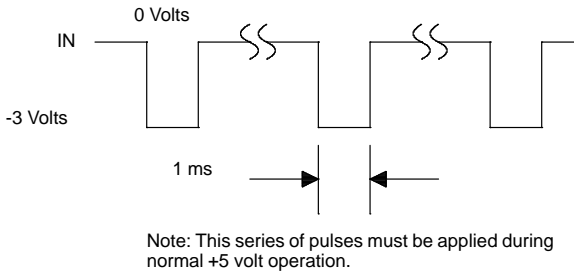
## POWER SWITCHING

When larger operating currents are required in a battery-backed system, the internal switching devices of the DS1238 may be too small to support the required load through  $V_{CCO}$  with a reasonable voltage drop. For these applications, the PF output is provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from  $V_{CC}$  to battery on power down, and from battery to  $V_{CC}$  on power up. The DS1336 is designed to use the PF output to switch between  $V_{BAT}$  and  $V_{CC}$ . It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF is set to the external battery voltage  $V_{BAT}$ , allowing a smooth transition between sources. Any load applied to the PF pin by an external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

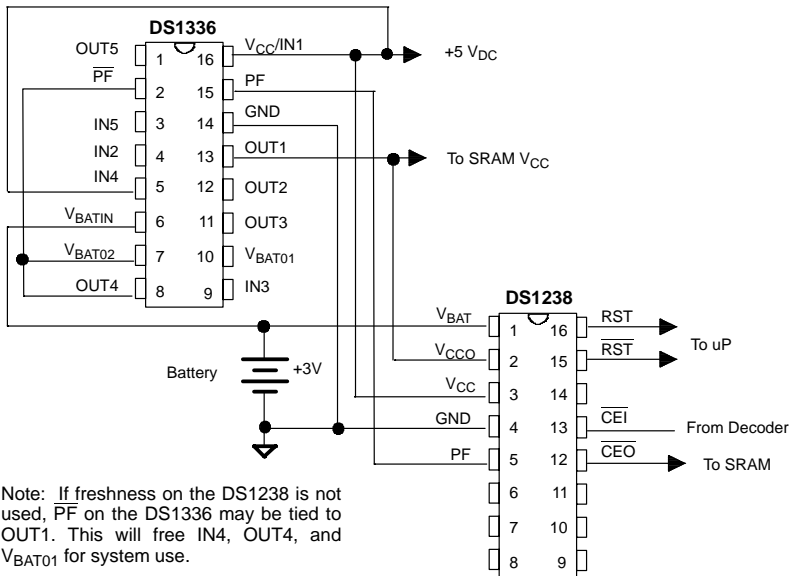
## NONVOLATILE SRAM Figure 7



**FRESHNESS SEAL** Figure 8



**POWER SWITCHING** Figure 9



**TIMING DIAGRAMS**

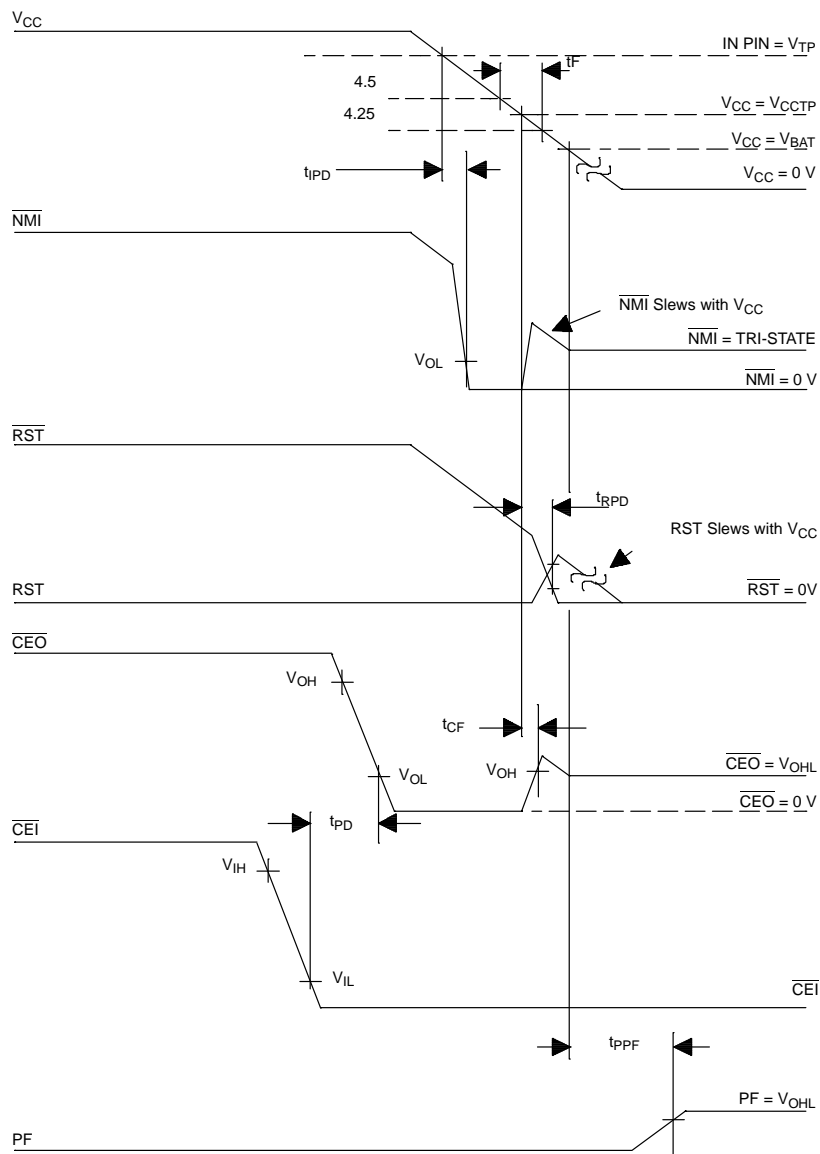
This section provides a description of the timing diagrams shown in Figure 10 and Figure 11. Figure 10 illustrates the relationship for power down. As  $V_{CC}$  falls, the IN pin voltage drops below  $V_{TP}$ . As a result, the processor is notified of an impending power failure via an active NMI. This gives the processor time to save critical data in nonvolatile SRAM. As the power falls further,  $V_{CC}$  crosses  $V_{CCTP}$ , the power monitor trip point. When  $V_{CC}$  reaches  $V_{CCTP}$ , and active RST and  $\overline{RST}$  are given. At this time,  $\overline{CEO}$  is brought high to write protect the

RAM. When the  $V_{CC}$  reaches  $V_{BAT}$ , a power fail is issued via the PF pin.

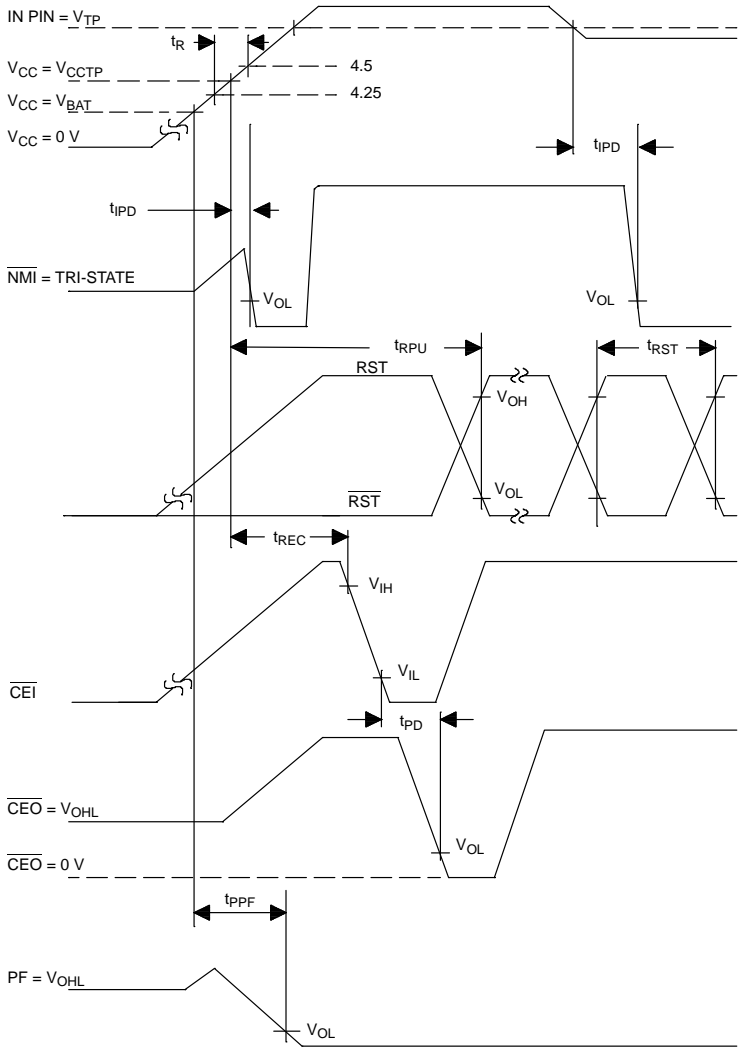
Figure 11 shows the power up sequence. As  $V_{CC}$  slews above  $V_{BAT}$ , the PF pin is deactivated. An active reset occurs as well as an NMI. Although the NMI may be short due to slew rates, reset will be maintained for the standard  $t_{RPU}$  timeout period. At a later time, if the IN pin falls below  $V_{TP}$ , a new NMI will occur. If the processor does not issue an  $\overline{ST}$ , a watchdog reset will also occur. The second NMI and RST are provided to illustrate these possibilities.



## POWER DOWN TIMING Figure 10



**POWER UP TIMING** Figure 11



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on $V_{CC}$ Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to $V_{CC} + 0.5V$
Voltage on IN Pin Relative to Ground	-3.5V to $V_{CC} + 0.5V$
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	$V_{CC}$	4.75	5.0	5.5	V	1
Input High Level	$V_{IH}$	2.0		$V_{CC}+0.3$	V	1
Input Low Level	$V_{IL}$	-0.3		+0.8	V	1
IN Input Pin	$V_{IN}$	0		$V_{CC}$	V	1
Battery Input	$V_{BAT}$	2.7		4.0	V	1

**DC ELECTRICAL CHARACTERISTICS**(0°C to 70°C;  $V_{DD} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	$I_{CC}$			4	mA	2
Battery Current	$I_{BAT}$	0		200	nA	2, 12
Supply Output Current ( $V_{CCO} = V_{CC} - 0.3V$ )	$I_{CCO1}$			100	mA	3
Supply Out Current ( $V_{CC} < V_{BAT}$ )	$I_{CCO2}$			1	mA	4
Supply Output Voltage	$V_{CCO}$	$V_{CC} - 0.3$			V	1
Battery Back Voltage	$V_{CCO}$		$V_{BAT} - 0.8$		V	6
Low Level @ RST	$V_{OL}$			0.4	V	1
Output Voltage @ -500 $\mu A$	$V_{OH}$	$V_{CC} - 0.5V$	$V_{CC} - 0.1V$		V	1
$\overline{CEO}$ and PF Output	$V_{OHL}$		$V_{BAT} - 0.8$		V	6
Input Leakage Current	$I_{LI}$	-1.0		+1.0	$\mu A$	121
Output Leakage	$I_{LO}$	-1.0		+1.0	$\mu A$	
Output Current @0.4V	$I_{OL}$			4.0	mA	9
Output Current @2.4V	$I_{OH}$	-1.0			mA	10
Power Sup. Trip Point	$V_{CCTP}$	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	$V_{CCTP}$	4.50	4.62	4.75	V	
IN Input Pin Current	$I_{CCIN}$	-1.0		+1.0	$\mu A$	
IN Input Trip Point	$V_{TP}$	1.15	1.27	1.35	V	1

**AC ELECTRICAL CHARACTERISTIC**(0°C to 70°C;  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$V_{CC}$ Fall Detect to RST, $\overline{RST}$	$t_{RPD}$	40	100	175	$\mu s$	
$V_{TP}$ to $\overline{NMI}$	$t_{IPD}$	40	100	175	$\mu s$	
RESET Active OSCSEL=high	$t_{RST}$	40	85	150	ms	
$\overline{ST}$ Pulse Width	$t_{ST}$	20			ns	13
PBRST @ $V_{IL}$	$t_{PB}$	30			ms	
$V_{CC}$ Slew Rate 4.75 to 4.25	$t_F$	300			$\mu s$	
Chip Enable Prop Delay	$t_{PD}$			20	ns	
$V_{CC}$ Fail to Chip Enable High	$t_{CF}$	7	12	144	$\mu s$	11
$V_{CC}$ Valid to RST (RC = 1)	$t_{FPU}$			100	ns	
$V_{CC}$ Valid to RST	$t_{RPU}$	40	100	150	ms	5
$V_{CC}$ Slew to 4.25 to $V_{BAT}$	$t_{FB1}$	10			$\mu s$	
Chip Enable Output Recovery Time	$t_{REC}$	0.1			$\mu s$	7
$V_{CC}$ Slew 4.25 to 4.75	$t_R$	0			$\mu s$	
Chip Enable Pulse Width	$t_{CE}$			5	$\mu s$	8
Watchdog Time Delay int clock Long period	$t_{TD}$	1.7	2.7		s	
Short period		110	170		ms	
Watchdog Time Delay, ext clock, After reset	$t_{TD}$		20480		clocks	
Normal			5120		clocks	
$V_{BAT}$ Detect to PF	$t_{PPF}$			2	$\mu s$	
OSC IN Frequency	$f_{OSC}$	0		250	KHz	

**CAPACITANCE** $(t_A = 25^\circ C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$			5	pF	
Output Capacitance	$C_{OUT}$			7	pF	

**NOTES:**

1. All voltages referenced to ground.
2. Measured with  $V_{CC0}$ ,  $\overline{CEO}$ , PF,  $\overline{ST}$ , RST,  $\overline{RST}$ , and  $\overline{NMI}$  pin open.
3.  $I_{CCO1}$  is the maximum average load which the DS1238 can supply at  $V_{CC}-3V$  through the  $V_{CC0}$  pin during normal 5-volt operation.
4.  $I_{CCO2}$  is the maximum average load which the DS1238 can supply through the  $V_{CC0}$  pin during data retention battery supply operation, with a maximum drop of 0.8 volts for commercial, 1.0V for industrial.
5. With  $t_R = 5 \mu s$ .
6.  $V_{CC0}$  is approximately  $V_{BAT}-0.5V$  at  $1 \mu A$  load.
7.  $t_{REC}$  is the minimum time required before  $\overline{CEI}/\overline{CEO}$  memory access is allowed.
8.  $t_{CE}$  maximum must be met to insure data integrity on power loss.
9. All outputs except RST which is  $25 \mu A$  max.
10. All outputs except  $\overline{RST}$ ,  $\overline{RVT}$ , and  $\overline{NMI}$  which is  $25 \mu A$  min.
11. The  $\overline{ST}$  pin will sink  $\pm 50 \mu A$  in normal operation. The OSCIN pin will sink  $\pm 5 \mu A$  in normal operation. The OSCSEL pin will sink  $\pm 10 \mu A$  in normal operation.
12.  $I_{BAT}$  is measured with  $V_{BAT}=3.0V$ .
13.  $\overline{ST}$  should be active low before the watchdog is disabled (i.e., before the  $\overline{ST}$  input is tristated).

