CIRRUS LOGIC®

# CL-MD1414UXX

*Data Book*

## FEATURES

- **International telephony support**
  - — Call progress and black listing
  - — CCITT V.23 and V.21 data modes
- **Flash memory interface**
  - — Firmware-upgradeable microcontroller
  - — Programmable manufacturer-specific parameters
- **Caller ID and distinctive ringing**
- **Telephone-Emulation mode (speakerphone)**
- **Three DTE (data terminal) interfaces available**
  - — PC card (PCMCIA) bus interface
    - Direct connection to a PC card bus
    - 16C550A/16C450 register-compatible UART
    - Manufacturer-programmable internal CIS
    - DMA for Voice playback and record modes
  - — Parallel bus interface
    - Direct connection to PC ISA bus
    - Direct connection to PC ISA bus plug-and-play interface with pin-compatibility
    - 16C550A/16C450 register-compatible UART
    - Built-in COM 1–4 address decoding and bus drivers
    - DMA for Voice playback and record modes
  - — Serial RS-232 (V.24)
- **Voice mode**
  - — Embedded voice mode AT command set
  - — Sample Rates: 4800, 7200, 8000, 9600, 11025, and 22050 bps
  - — Compression: ADPCM, Linear, and CL1
  - — Radish® VoiceView™

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## Universal 14,400-bps Data/Fax/Voice Modem Device Set Family (Two-Chip Set)

## OVERVIEW

The CL-MD1414UXX, the Cirrus Logic Universal, is a complete, intelligent, multi-mode modem combining data, fax, and voice features in only two devices, a DSµP (Digital Signal Microprocessor) and a SAFE (Sigma-Delta Analog Front End).

The CL-MD1414UXX operates up to 14,400 bps as a data and fax (transmit and receive) modem, and is intended for stand-alone, ISA bus card, and PC card (PCMCIA) applications. No additional firmware development is required for this complete solution.

The Universal provides the standard data, EIA/TIA-578 Class 1 and EIA/TIA-592 Class 2 fax AT commands. In addition, the Universal includes a voice and V.42/MNP® 2–4 error correction and V.42 bis/MNP 5 data compression command set to ensure fast error-free data transfer during data modem connections. The Universal implements a voice mode AT command set, that enables a host computer and the CL-MD1414UXX to emulate a telephone answering machine and telephone.

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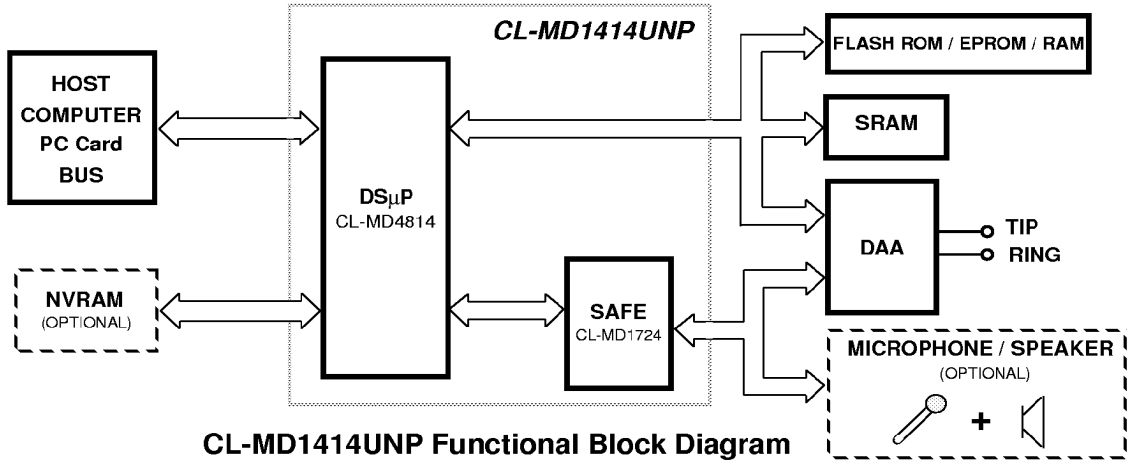



**CL-MD1414UNP Functional Block Diagram**

**Version 1.2**

***November 1995***

## FEATURES (cont.)

- **Data modem modes**
  - CCITT: V.32 bis, V.32, V.23, V.22 bis, V.22, and V.21
  - Bell®: 212A and 103
  - Speeds: 14400, 12000, 9600, 7200, 4800, 2400, 1200, and 300 bps
  - Industry-standard AT command set
- **Fax Modem Send and Receive modes**
  - CCITT: V.17, V.29, V.27 ter, and V.21 ch2
  - Speeds: 14400, 12000, 9600, 7200, 4800, 2400, and 300 bps
  - Supports Group 3 fax
  - EIA/TIA-578 Class 1 Fax AT command set
  - EIA/TIA-592 Class 2 Fax AT command set
- **V.42/MNP® protocols**
  - Error correction: V.42 and MNP® 2–4
  - Data compression: V.42 bis and MNP® 5
- **Microphone interface**
- **Low power requirement**
  - Automatic sleep (power-down) and wake-up
  - Operates from a single +5-V power supply
  - Typical power requirements for CL-MD1414US/UN:
    - Operating power: 450 mW
    - Sleep mode: 40 mW
    - Stop mode: 50 µW
  - Typical power requirements for CL-MD1414USP/UNP:
    - Operating power: 450 mW
    - Sleep mode: 40 mW
- **Small package dimensions**
  - DSµP (CL-MDXX14): 128-pin SQFP or 120-pin VQFP
  - SAFE (CL-MD1724): 44-pin VQFP

## OVERVIEW (cont.)

New voice features in the Universal include higher sampling rates (4800, 7200, 8000, 9600, 11025, and 22050 samples/sec.), speakerphone, and Radish® VoiceView™.

The Universal also offers an extended data, EIA/TIA-578 Class 1 and EIA/TIA-592 Class 2 fax, and voice AT command set interpreter, which is embedded in the device sets. This allows system designers to develop a Hayes® compatible modem with minimal effort.

The CL-MD1414UXX offers several hardware interfaces. The Universal can host interface in serial RS232, parallel bus, plug-and-play, and PC card modes. Additionally, the CL-MD1414UXX supports expansion bus, NVRAM, DAA, speaker, microphone, and flash memory interfaces.

The flash memory interface is a new feature to the Cirrus Logic modem devices. It allows end-users and modem designers to download new firmware easily and quickly. It works by downloading the new firmware through the UART interface to a flash ROM or RAM.

### APPLICATIONS

- Notebook computers
- PDA applications
- ISA bus modems
- Box modems
- Pocket modems
- PC cards

## ADVANTAGES

| Unique Features | Benefits |
|---|---|
| ***Downloadable flash memory interface*** | Allows end-users to download firmware upgrades |
| ***.wave-compatible sample rates and compression (with DTMF detection)*** | Allows playing or recording of .wave files without a file translation program |
| ***Direct connection to PC ISA bus or PC card bus*** | Eliminates the need for bus drivers, address decoding logic, PC card interface chip, and CIS ROM |
| ***14400-bps fax transmission and reception*** | Latest fax standard reduces telephone connect time |
| ***16C550A register-compatible UART*** | Supports enhanced communication software for improved data throughput |
| ***Small package sizes*** | Minimizes board area |
| ***Power-management modes*** | Reduces power consumption over 92 percent |
| ***Requires a single +5-V power supply*** | Simplifies board design |

# Table of Contents

# 1. FUNCTIONAL BLOCK DIAGRAMS

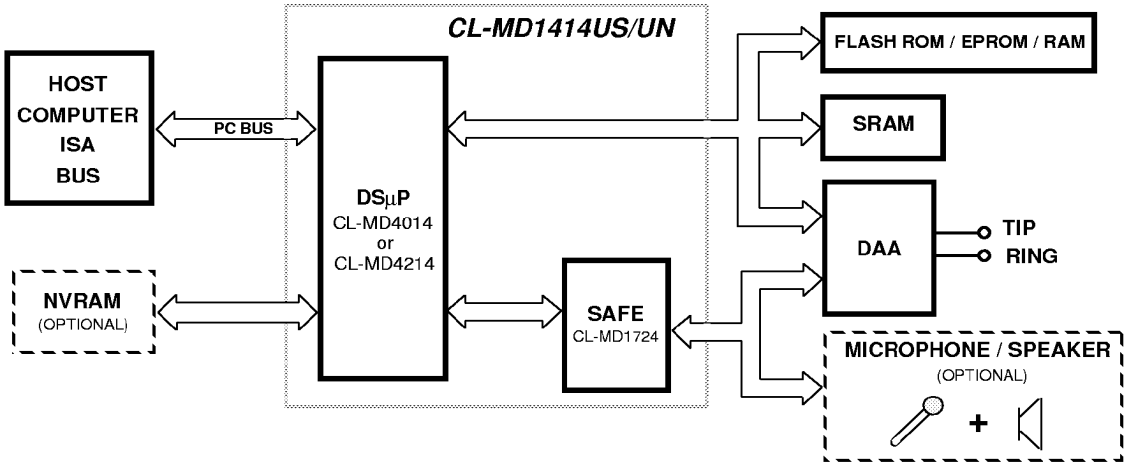



**Figure 1-1. CL-MD1414US/UN Functional Block Diagram**

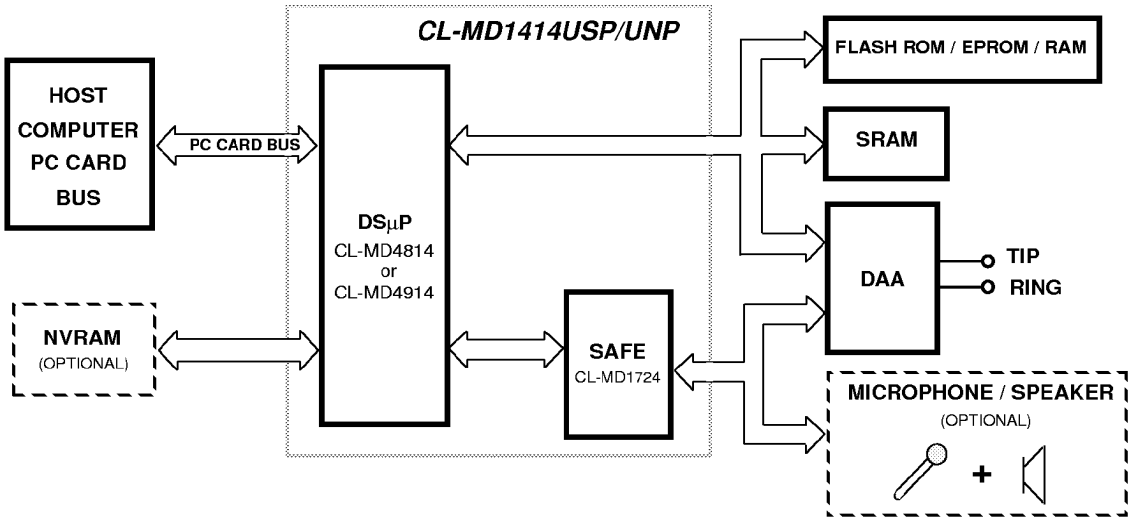



**Figure 1-2. CL-MD1414USP/UNP Functional Block Diagram**

# 2. DEVICE SET DESCRIPTION

The CL-MD1414UXX Cirrus Logic Universal product family is a two-chip solution consisting of a DSµP (digital signal microprocessor) and a SAFE (sigma-delta analog front end) device. The Universal family supports a variety of applications and needs no additional firmware development. Currently there are four CL-MD1414UXX device set solutions. These are shown with their corresponding DSµP and SAFE part numbers in Figure 2-1. Each Universal device set is defined by two or three of the following suffixes:

- *U* Universal 2-chip device set (data/fax/voice with MNP 2–5/V.42/V.42 bis)
- *N* International version
- *S* U.S. version
- *P* PC card interface
- *T* Plug-and-play interface

## 2.1 DSµP (Digital Signal Microprocessor)

One of the two chips in the Universal product is the DSµP. The DSµP performs the functions of a microprocessor and DSP. It implements all of the AT commands, manages data transmission and reception, controls the SAFE, and interfaces with the DTE. The DSµP's internal ROM contains code for all the DSP functions for Group 3 fax mode, data mode (without error correction or data compression), and voice mode.

## 2.2 SAFE (Sigma-Delta Analog Front End) Device

The Universal product's second chip is the SAFE device. This uses sigma-delta techniques to convert analog information from a telephone line to digital information that can be processed by the DSµP. In addition to its analog circuitry, the SAFE chip incorporates unique and proprietary sigma-delta digital-to-analog and analog-to-digital functions. These features improve receiver accuracy, which in turn improves performance at low receive-signal levels. The sigma-delta implementation better stabilizes the SAFE device's functions and makes them less sensitive to board layout than other analog front-end technologies. Since a significant amount of signal processing is performed by digital rather than analog techniques, sigma-delta analog-to-digital conversion considerably improves signal quality.

| Market | Parallel/Serial Host Interface | PC card (PCMCIA) Host Interface | Plug-and-Play Interface |
|---|---|---|---|
| United States | **CL-MD1414US**<br>DSµP (CL-MD4214) + SAFE (CL-MD1724) | **CL-MD1414USP**<br>DSµP (CL-MD4914) + SAFE (CL-MD1724) | **CL-MD1414UST**<br>DSµP (CL-MD4314) + SAFE (CL-MD1724) |
| International (including U.S.) | **CL-MD1414UN**<br>DSµP (CL-MD4014) + SAFE (CL-MD1724) | **CL-MD1414UNP**<br>DSµP (CL-MD4814) + SAFE (CL-MD1724) | **CL-MD1414UNT**<br>DSµP (CL-MD4514) + SAFE (CL-MD1724) |

**Figure 2-1. Device Set Composition**

# 3. MODES OF OPERATION

The Universal device sets provide the complete modem functions for Group 3 fax, data, voice, V.42/MNP 2–4 and V.42 bis/MNP 5 (Microcom Networking Protocol Class 5) modes of operation. Each of these modes has its own unique AT command set. The data rates and modulation schemes for data and fax modes are presented in Table 3-1 on page 8. Additionally, the Universal device sets provide special modes of operation for Radish VoiceView, power management, and loopback testing.

## 3.1 Data Mode

In the data mode, the Universal device set operates up to 14,400 bps and implements all of the data rates and modulation schemes for CCITT standards V.32 bis, V.32, V.22 bis, V.22, V.21, Bell 212A, and Bell 103. The Universal device set uses a standard data mode AT command set compatible with any communication application software that supports the Hayes AT command set. The standard AT commands for data mode are listed in Table 5-1 on page 16.

## 3.2 Fax Mode

In the fax mode, the Universal device set operates up to 14,400 bps (transmit and receive) and implements all of the data rates and modulation schemes in CCITT standards V.17, V.29, V.27 ter, and V.21 ch2. The Universal implements a standard fax mode AT command set that is compatible with any communication application software that supports EIA/TIA-578 Fax Class 1 or EIA/TIA-592 Fax Class 2 standards. The standard AT commands for fax mode are listed in Table 5-3 on page 17 and Table 5-4 on page 17.

## 3.3 Voice Mode

The Universal device set supports Telephone-Emulation mode, as well as message record and play back capabilities. Telephone-Emulation mode allows a handset/microphone-speaker and modem to be used as a complete telephone. In Telephone-Emulation mode, the received data from the SAFE (CL-MD1724) microphone interface is looped back to the SAFE analog transmit pins. In voice mode, the message record and play back abilities are accessed by the extended AT command set shown in Table 5-8 on page 18.

## 3.4 V.42/MNP® 2–4 and V.42 bis/MNP® 5 Modes

The Universal supports error correction (V.42/MNP 2–4) and data compression (V.42 bis/MNP 5). Error correction ensures error-free data transfer. Data compression substantially increases the modem data throughput over the basic data rate throughput. Depending on the data stream, MNP 5 may provide up to 2-to-1 compression. Alternately, CCITT V.42 bis may provide up to 4-to-1 compression. A description of the AT commands and S-registers that support error correction and data compression are provided in Table 5-3 on page 17.

## 3.5 Radish® VoiceView™ Mode

The CL-MD1414UXX supports Radish® VoiceView™, a widely supported protocol that alternates voice and data. VoiceView enables data transfer during a regular telephone connection. It can be used in a variety of applications, such as customer service and technical support.

**Table 3-1. Communication Modes and Data Rates**

| Application | Mode | Data Rate (bps) | Modulation | Baud Rate (symbols/sec.) | Carrier Frequency (Hz) (originate/answer) | Constellation Points |
|---|---|---|---|---|---|---|
| Fax | V.17 | 14,400 | TCM | 2400 | 1800 | 128 |
| | | 12,000 | TCM | 2400 | 1800 | 64 |
| | | 9600 | TCM | 2400 | 1800 | 32 |
| | | 7200 | TCM | 2400 | 1800 | 16 |
| | V.29 | 9600 | QAM | 2400 | 1700 | 16 |
| | | 7200 | QAM | 2400 | 1700 | 8 |
| | | 4800 | QAM | 2400 | 1700 | 4 |
| | V.27 ter | 4800 | DPSK | 1600 | 1800 | 8 |
| | | 2400 | DPSK | 1200 | 1800 | 4 |
| | V.21 | 300 | FSK | 300 | 1650 M<br>1850 S | 1 |
| Data | V.32 bis | 14,400 | TCM | 2400 | 1800 | 128 |
| | | 12,000 | TCM | 2400 | 1800 | 64 |
| | | 9600 | TCM | 2400 | 1800 | 32 |
| | | 7200 | TCM | 2400 | 1800 | 16 |
| | | 4800 | QAM | 2400 | 1800 | 4 |
| | V.32 | 9600 | TCM | 2400 | 1800 | 32 |
| | | 9600 | QAM | 2400 | 1800 | 16 |
| | | 4800 | QAM | 2400 | 1800 | 4 |
| | V.22 bis | 2400 | QAM | 600 | 1200/2400 | 16 |
| | V.22 | 1200 | DPSK | 600 | 1200/2400 | 4 |
| | V.21 | 300 | FSK | 300 | 980 M/1650 M<br>1180 S/1850 S | 1 |
| | Bell 212A | 1200 | DPSK | 600 | 1200/2400 | 4 |
| | Bell 103 | 300 | FSK | 300 | 1270 M/2225 M<br>1070 S/2025 S | 1 |

**NOTES**: M = Mark S = Space FSK = Frequency Shift Keying QAM = Quadrature Amplitude Modulation DPSK = Differential Phase Shift Keying TCM = Trellis-Coded Modulation

## 3.6 Power Management Modes

The CL-MD1414UXX provides both sleep and stop modes to reduce power consumption when the modem is inactive. Stop mode turns off the modem power except for the circuitry required to maintain the host interface signals at the appropriate high-impedance state. To enter stop mode, the host asserts the DSμP stop pin. When the stop pin is deasserted, the modem exits stop mode, performs an internal reset and enters power-on mode.

After the modem internal reset, the DTE reconfigures the modem.

Power-on mode consists of an operational mode and a sleep (or power-down) mode. In operational mode, the modem device set is fully powered and is either communicating with the host and/or another modem, or is performing some internal processing. In sleep mode, power to most of the internal circuitry of the DSμP and SAFE is turned off. Sleep mode is controlled by S-register **S30**. When enabled, the DSμP will enter sleep or power-down mode whenever the modem has been inactive for a user-programmable time delay. The modem is considered to be in an inactive state when

1) no internal processing is being performed;
2) there is no activity between the host and the modem within a specified time period (S-register **S30**);
3) the modem is on-hook.

The modem exits sleep mode whenever the host reads or writes to the modem, or a ring signal is detected.

The parallel and serial host interface power requirements for each power mode are presented in Table 3-2**.** The PC card host interface power requirements for each power mode are presented in Table 3-3.

**Table 3-2. CL-MD1414US/UN Power Requirement**

| Mode | Typical @ 25°C | | Maximum @ 0°C | |
|---|---|---|---|---|
| | Current | Power | Current | Power |
| Operational | 90 mA | 450 mW | 135 mA | 675 mW |
| Sleep (power-down) | 8 mA | 40 mW | 15 mA | 75 mW |
| Stop (power-off) | 10 μA | 50 μW | 1 mA | 5 mW |

**Table 3-3. CL-MD1414USP/UNP Power Requirement**

| Mode | Typical @ 25°C | | Maximum @ 0°C | |
|---|---|---|---|---|
| | Current | Power | Current | Power |
| Operational | 90 mA | 450 mW | 135 mA | 675 mW |
| Sleep (power-down) | 8 mA | 40 mW | 15 mA | 75 mW |

## 3.7 Loopback Test Modes

Local and remote digital and analog loop tests are provided for testing modem-to-modem and modem-to-DTE communication integrity. These tests are accessed through the AT&Tn command, and are explained in more detail in the *CL-MD1414UXX Programmer's Guide*.

## 3.8 Transmit Levels

The factory default transmit level is –10 dBm ± 1 dB at tip and ring.The transmit level is programmable by using the firmware configuration utility.

## 3.9 Transmit Tone Levels

The modem generates DTMF, answer, call, and guard tones. The specification for each tone is provided in Tables 3-4 and 3-5. DTMF tones are transmitted at –6 dBm for Tone 1 and –4 dBm for Tone 2.

## 3.10 Receive Level

The receiver can accommodate a receive signal from –9 dBm to –43 dBm. The DCD (data carrier detect) function is activated at –43 dBm and above; it is deactivated at –48 dBm and below.

### 3.10.1 Receiver Tracking

The receiver compensates for up to ±7 Hz of carrier-frequency offset.

### 3.10.2 Equalizers

Automatic adaptive and compromise equalizers are provided to compensate for line distortions.

### 3.10.3 Call Progress

The modem monitors the detection of call-progress tones during call origination and reports them to the DTE. Call-progress tones include dial tone, busy tone, ring back, and answer tone.

### 3.10.4 Caller ID

Caller ID is a service that allows the user to see the telephone number of the caller before answering the call. The user also receives information on call date and time. This service is not available in some locations due to Central Office telephone equipment limitations and legal prohibition.

For more detailed information, refer to Appendix A of the *CL-MD1414UXX Programmer's Guide*.

### 3.10.5 International Support

The Universal modem supports international applications. For specific country settings, modify and download new modem specifications using the configuration utility supplied by Cirrus Logic. For information on specific countries, contact your local Cirrus Logic sales representative listed on the back cover of this document.

**Table 3-4. DTMF Tone Pairs**

| Dial Digit | Tone 1 (Hz) | Tone 2 (Hz) |
|---|---|---|
| 0 | 941 | 1336 |
| 1 | 697 | 1209 |
| 2 | 697 | 1336 |
| 3 | 697 | 1447 |
| 4 | 770 | 1209 |
| 5 | 770 | 1336 |
| 6 | 770 | 1477 |
| 7 | 852 | 1209 |
| 8 | 852 | 1336 |
| 9 | 852 | 1447 |
| * | 941 | 1209 |
| # | 941 | 1447 |
| A | 697 | 1633 |
| B | 770 | 1633 |
| C | 852 | 1633 |
| D | 941 | 1633 |

**Table 3-5. Transmit Tones**

| Tone | Value | Application |
|---|---|---|
| Calling tone | 1100 Hz | Fax originator |
| | 1300 Hz | Data originator |
| Answer tone | 2100 Hz | Data/fax (CCITT) |
| | 2225 Hz | Data (Bell mode) |
| Guard tone | 1800 Hz | Data/fax (answer mode) |
| | 500 Hz | |

# 4. HARDWARE INTERFACES

The Universal device sets support hardware interfaces for the host, flash memory, expansion bus, NVRAM, DAA, speaker, microphone, and general-purpose I/O pins. The hardware interfaces are demonstrated in Figure 4-1, the CL-MD1414UN system block diagram.

## 4.1 Host Interfaces

All CL-MD1414UXX device sets, except the USP/UNP, can support either a parallel or a serial host interface. The interface type is selected by connecting the DSµP HOSTSEL[1:0] pins to $V_{CC}$ or ground. The CL-MD1414USP/UNP integrates a PC card host interface.

### 4.1.1 Serial RS-232 Interface

When using TTL levels, the serial interface is compatible with an RS-232 interface. The serial interface also provides LED drivers for commonly used status information such as AA (auto-answer enable) and OH (modem off-hook). See Section 6.4.1, "DSµP Parallel/Serial (RS-232) Host Interface Pin Descriptions," for a complete list of LED drivers.

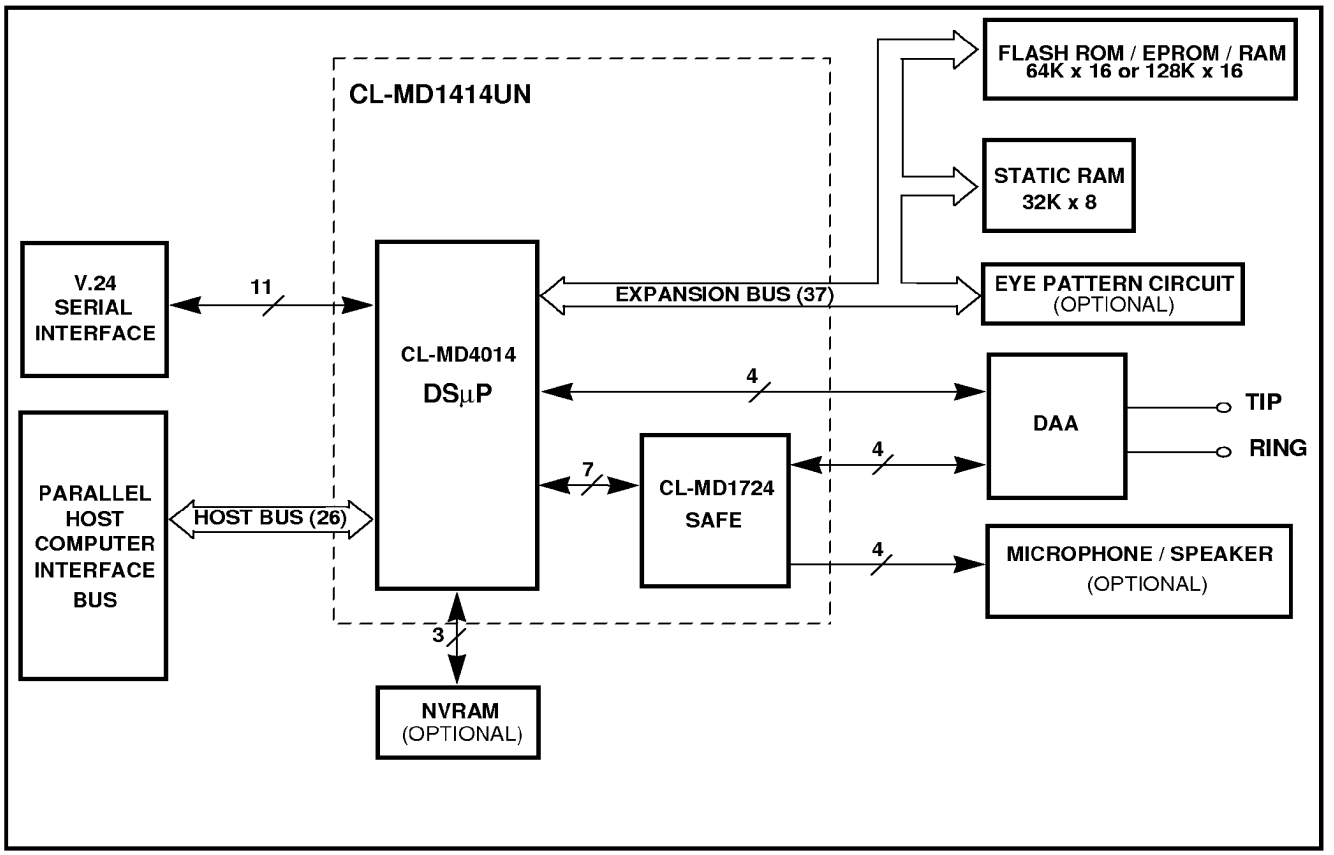



**Figure 4-1. Modem System Block Diagram (CL-MD1414UN)**

### 4.1.2 Parallel Bus Interface

The parallel interface emulates the electrical and register functions of a 16C550A and 16C450 UART. Upon modem reset, the UART interface defaults to a 16C450. The DTE can then configure the UART to function as a 16C550A. Table 4-1 shows the UART register bit assignments.

The parallel UART interface can be selected to internally decode the addresses for COM 1–4. For applications not utilizing COM 1–4, the standard method of selecting the modem with external address decoding is also provided. The type of address decoding is selected by either asserting or deasserting the signal at the DSμP ADRDEC hardware pin.

The parallel UART also provides an internal tristate bus interface that eliminates the need for external bus drivers between the host bus and the modem UART. These features eliminate the need for a 74HCT245 and a 74HCT30 device, and facilitates system designs with lower chip counts, power requirements, and costs.

### 4.1.3 Plug-and-Play Interface

Additionally, future revisions of the Universal will support a parallel plug-and-play host interface. These plug-and-play device sets are pin-compatible with the SQFP non-plug-and-play device sets. This pin compatibility allows an OEM to design one board to support both plug-and-play and non-plug-and-play PC bus applications. The additional plug-and-play pin requirements are described in Section 6.4.1 on page 27.

### 4.1.4 PC Card Interface

The CL-MD1414USP/UNP integrates a PC card host interface that allows the modem to be connected directly to a PC card bus without additional hardware. This host interface also provides a 16C450/16C550 register-compatible UART. Upon modem reset, the UART interface defaults to a 16C450. The DTE can then configure the UART to function as a 16C550A. Table 4-1 shows the UART register bit assignments.

A built-in 256 × 8 CIS RAM eliminates the need for an external CIS ROM. The CIS contents, which are stored in the external DSμP microcontroller memory (such as flash ROM or EPROM) are downloaded into the internal CIS RAM during the modem power-on sequence.

To customize the modem design, the CIS may be overridden by changing the microcontroller firmware CIS contents using the modem flash download utility program.

## 4.2 Flash Interface

A flash interface is provided for OEMs and end users to be able to quickly and easily download new features as they become available. The Universal flash interface works with the parallel and PC card host interfaces, and allows the microcontroller firmware code to be downloaded from a PC to the modem flash ROM or RAM. When firmware is downloaded it goes through the UART interface, thus eliminating the need for additional address space and extra hardware, as required by competing designs.

## 4.3 The Expansion Bus Interface

An expansion bus provides access to external memory and circuitry. The expansion bus is used for the DSμP microcontroller firmware and SRAM. The bus access time for the DSμP's microcontroller firmware is 70 ns for the DSμP's flash RAM/ROM, RAM, and EPROM. This memory device can be 64K ×16 bits or 128K ×16 bits.

A 32K × 8 120-ns SRAM is required for all CL-MD1414-based modems. The SRAM is used to buffer data during data, voice, fax, and V.42/MNP modes of operation.

## 4.4 NVRAM Interface

A serial interface is provided for optional non-volatile RAM (NVRAM). A NVRAM may be used for storing modem configurations and telephone numbers.

## 4.5 DAA Interface

A DAA interface is provided to control the telephone line off-hook relays, to detect ring signals, and to transmit and receive analog signals.

## 4.6 Speaker Interface

The SAFE internally implements both the volume control and amplifier necessary to drive an external speaker. The output of the internal amplifier can be connected directly to a speaker or to the input of the host speaker amplifier. The internal amplifier is capable of driving a minimum load of 8 Ω. The speaker volume is controlled by the **ATLn** command.

## 4.7 Microphone Interface

The CL-MD1724 SAFE device provides a microphone interface for connecting a microphone or handset to the modem with a minimum of external parts. This microphone input can then be used for local-voice-record mode or for Telephone-Emulation mode. This interface is controlled by the **AT#VLN=n** command.

## 4.8 General-Purpose I/O Interface

To customize the modem design, the DSμP provides eight general-purpose input pins and eight general-purpose output pins that can be used to control or monitor external circuitry.

Some of the general-purpose output pins may be configured for specific functions (such as a Caller ID relay CIDREL*). The functions of these pins can be selected using the microcontroller firmware configuration utility program.

The general-purpose input pins may be configured to provide information to the DTE whenever the signal at the pins changes polarity. Additionally, the host can query the modem for the signal states at these pins. The functions of these pins can also be configured using the microcontroller firmware configuration utility program.

The following two AT commands are used to control these pins:

1) AT#VIN
2) AT#VOUT=n

**Table 4-1. Parallel Host Interface UART Register Bit Assignments**

| REGISTER ADDRESS | REGISTER NAME | BIT NUMBER | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 7 | Scratch Register (SCR) | Scratch Register (SCR) | | | | | | | |
| 6 | Modem Status Register (MSR) | Data Carrier Detect (DCD) | Ring Indicator (RI) | Data Set Ready (DSR) | Clear to Send (CTS) | Delta Data Carrier Detect (DDCDD) | Trailing Edge of Ring Indicator (TERI) | Delta Data Set Ready (DDSR) | Delta Clear to Send (DCTS) |
| 5 | Line Status Register (LSR) | Error in RCVR FIFO (Note 1) | Transmitter Empty (TEMT) | Transmitter Holding Register Empty (THRE) | Break Interrupt (BI) | Framing Error (FE) | Parity Error (PE) | Overrun Error (OE) | Data Ready (DR) |
| 4 | Modem Control Register (MCR) | 0 | 0 | 0 | Loop | Out 2 | Out 1 | Request to Send (RTS) | Data Terminal Ready (DTR) |
| 3 | Line Control Register (LCR) | Divisor Latch Access Bit (DLAB) | Set Break (SBRK) | Stick Parity (SPAR) | Even Parity Select (EPS) | Parity Enable (PEN) | Number of Stop Bits (STB) | Word Length Select Bit 1 (WLS1) | Word Length Select Bit 0 (WLS0) |
| 2 | FIFO Control Register [write only] (FCR) | RCVR Trigger (MSB) | RCVR Trigger (LSB) | Reserved | Reserved | DMA Mode Select (DMA) | XMIT FIFO Reset (XFIFOR) | RCVR FIFO Reset (RFIFOR) | FIFO Enable (FIFOE) |
| 2 | Interrupt Identity Register [Read only] (IIR) | FIFOs Enabled (See note) | FIFOs Enabled (See note) | 0 | VDMA | Interrupt ID Bit 2 (See note ) | Interrupt ID Bit 1 | Interrupt ID Bit 0 | '0' if Interrupt pending |
| 1 DLAB=0 | Interrupt Enable Register (IER) | 0 | 0 | 0 | 0 | Modem Status Interrupt Enable (MSIE) | Receiver Line Status Interrupt Enable (RLSIE) | Transmitter Holding Reg. Empty Int. Enable (THREIE) | Received Data Available Int. Enable (RDAIE) |
| 0 DLAB=0 | Transmit Holding Register [Write only] (THR) | Transmit Holding Register (THR) [Write only] | | | | | | | |
| 0 DLAB=0 | Receiver Buffer Register [Read only] (RBR) | Receiver Buffer Register (RBR) [Read only] | | | | | | | |
| 1 DLAB=1 | Divisor Latch (MS) (DLM) | Divisor Latch (MS) | | | | | | | |
| 0 DLAB=1 | Divisor Latch (LS) (DLL) | Divisor Latch (LS) | | | | | | | |

**NOTE:** These bits are always '0' in 16C450 mode.

# 5. AT COMMAND SET

## 5.1 AT Command Description

The CL-MD1414UXX's AT command set and S-registers are divided into four categories: Group 3 fax, data, V.42/MNP and voice. Tables 5-1 through 5-14 provide summaries of all the commands, while Table 5-15 provides a summary of all the S-registers.

All command lines sent to the modem, except for **A/**, must be preceded by an 'AT' and terminated by the contents of S-register **S3** (typically a carriage return <CR>). 'AT' stands for 'attention', and prompts the modem to receive a command line from the DTE. A <CR> informs the modem that the entire command string has been transmitted and that it should begin processing all the commands within the command line. A command line may include one or more AT commands, and may or may not be separated by a space. One exception to this is the set of fax commands. Each fax AT command in a multiple-command line must be separated by a semicolon (;).

Examples:

ATS1?<CR>
A/
AT &F &D2 +FCLASS=? <CR>
AT +FCLASS=80; S0=1<CR>

The modem provides status information to the DTE in the form of response codes. The supported response codes are listed in Tables 5-16 through 5-19.

After sending an AT command string to the modem, the DTE must wait for a response code from the modem before sending a new AT command string to the modem.

## 5.2 AT Escape Sequence

The CL-MD1414UXX provides two industry-standard escape sequences. The supported escape sequences are the TIES (Time Independent Escape Sequence) and the Hayes® Escape Sequence.

Currently, most modems implement the Hayes Escape Sequence; however, because licensing from Hayes may be required, TIES provides an alternative. TIES is an escape sequence designed to work with existing communication software written for the Hayes Escape Sequence.

**TIES/Hayes® Escape Sequences**

The Cirrus Logic CL-MD1414UXX Modem Device Set is manufactured with the TIES (Time Independent Escape Sequence) as the default setting. The firmware utility can be used to change the default from TIES to Hayes Escape Sequence. However, it is Hayes' position that you must either have or obtain a valid licence from Hayes Micro Computer of Norcross, Georgia before producing modem systems that utilize the Hayes Escape Sequence.

*Cirrus Logic accepts no responsibility and does not indemnify nor in any way provide protection for patent or possible patent violations to its customers or users of its products.*

**Table 5-1. Basic Data Modem AT Commands**

| Command | | Default | Function |
|---|---|---|---|
| A/ | ** | none | Repeat last command |
| A | | none | Answer |
| Bn | * | 1 | Select CCITT or Bell |
| Cn | | 1 | Carrier control option |
| D | | none | Dial command |
| En | * | 1 | Command echo |
| Fn | | 1 | Online echo |
| Hn | | 0 | Switch hook control |
| In | | 0 | Identification/checksum |
| Kn | | 1 | SRAM buffer control |
| Ln | * | 2 | Speaker volume control |
| Mn | * | 1 | Speaker control |
| Nn | * | 1 | Connection data rate control |
| On | | 0 | Go on line |
| P | * | none | Select pulse dialing |
| Qn | * | 0 | Result code display control |
| Sn | | none | Select an S-register |
| Sn=x | | none | Write to an S-register |
| Sn? | | none | Read from an S-register |
| T | * | none | Select DTMF dialing |
| Vn | * | 1 | Result code form |
| Xn | * | 4 | Result code type |
| Yn | * | 0 | Long space disconnect |
| Zn | | 0 | Recall stored profile |
| &Cn | * | 1 | DCD option |
| &Dn | * | 2 | DTR option |
| &F | | none | Load factory defaults |
| &Gn | * | 0 | Guard tone option |
| &Jn | * | 0 | Auxiliary relay control |
| &M0 | * | 0 | Communication mode option |
| &Pn | * | 0 | Dial pulse ratio |
| &Q0 | * | 0 | Communication mode option |
| &Sn | * | 0 | DSR option |
| &Tn | | 0 | Self test commands |
| &Vn | | 0 | View active and stored configuration |
| &Un | * | 0 | Disable Trellis coding |
| &Wn | | 0 | Stored active profile |
| &Yn | * | 0 | Select stored profile on power up |
| &Zn=x | | none | Store telephone number |
| %En | * | 1 | Auto-retrain control |
| %G0 | * | 0 | Rate Renegotiation |
| %Qn | | none | Line signal quality |
| -Cn | * | 1 | Generate data modem calling tone |
| +GMI? | | none | Identify modem manufacturer |
| +GMM? | | none | Identify product model |
| +GMR? | | none | Identify product revision |

* Value saved in NVRAM.
** Command not preceded by an 'AT'.

**Table 5-2. V.42 / V.42 bis MNP AT Commands**

| Command | | Default | Function |
|---|---|---|---|
| %An | * | 13 | Set auto-reliable fallback character |
| %Cn | * | 1 | MNP 5 data compression control |
| \An | * | 3 | MNP block size |
| \Bn | * | none | Transmit break |
| \Cn | * | 0 | Set auto-reliable buffer |
| \Gn | * | 0 | Set modem port flow control |
| \Jn | * | 0 | bps rate adjust control |
| \Kn | * | 5 | Set break control |
| \Nn | * | 3 | Set operating mode |
| \O | | none | Originate reliable link |
| \Qn | * | 3 | Set serial port flow control |
| \Tn | * | 0 | Set inactivity timer |
| \U | | none | Accept reliable link |
| \Vn | * | 3 | Modify result code form |
| \Xn | * | 0 | Set XON/XOFF pass-through |
| \Y | | none | Switch to reliable mode |
| \Z | | none | Switch to normal mode |
| -Jn | * | 1 | Set V.42 detect phase |
| "Hn | * | 3 | V.42 bis compression control |
| "On | | 32 | V.42 bis string length |

* Value saved in NVRAM.

### Table 5-3. Fax Class 1 Identity AT Commands

| Command | Default | Function |
|---|---|---|
| +FMFR? | none | Identify modem manufacturer |
| +FMDL? | none | Identify product model |
| +FMI? | none | Identify modem manufacturer |
| +FMM? | none | Identify product number |
| +FMR? | none | Identify product revision |
| +FREV? | none | Identify product revision |

### Table 5-4. Fax Class 1 AT Commands

| Command | | Function |
|---|---|---|
| +FCLASS=1 | | Mode selection |
| +FCLASS? | | Mode query |
| +FCLASS=? | | Supported modes |
| +FRH=<mod> | | Receive HDLC data |
| +FRM=<mod> | | Receive data |
| +FRS=<time> | | Wait for silence |
| +FTH=<mod> | | Transmit HDLC data |
| +FTM=<mod> | | Transmit data |
| +FTS=<time> | | Stop transmission and pause |
| +FTTn | none | Fax transmit test command |
| +FRTn | none | Fax receive test command |

### Table 5-5. Fax Class 2 Action Commands

| Command | Default | Function |
|---|---|---|
| A | | Answer a call |
| D | | Originate a call |
| +FDR | | Begin or continue Phase C data reception |
| +FDT | | Begin or resume fax data transmission |
| +FET=ppm [pc, bc, fc] | 0 | Transmission page punctuation |
| +FK | | Kill operation |

### Table 5-6. Fax Class 2 Session Parameters

| Command | Default | Function |
|---|---|---|
| +FCLASS=2 | 0 | Service class identification and selection |
| +FAA=n | 0 | Fax/data automoding |
| +FAXERR=? | none | Session error report, read only |
| +FBADLN=0 | 0 | Bad line threshold |
| +FBADMUL=0 | 0 | Error threshold multiplier |
| +FBOR=n | 0 | Phase C data bit order |
| +FCIG=<string> | 0 | Local polling ID string |
| +FCQ=0 | 0 | Copy quality checking* |
| +FCR=n | 1 | Capability to receive |
| +FCTCRTY=0 | 0 | ECM retry count |
| +FDCC=n | none | DCE capabilities parameters |
| +FDCS? | 0000 0000 | Current session results |
| +FDFFC=0 | 0 | Data compression format |
| +FDIS:<string> | none | Current session negotiation parameters |
| +FECM=0 | 0 | Error correction mode control |
| +FLID=n | 0 | Local ID string |
| +FLNFC=0 | 0 | Page length format conversion |
| +FLPL=n | 0 | Indicates document available for polling |
| +FMDL? | none | Requests model ID |
| +FMFR? | none | Requests manufacturer ID |
| +FPHCTO=n | 30 | DTE phase C response time-out t |
| +FPTS=n | 0 | Page transfer status |
| +FREL=0 | 0 | Phase C received EOL alignment* |
| +FREV? | none | Request product revision ID |
| +FSPL=n | 0 | Enable polling* |
| +FVRFC=0 | 0 | Vertical resolution format conversion |
| +FWDFC=0 | 0 | Page width format conversion |

*Noted parameters, commands, and responses depend on the capability to receive.

### Table 5-7. Fax Class 2 Response Codes

| Command | Function |
|---|---|
| +FCFR | Indicates confirmation to receive |
| +FCIG=<CIG ID string> | Reports polling station ID and CIG |
| +FCIS:<CIS ID string> | Report called station ID and CSI |
| +FCON | Indicates connection with fax modem or machine status |
| +FDCS=<string> | Reads current session DCS information |
| +FDIS=<string> | Reports DIS information for remote identification |
| +FDTC:<string> | Reports the DTC frame information |
| +FET:ppm | Post-page message report |
| +FHNG:<hangup cause code> | Call termination with status |
| +FNSC:<NSC FIFstring> | Reports nonstandard commands |
| +FNFS:<NFS FIF string> | Report nonstandard facilities |
| +FNSS:<NSS FIF string> | Report nonstandard setup |
| +FPOLL | Indicates polling request |
| +FPTS:ppr | Transfer page transfer status* |
| +FPTS:ppr, lc [blc, cblc, lbc] | Receive page transfer status* |
| +FTSI:<TSI ID string> | Reports transmit status ID and TSI |
| +FVOICE | Indicates transition to voice |

*Noted parameters, commands, and responses depend on the capability to receive.

### Table 5-8. Voice AT Commands

| Command | Default | Function |
|---|---|---|
| #VCL=1 | 0 | Voice mode selection |
| #VBP | none | Generate beep tone |
| #VCID=n* | 0 | Caller ID selection |
| #VCSD=n | 0 | Command mode silence detection |
| #VDDS=n | 0 | DMA <DKE> shielding |
| #VDR=n,m | 0, 0 | Distinctive Ring selection |
| #VFR=n | 0 | Playback/record fixed UART port rate |
| #VIN | none | Read general-purpose input pins |
| #VIP=n | 0 | Initialize parameter |
| #VLN=n | 0 | Relay/speaker control |
| #VOUT=n | 0 | Write to output pins |
| #VPH | none | Telephone-Emulation mode |
| #VDPY | none | DMA play mode |
| #VPL=n | 127 | Play level |
| #VPY | none | Play mode |
| #VDRD | none | DMA record mode |
| #VRD | none | Record mode |
| #VRL=n | 127 | Recording level |
| #VSL=n | 127 | Record silence threshold level |
| #VSM=n | CL1 | Sampling mode |
| #VSPH=n | 0 | Analog speakerphone feature control |
| #VSQT=n | 60 | Record 'q' silence time |
| #VSR=n | 9600 | Sampling rate |
| #VSST=n | 60 | Record 's' silence time |

* Value saved in NVRAM.

### Table 5-9. Voice <DLE> Character Pairs (DTE→DCE)

| Command | Hex Code | Function |
|---|---|---|
| <ETX> | 03 | End of playback mode data (normal termination) |
| <DLE> | 10 | Single <DLE> character in the data stream |
| A | 41 | Immediate termination of playback mode |
| CTRL-Z | 1A | Terminate record mode and empty internal modem voice buffer (immediate termination) |
| u | 75 | Bump up playback volume |
| d | 64 | Bump down playback volume |
| <FS> | 1C | Finish current message, then start new message |

### Table 5-10. Voice <DLE> Character Pairs (DTE←DCE)

| Command | Hex Code | Function |
|---|---|---|
| <ETX> | 03 | End of record mode data |
| <DLE> | 10 | Single <DLE> character in the data stream |
| 0–9 | 30–39 | DTMF 0–9 |
| A–D | | 41–44DTMF A–D |
| E | 43 | DTMF * |
| F | 44 | DTMF # |
| N | 4E | 1100 Hz Fax CNG Tone |
| g | 67 | 1300 Hz data calling tone |
| R | 52 | Incoming ring |
| b | 62 | Busy tone detected |
| d | 64 | Dial tone detected |
| e | 65 | Energy detected |
| q | 71 | Presumed hangup |
| s | 73 | Presumed end of message |
| h | 68 | Local phone goes on-hook |
| H | 48 | Local phone goes off-hook |
| I | 6C | Remote hangup |
| L | 4C | Remote hangup |
| p | 70 | Extension phone goes on-hook |
| P | 50 | Extension phone goes off-hook |
| Z z { | 5A, 7A, | Manufacturer-specific |
| } ( ) | 7B, 7D, 28, | |
| % & | 29, 25, 26 | |

### Table 5-11. VoiceView™ Commands

| Command | Function |
|---|---|
| +FCLASS=80 | Mode selection |
| +FLO | Flow control select |
| +FPR | Serial port rate control |
| -SVV | Start VoiceView data mode |
| -SAC | Accept data mode request |
| -SIP | Initialize VoiceView parameters |
| -SCD | Capabilities data |
| -SER? | Error status (read only) |
| -SIC | Reset capabilities to default setting |
| -SSQ | Start capabilities query |
| -SDA | Start modem data mode |
| -SFX | Start fax data mode |
| -SQR | Capabilities query response control |
| -SSP | VoiceView transmission speed |
| -SSR | Start sequence response control |

### Table 5-12. VoiceView™ Response Codes

| Command | Function |
|---|---|
| -SFA | Fax data mode start sequence event (mandatory only if fax data mode is supported) |
| -SMD | Modem data mode start sequence event (mandatory only if modem data mode is supported) |
| -SSV | VoiceView data mode start sequence event |
| -SRQ | Receive capabilities query event |
| -SRC: | Receive capabilities information event |
| -STO | Talk-off event |

### Table 5-13. VoiceView™ <DLE> Character Pairs

| Command | Function |
|---|---|
| <DLE><CAN> | Abort data transfer in progress |
| <DLE><EOT> | End of message marker, final message of transaction, no response accepted (ASCII 10h 04h) |
| <DLE><ESC> | End of message marker, DCE shall immediately return to voice mode (ASCII 10h 1Bh) |
| <DLE><ETB> | End of message marker, final response requested, after which the transaction will terminate (ASCII 10h 17h) |
| <DLE><ETX> | End of message marker, continue transaction, response requested (ASCII 10h 03h) |
| <XOFF> | Indicates not ready to receive data |
| <XON> | Indicates ready to receive data |

### Table 5-14. Dial Modifiers

| Command | Function |
|---|---|
| 0 to 9 | Dialing digits |
| A,B,C, D, *, # | Tone dial characters |
| P | Pulse dial |
| R | Reverse originate mode |
| S=n | Dial NVRAM telephone number |
| T | Tone dial |
| W | Wait for dial tone |
| , | Pause |
| ! | Flash hook |
| @ | Wait for quiet answer |
| ; | Return to idle state |
| - ( ) | Ignored by modem |

### Table 5-15. S-Registers Summary

| Register | | Default | Function |
|---|---|---|---|
| S0 | * | 0 | No. of rings to auto-answer on |
| S1 | | 0 | Ring count |
| S2 | * | 43 | Escape character |
| S3 | | 13 | Carriage return character |
| S4 | | 10 | Line feed character |
| S5 | | 8 | Backspace character |
| S6 | * | 2 | Wait before dialing |
| S7 | * | 60 | Wait for carrier |
| S8 | * | 2 | Pause time for dial modifier |
| S9 | * | 6 | Carrier recovery time |
| S10 | * | 14 | Lost carrier hang up delay |
| S11 | * | 70 | DTMF dialing speed |
| S12 | * | 50 | Guard Time |
| S13 | | none | Reserved |
| S14 | * | none | Bit-mapped options |
| S15 | | none | Reserved |
| S16 | * | none | Modem test options |
| S17 | | none | Reserved |
| S18 | * | 0 | Modem test timer |
| S19 | | none | Reserved |
| S20 | | none | Reserved |
| S21 | * | none | Bit-mapped options |
| S22 | * | none | Bit-mapped options |
| S23 | * | none | Bit-mapped options |
| S24 | | none | Reserved |
| S25 | * | 5 | Detect DTR change |
| S27 | * | none | Bit-mapped options |
| S30 | * | 10 | Sleep mode timer |
| S31 | | none | Bit-mapped options |
| S37 | * | 0 | Maximum line speed attempted |
| S86 | | none | Call failure code |
| S90 | * | 0 | Disconnect Inactivity timer |
| S91 | * | 10 | PSTN Transmit level |
| S108 | * | 1 | Retrain signal quality selector |
| S109 | * | 62 | Line speeds permitted |

* Value saved in NVRAM.

### Table 5-16. Basic Response Codes (\V0)

| Numeric Code | Verbose Code |
|---|---|
| 0 | OK |
| 1 | CONNECT |
| 2 | RING |
| 3 | NO CARRIER |
| 4 | ERROR |
| 5 | CONNECT 1200 |
| 6 | NO DIAL TONE |
| 7 | BUSY |
| 8 | NO ANSWER |
| 9 | BLACKLISTED |
| 10 | CONNECT 2400 |
| 11 | CONNECT 4800 |
| 12 | CONNECT 7200 |
| 14 | CONNECT 9600 |
| 16 | CONNECT 12000 |
| 17 | CONNECT 14400 |
| +F4 | +FCERROR |

### Table 5-17. Modified Response Codes (\V1)

| Numeric Code | Verbose Code |
|---|---|
| 22 | CONNECT 300/REL |
| 24 | CONNECT 1200/REL |
| 25 | CONNECT 2400/REL |
| 26 | CONNECT 4800/REL |
| 27 | CONNECT 7200/REL |
| 28 | CONNECT 9600/REL |
| 29 | CONNECT 12000/REL |
| 30 | CONNECT 14400/REL |

### Table 5-18. V.42 Extended Response Codes (\V2)

| Numeric Code | Verbose Code |
|---|---|
| 32 | CONNECT 300/REL-MNP |
| 34 | CONNECT 1200/REL-MNP |
| 35 | CONNECT 2400/REL-MNP |
| 36 | CONNECT 4800/REL-MNP |
| 37 | CONNECT 7200/REL-MNP |
| 38 | CONNECT 9600/REL-MNP |
| 39 | CONNECT 12000/REL-MNP |
| 40 | CONNECT 14400/REL-MNP |
| 42 | CONNECT 300/REL-MNP5 |
| 44 | CONNECT 1200/REL-MNP5 |
| 45 | CONNECT 2400/REL-MNP5 |
| 46 | CONNECT 4800/REL-MNP5 |
| 47 | CONNECT 7200/REL-MNP5 |
| 48 | CONNECT 9600/REL-MNP5 |
| 49 | CONNECT 12000/REL-MNP5 |
| 50 | CONNECT 14400/REL-MNP5 |
| 54 | CONNECT 1200/REL-LAPM |
| 55 | CONNECT 2400/REL-LAPM |
| 56 | CONNECT 4800/REL-LAPM |
| 57 | CONNECT 7200/REL-LAPM |
| 58 | CONNECT 9600/REL-LAPM |
| 59 | CONNECT 12000/REL-LAPM |
| 60 | CONNECT 14400/REL-LAPM |
| 64 | CONNECT 1200/REL-LAPM V.42 BIS |
| 65 | CONNECT 2400/REL-LAPM V.42 BIS |
| 66 | CONNECT 4800/REL-LAPM V.42 BIS |
| 67 | CONNECT 7200/REL-LAPM V.42 BIS |
| 68 | CONNECT 9600/REL-LAPM V.42 BIS |
| 69 | CONNECT 12000/REL-LAPM V.42 BIS |
| 70 | CONNECT 14400/REL-LAPM V.42 BIS |

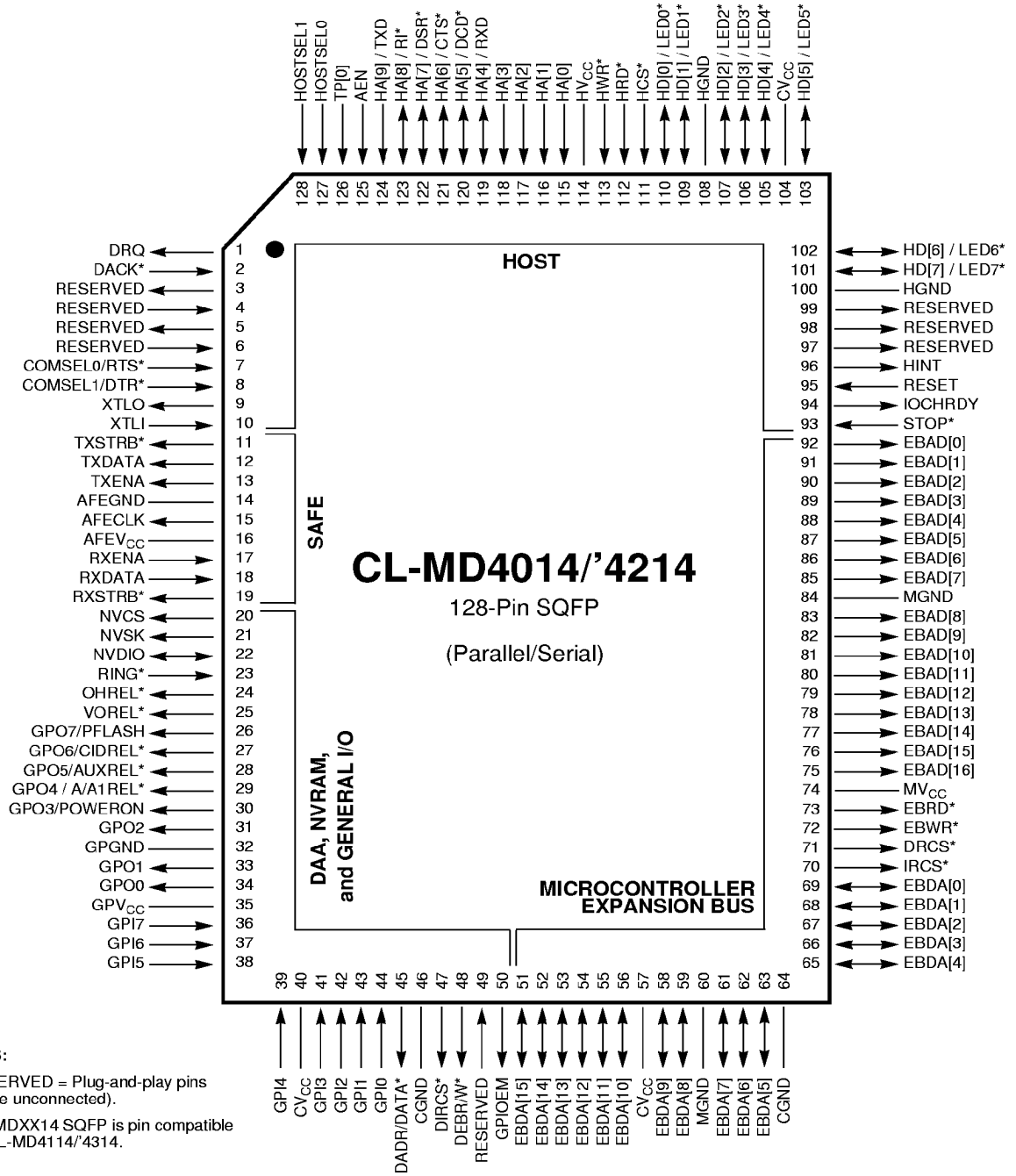
### Table 5-19. DTE-Modem Data Rate Response Codes (\V3)

| Numeric Code | Verbose Code |
|---|---|
| 0 | OK |
| 1 | CONNECT |
| 2 | RING |
| 3 | NO CARRIER |
| 4 | ERROR |
| 5 | CONNECT 1200 |
| 6 | NO DIAL TONE |
| 7 | BUSY |
| 8 | NO ANSWER |
| 10 | CONNECT 2400 |
| 11 | CONNECT 4800 |
| 12 | CONNECT 9600 |
| 13 | CONNECT 14400 |
| 14 | CONNECT 19200 |
| 18 | CONNECT 57600 |
| 24 | CONNECT 7200 |
| 25 | CONNECT 12000 |
| 26 | CONNECT1200/75 |
| 27 | CONNECT75/1200 |
| 28 | CONNECT 38400 |
| 31 | CONNECT 115200 |
| 33 | FAX |
| 35 | DATA |
| 40 | CARRIER 300 |
| 42 | CARRIER 75TX/1200RX |
| 43 | CARRIER 1200TX/75RX |
| 46 | CARRIER 1200 |
| 47 | CARRIER 2400 |
| 48 | CARRIER 4800 |
| 49 | CARRIER 7200 |
| 50 | CARRIER 9600 |
| 51 | CARRIER 12000 |
| 52 | CARRIER 14400 |
| 62 | BLACKLISTED |
| 63 | DELAYED |
| 64 | PROHIBITED |
| 66 | COMPRESSION: MNP5 |
| 67 | COMPRESSION: V.42 BIS |
| 69 | COMPRESSION: NONE |
| 70 | PROTOCOL: NONE |
| 77 | PROTOCOL: LAPM |
| 80 | PROTOCOL: MNP |
| 81 | PROTOCOL: MNP2 |
| 82 | PROTOCOL: MNP3 |
| 83 | PROTOCOL: MNP2, 4 |
| 84 | PROTOCOL: MNP3, 4 |
| 85 | PROTOCOL: MNP2 |
| 86 | PROTOCOL: MNP3 |
| 87 | PROTOCOL: MNP2,4 |
| 88 | PROTOCOL: MNP3, 4 |
| +F4 | +FCERROR |

# 6. HARDWARE SIGNALS

## 6.1 DSμP Pin Diagram

### 6.1.1 Parallel/Serial (128-pin SQFP) Package

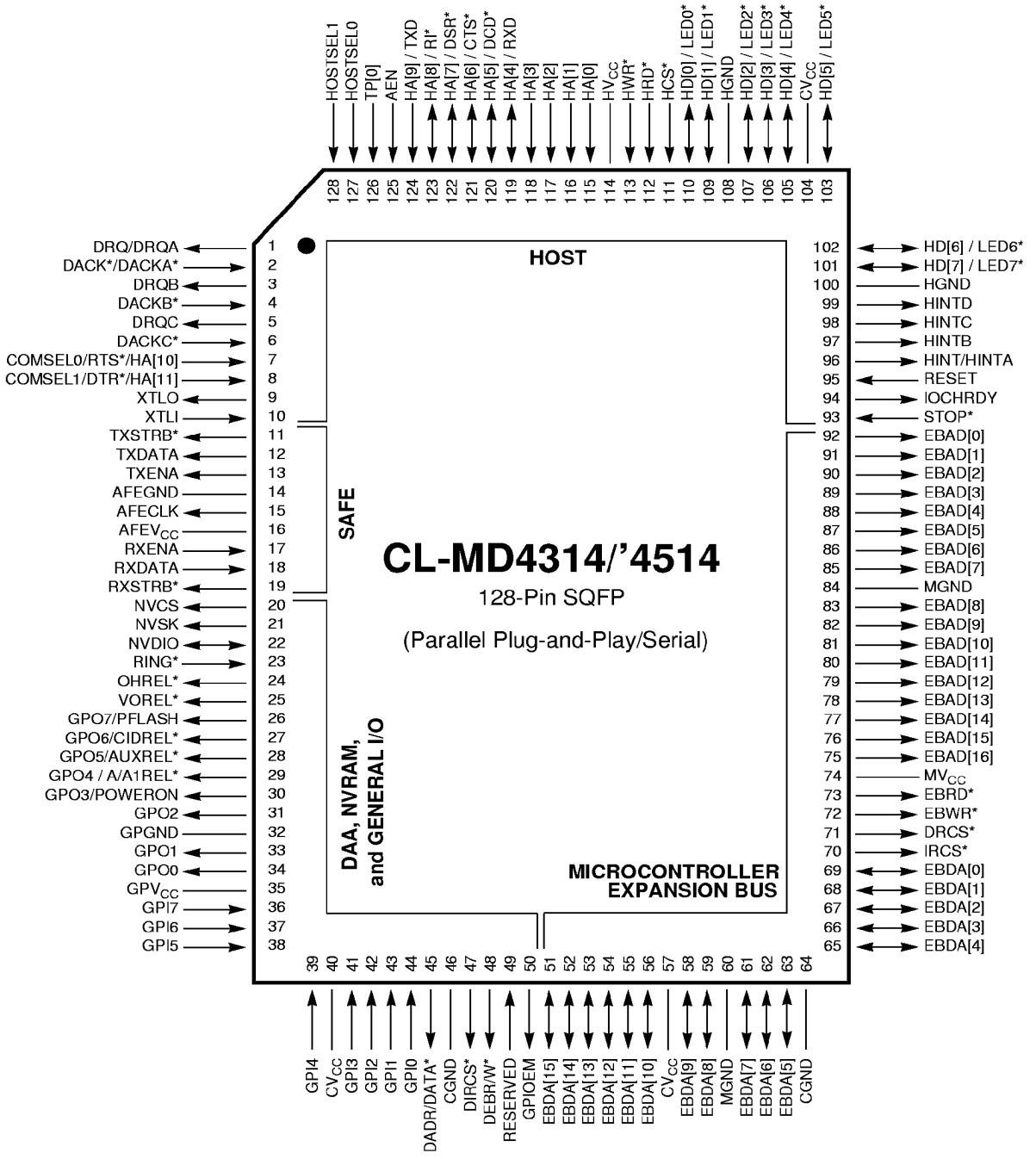



**NOTES:**

1) RESERVED = Plug-and-play pins (leave unconnected).

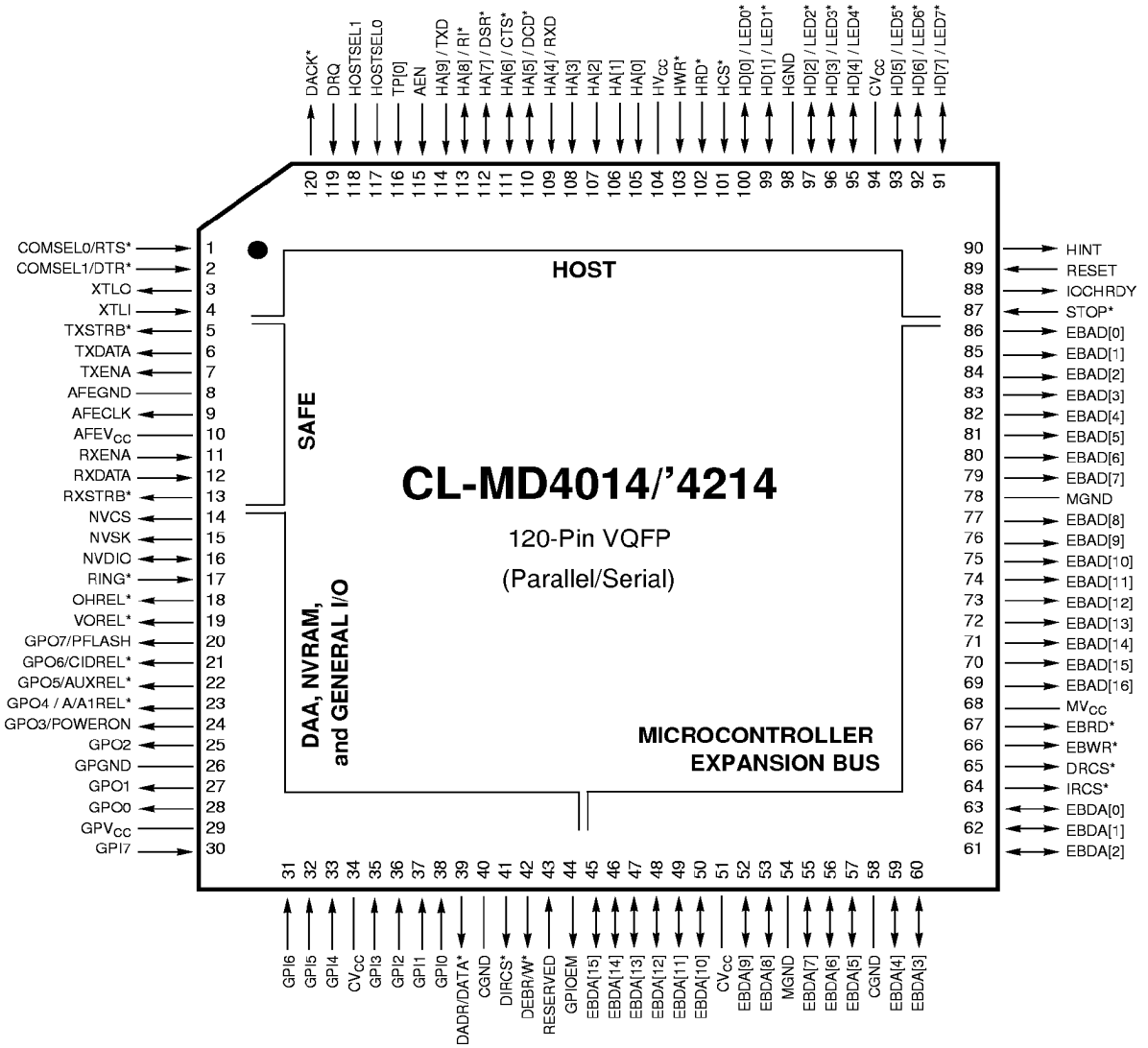
2) CL-MDXX14 SQFP is pin compatible to CL-MD4114/'4314.

### 6.1.2 Parallel Plug-and-Play/Serial (128-pin SQFP) Package

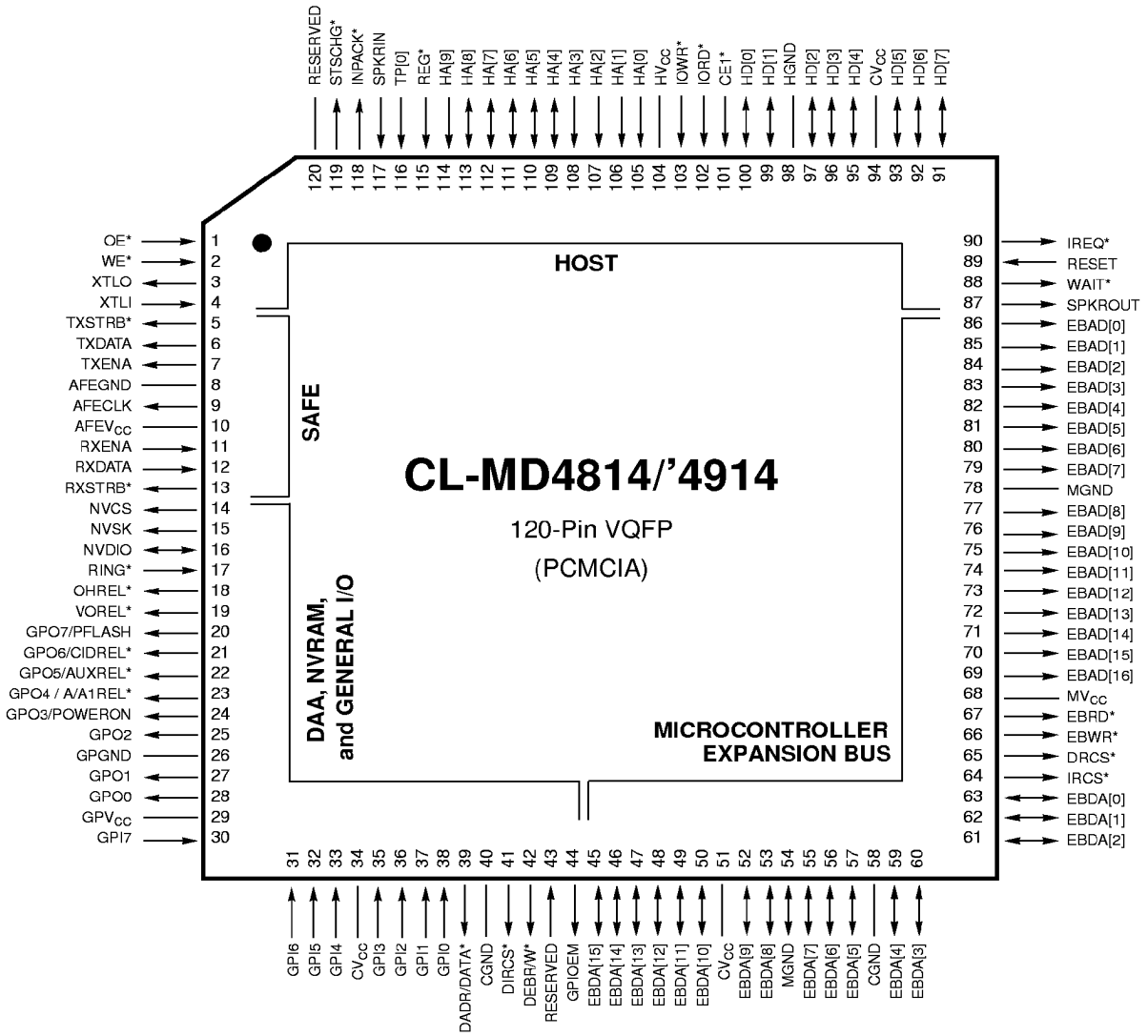



**NOTE:** The CL-MDXX14 SQFP is pin compatible to the CL-MD4114/'4314.

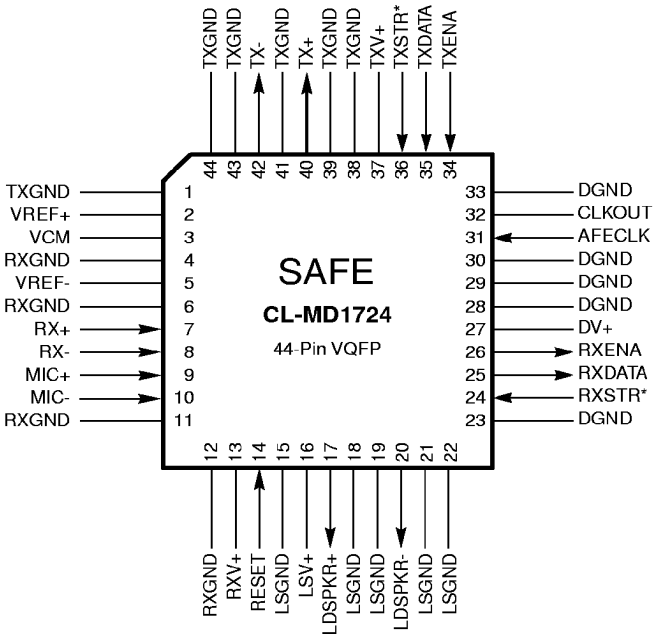
### 6.1.3 Parallel/Serial (120-pin VQFP) Package



## 6.2 PC Card Pin Diagram — 120-pin VQFP Package



## 6.3 SAFE Pin Diagram — 44-pin VQFP Package



## 6.4 DSμP Pin Descriptions (CL-MDXX14)

This section describes the DSμP hardware pins. The following conventions are used in the pin assignment tables: (*) denotes an active-low signal; all other pin are active-high; I = input; I/O = input/output; O = output; OD = open-drain output; OT = open collector output when function enabled and tristated when function disabled; GND = ground; AGND = analog ground; and PWR = power supply.

To support future mixed-voltage requirements, each pin is grouped into a family. Each family consists of pins that interface with the same device, and are driven by the corresponding $V_{CC}$ and ground pins. In future products, the modem DSμP processor core may be able to use 3.3 V and the host interface may be able to use 5 V. The current universal device set runs only at 5 V but is expected to allow mixed voltage sources in the future.

### 6.4.1 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions (CL-MDXX14)

The function of these pins depends on the signal levels at HOSTSEL[0–1]. The pin requirements for each interface are provided in Table 6-1 below, and the pin descriptions are given in the following sections.

**Table 6-1. Pin Requirements for a Given Host Interface**

| Host Interface | DSμP Pins | | | | |
|---|---|---|---|---|---|
| | HOSTSEL1 | HOSTSEL0 | HCS* | COMSEL[0–1] | AEN, HA[0–9] |
| Serial without LEDs | 0 | 0 | 1 | (DTR*/RTS*) | No connects |
| Serial with LEDs | 0 | 0 | 0 | (DTR*/RTS*) | HA[0–2] = '001' See Note 1 |
| Parallel with plug-and-play (internal address decode) [See Notes 2, 3, and 4] | 0 | 1 | 1 | HA[10–11] See Note 5 | AEN, HA[0–9] |
| Parallel with external address decode | 1 | 0 | HCS* | See Note 6 | HA[0–2] See Note 7 |
| Parallel with internal address decode | 1 | 1 | 1 | COMSEL[0–1] | AEN, HA[0–9] |

**NOTES:**

1) Connect HA[0–1] to ground and HA[2] to $V_{CC}$.
2) Only the 128-pin SQFP DSμP package will support plug-and-play mode.
3) For plug-and-play designs, HOSTSEL0 is connected to $V_{CC}$, and HOSTSEL1 is used to indicate whether the board is in plug-and-play or non-plug-and-play mode.
4) For plug-and-play designs, there are three DMA channels (A–C) and four host interrupt pins supported (DACK*, DRQA, DACKB*, DRQB, DACKC*, DRQC, HINTA, HINTB, HINTC, and HINTD).
5) For plug-and-play designs, connect ISA bus signals HA[10] to COMSEL0 and HA[11] to COMSEL1.
6) Connect COMSEL[0–1] to either $V_{CC}$ or ground. Do not leave unconnected.
7) Connect HA[0–2] to the PC bus, and connect AEN and HA[3–9] pins to $V_{CC}$ or ground. Do not leave unconnected.

### 6.4.1 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions (CL-MDXX14) *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| HOSTSEL1<br>HOSTSEL0 | 128<br>127 | 118<br>117 | I | **PARALLEL/SERIAL HOST INTERFACE SELECTION**: The two HOSTSEL inputs pins are used to select the host interface type. These include serial, parallel with external address decode, parallel with internal address decode, and parallel plug-and-play with internal address decode.<br><br>Device sets that support plug-and-play are pin compatible with device sets that do not support plug-and-play (SQFP package only). Thus OEMs can design one modem ISA bus board that will support both plug-and-play and current non-plug-and-play applications. |
| $HV_{CC}$ | 114 | 104 | PWR | **HOST INTERFACE +5-V POWER SUPPLY**: The current DSμP requires only +5 V to perform all the digital processing. |
| HGND | 100<br>108 | 98 | GND | **HOST INTERFACE DIGITAL GROUND**. |
| STOP* | 93 | 87 | I | **STOP MODE**: A high input signal powers up the device set. A low input signal places the modem in stop mode that effectively turns off all device-set power usage except some internal control logic. When stop mode is not needed, this input pin should be pulled up to $V_{CC}$. |
| XTLI<br>XTLO | 10<br>9 | 4<br>3 | I<br>O | **DSμP CRYSTAL INPUT AND OUTPUT**: These two pins provide a feed-back circuit for generating the device set system clock. |
| RESET | 95 | 89 | I | **DSμP RESET**: This pin is used to generate a modem reset. A modem reset is accomplished by pulsing the signal at the RESET pin from a low to high to low. The RESET input pin must be high for at least 10 μs. The modem requires 200 ms, after the high-to-low transition, to initialize all modem functions before receiving any AT commands. |
| AEN | 125 | 115 | I | **PARALLEL ADDRESS ENABLE/SERIAL EXTERNAL TRANSMIT CLOCK**: In parallel mode, this pin is used for host address enable. This clock must exhibit the same characteristics as TXC. |

### 6.4.1 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions (CL-MDXX14) *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| COMSEL0/ RTS*/HA[10] | 7 | 1 | I | **PARALLEL COM PORT SELECTION LINE 0 / SERIAL REQUEST TO SEND / HOST ADDRESS LINE 10**: The function of this pin is controlled by HOSTSEL0 and HOSTSEL1 input pins. In parallel mode with both HOSTSEL0 and HOSTSEL1 high, the states of COMSEL0 and COMSEL1 are used to select a COM port.<br><br>*HA[9:0]* — *COM Port* — *COMSEL1* — *COMSEL0*<br>3F8–3FF — 1 — 0 — 0<br>2F8–2FF — 2 — 0 — 1<br>3E8–3EF — 3 — 1 — 0<br>2E8–2EF — 4 — 1 — 1<br><br>In parallel plug-and-play mode, this pin is used for host address line 10.<br><br>In serial mode, when low, this signal informs the modem that the DTE is ready to send data on TXD. |
| COMSEL1/ DTR*/HA[11] | 8 | 2 | I | **PARALLEL COM PORT SELECTION LINE 1 / SERIAL DATA TERMINAL READY / HOST ADDRESS LINE 11**: The function of this pin is controlled by HOSTSEL0 and HOSTSEL1 input pins. In parallel mode, the states of COMSEL0 and COMSEL1 are used to select a COM port. In parallel plug-and-play mode, this pin is used for host address line 11. In serial mode, when low, this signal informs the modem that the DTE is ready to establish a communication link. |
| HCS* | 111 | 101 | I | **HOST CHIP SELECT (UART)**: When HOSTSEL0 is high and HOSTSEL1 is low, a low input signal at this pin allows the host computer to read or write to the UART interface registers. HCS* is used to select alternate options, as defined in Table 6-1 on page 27. |
| HINT/HINTA | 96 | 90 | OT | **HOST INTERRUPT/HOST INTERRUPT A**: When enabled, this signal goes high whenever certain bits change within the UART registers. There are four possible interrupt sources that may be enabled or disabled using the UART IER register: receiver data available, transmitter holding register empty, receiver line status, and modem line status. The UART interface automatically drops the HINT signal level whenever the host performs the appropriate action for the interrupt source.<br><br>When disabled, this output is tristated. In parallel plug-and-play mode, this pin can be selected from up to four interrupt output pins (A–D) as the ISA bus HINT signal (that is, only one HINT output can be used at a time). This output can sink up to 20 mA. |

### 6.4.1 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions (CL-MDXX14) *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| HINTB<br>HINTC<br>HINTD | 97<br>98<br>99 | | OT | **HOST INTERRUPTS (B–D)**: In parallel plug-and-play mode, four interrupt outputs are provided (A–D). Any one of these pins can be selected as the ISA bus HINT signal, but only one output is selected at a time. This allows a board to be designed, which allows the end user to select the COM port IRQ from a list of 4 different IRQs (for example, IRQ3, IRQ4, IRQ5, and IRQ12). These pins are tristated in non-plug-and-play modes or when not selected.<br><br>When enabled, this signal goes high whenever certain bits change within the UART registers. There are four possible interrupt sources that may be enabled or disabled using the UART IER register: receiver data available, transmitter holding register empty, receiver line status, and modem line status. The UART interface automatically drops the HINT signal level whenever the host performs the appropriate action for the interrupt source. When disabled, this output is tristated. This output can sink up to 20 mA. |
| HRD* | 112 | 102 | I | **HOST READ**: When HRD* and HCS* are low, the host can read the data, control, and status information from the selected UART registers. In the serial mode, connect HRD* to ground when the DSμP LED drivers [for example, SQFP package pins 101, 102, 103, 105, 106, 107, 109, and 110] are used; otherwise, connect HRD* to $V_{CC}$. |
| HWR* | 113 | 103 | I | **HOST WRITE**: When HWR* and HCS* are low, the host can write control information or data to the selected UART registers. In the serial mode, connect HWR* to $V_{CC}$. |
| IOCHRDY | 94 | 88 | OD | **IOCHRDY**: This pin provides a wait-stated output for data, control, and status information reads and writes to the modem UART. This output can sink up to 20 mA. |
| HA[0–2] | 115<br>116<br>117 | 105<br>106<br>107 | I | **HOST ADDRESS LINES [0–2]**: These three address lines are used to select the UART interface registers. In the serial mode connect HA[0] to $V_{CC}$ and connect HA[2:1] to ground. |
| HA[3] | 118 | 108 | I | **HOST ADDRESS LINE 3**: When HOSTSEL0 is high, this pin is used as host address line 3. In serial mode, connect HA[3] to ground. |
| HA[4]/RXD | 119 | 109 | I/O | **PARALLEL ADDRESS LINE 4/SERIAL RECEIVE DATA**: In parallel mode with HOSTSEL0 high, this pin is used for host address line 4. In serial mode, this is the serial data output to the DTE. |

### 6.4.1 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions (CL-MDXX14) *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| HA[5]/DCD* | 120 | 110 | I/O | **PARALLEL ADDRESS LINE 5 / SERIAL DATA CARRIER DETECT**: In parallel mode with HOSTSEL0 high, this pin is used for host address line 5. In serial mode when low, this signal informs the DTE that the modem has detected the remote modem data carrier. |
| HA[6]/CTS* | 121 | 111 | I/O | **PARALLEL ADDRESS LINE 6 / SERIAL CLEAR TO SEND**: In parallel mode with HOSTSEL0 high, this pin is used for host address line 6. In serial mode when low, this signal informs the DTE that the modem is ready to receive data on TXD. |
| HA[7]/DSR* | 122 | 112 | I/O | **PARALLEL ADDRESS LINE 7 / SERIAL DATA SET READY**: In parallel mode with HOSTSEL0 high, this pin is used for host address line 7. In serial mode when low, this signal informs the DTE that the modem is ready to establish a communication link. |
| HA[8]/RI* | 123 | 113 | I/O | **PARALLEL ADDRESS LINE 8 / SERIAL RING INDICATOR**: In parallel mode with HOSTSEL0 high, this pin is used for host address line 8. In serial mode, when low, this signal informs the DTE that the modem has received a valid ring signal. |
| HA[9]/TXD | 124 | 114 | I | **PARALLEL ADDRESS LINE 9 / SERIAL TRANSMIT DATA**: In parallel mode with HOSTSEL0 high, this pin is used for the host address line 9. In serial mode, this signal is the serial data input from the DTE. |
| HD[0]/LED0* | 110 | 100 | I/O | **PARALLEL DATA BUS LINE 0 / SERIAL LED DRIVER 0**: In parallel mode, this pin is used for the host data bus line 0. In serial mode with HCS* low and the appropriate microcontroller firmware, this pin can be used as an LED driver. |
| HD[1]/LED1* | 109 | 99 | I/O | **PARALLEL DATA BUS LINE 1 / SERIAL LED DRIVER 1**: In parallel mode, this pin is used for the host data bus line 1. In serial mode with HCS* low and the appropriate microcontroller firmware, this pin can be used as an LED driver. |
| HD[2]/LED2* | 107 | 97 | I/O | **PARALLEL DATA BUS LINE 2 / SERIAL LED DRIVER 2**: In parallel mode, this pin is used for the host data bus line 2. In serial mode with HCS* low and the appropriate microcontroller firmware, this pin can be used as an LED driver. |
| HD[3]/LED3* | 106 | 96 | I/O | **PARALLEL DATA BUS LINE 3 / SERIAL LED DRIVER 3**: In parallel mode, this pin is used for the host data bus line 3. In serial mode with HCS* low and the appropriate microcontroller firmware, this pin can be used as an LED driver. |

### 6.4.1 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions (CL-MDXX14) *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| HD[4]/LED4* | 105 | 95 | I/O | **PARALLEL DATA BUS LINE 4 / SERIAL LED DRIVER 4**: In parallel mode, this pin is used for the host data bus line 4. In serial mode with HCS* low and the appropriate microcontroller firmware, this pin can be used as an LED driver. |
| HD[5]/LED5* | 103 | 93 | I/O | **PARALLEL DATA BUS LINE 5 / SERIAL LED DRIVER 5**: In parallel mode, this pin is used for the host data bus line 5. In serial mode with HCS* low and the appropriate microcontroller firmware, this pin can be used as an LED driver. |
| HD[6]/LED6* | 102 | 92 | I/O | **PARALLEL DATA BUS LINE 6 / SERIAL LED DRIVER 6**: In parallel mode, this pin is used for the host data bus line 6. In serial mode with HCS* low and the appropriate microcontroller firmware, this pin can be used as an LED driver. |
| HD[7]/LED7* | 101 | 91 | I/O | **PARALLEL DATA BUS LINE 7 / SERIAL LED DRIVER 7**: In parallel mode, this pin is used for the host data bus line 7. In-serial mode with HCS* low and the appropriate microcontroller firmware, this pin can be used as an LED driver. |
| DACK*/DACKA* | 2 | 120 | I | **PARALLEL DMA ACKNOWLEDGE / SERIAL RECEIVE CLOCK**: In parallel mode, this pin is the 16C550A DMA DACK* signal. In parallel plug-and-play mode, the DACKA* pin is the 16C550A DMA Acknowledge (DACK*) signal and works with the corresponding DRQA to support a given DMA channel. These DMA signals can be connected to any 8-bit DMA channel. This product supports three plug-and-play DMA channels (A–C). |
| DACKB*<br>DACKC* | 4, 6 | | I | **PARALLEL PLUG-AND-PLAY DMA ACKNOWLEDGE (B AND C)**: In parallel plug-and-play mode, the DACKB* and DACKC* pins are 16C550A DMA Acknowledge (DACK*) signals and work with the corresponding DRQB and DRQC, respectively, to support a given DMA channel. These DMA signals can be connected to any 8-bit DMA channel. This product supports three plug-and-play DMA channels (A–C). |
| DRQ/DRQA | 1 | 119 | O | **PARALLEL DMA REQUEST / SERIAL TRANSMIT CLOCK**: In parallel mode, this is the 16C550A DMA Request (DRQ). In parallel plug-and-play mode, the DRQA pin is the 16C550A DMA DRQ signal and works with the corresponding DACKA* to support a given DMA channel. These DMA signals can be connected to any 8-bit DMA channel. This product supports a total of three plug-and-play DMA channels (A–C). |

### 6.4.1 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions (CL-MDXX14) *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| DRQB/DRQC | 3, 5 | | O | **PARALLEL PLUG-AND-PLAY DMA REQUEST (B AND C)**: In parallel plug-and-play mode, the DRQB and DRQC pins are 16C550A DMA Acknowledge (DRQ) signals and work with the corresponding DACKB* and DACKC*, respectively, to support a given DMA channel. These DMA signals can be connected to any 8-bit DMA channel. This product supports three plug-and-play DMA channels (A–C). |
| TP[0] | 126 | 116 | I | **MANUFACTURING TEST PIN**: This pin is used during Cirrus Logic manufacturing testing. This pin should be pulled up to $V_{CC}$ for all applications. |

### 6.4.2 DSμP PC Card (PCMCIA) Host Interface Pin Descriptions (CL-MD4814/'4914)

| Symbol | VQFP | Type | Description |
|---|---|---|---|
| HVcc | 104 | PWR | **HOST INTERFACE +5 V POWER SUPPLY**: The DSμP requires only +5 V to perform all the digital processing. |
| HGND | 98 | GND | **HOST INTERFACE DIGITAL GROUND**. |
| RESET | 89 | I | **DSμP RESET**: This pin is used to generate a modem reset. A modem reset is accomplished by pulsing the signal at the RESET pin from a low to high to low. The RESET input pin must be high for at least 10 μs. The modem requires 200 ms, after the high-to-low transition, to initialize all modem functions before CE1 or CE2 be can asserted. After a reset, the host computer needs to configure the PC card interface, since the modem card will be in an unconfigured state following a reset. An internal resistor-capacitor circuit causes the modem to be reset during a hot insertion (that is, when the computer power is on during installation of the PC card). |
| RESERVED | 120 | – | **RESERVED**: This pin is reserved for future enhancements to the device set and should be connected to ground. |
| CE1* | 101 | I | **CARD ENABLE EVEN ADDRESS**: When CE1* and REG* are low, a low input signal at IORD*, IOWR*, OE*, or WE* allows the host to read or write to the modem UART and configuration registers, or read the PC card CIS. |
| HA[0–9] | 105–114 | I | **HOST ADDRESS LINES [0–9]**: These ten address lines are used to select the modem UART, and PC card CIS and configuration registers. |

### 6.4.2 DSμP PC Card (PCMCIA) Host Interface Pin Descriptions (CL-MD4814/'4914) *(cont.)*

| Symbol | VQFP | Type | Description |
|---|---|---|---|
| HD[0–7] | 100:99<br>97:95<br>93:91 | I/O | **HOST DATA BUS LINES [0–7]**: These eight data bus lines are used to read from or write to the modem UART and PC card CIS configuration registers, or read the PC card CIS. |
| INPACK* | 118 | O | **INPUT ACKNOWLEDGE**: This output signal will be asserted by the modem if the modem is selected and can respond to an I/O read cycle. This signal is inactive until configured within the modem PC card interface registers. |
| IOWR* | 103 | I | **HOST WRITE**: When IOWR*, REG*, and CE1* are low and the PC Card Configuration Option register (COR) CARD EN bit is set to '1', the host can write control information or data to the selected UART registers. |
| IORD* | 102 | I | **HOST READ**: When IORD*, REG*, and CE1* are low and the PC Card Configuration Option register (COR) CARD EN bit is set to '1', the host can read the data, control, and status information from the selected UART registers. |
| IREQ* | 90 | O | **HOST INTERRUPT**: When PC Card Configuration Option register (COR) CARD EN bit is set to '1', the interrupt structure is compatible with a 16C450/16C550 UART. When enabled by the appropriate UART bits, this signal goes low whenever certain bits change within the UART registers. There are four possible interrupt sources that may be enabled or disabled using the UART IER register: receiver data available, Transmitter Holding register empty, receiver line status, and modem line status. The UART interface automatically de-asserts the IREQ* signal level whenever the host performs the appropriate action for the interrupt source. When disabled (that is, CARD EN is set to '0'), this output pin is tristated. This output can sink up to 20 mA. |
| OE* | 1 | I | **OUTPUT ENABLE**: When OE*, REG*, and CE1* are low, the host can read data from the PC card CIS or card configuration registers. |
| REG* | 115 | I | **ATTRIBUTE MEMORY SELECT**: When REG* and CE1* are low, a low input signal at IORD*, IOWR*, OE*, or WE* allows the host to read or write to the modem UART and PC card configuration registers, or read from the PC card CIS. |
| SPKROUT | 87 | O | **DIGITAL SPEAKER OUTPUT**: When Audio Enable AUDIO is set to '1', the digital input signal at SPKRIN is transferred to SPKROUT. Audio Enable is bit 3 in the Card Configuration Status register (CCSR). SPKROUT is tristated until the card is configured. |

### 6.4.2 DSμP PC Card (PCMCIA) Host Interface Pin Descriptions *(cont.)*

| Symbol | VQFP | Type | Description |
|---|---|---|---|
| SPKRIN | 117 | I | **DIGITAL SPEAKER INPUT**: The audio signal from the SAFE LDSPKR+ output pin should be connected to the SPKRIN pin. This digital signal is then connected to the SPKROUT pin when the Card Configuration Status register (CCSR) Audio Enable bit (AUDIO) is set to '1'. |
| WAIT* | 88 | OD | **WAIT**: This pin provides a wait-stated output for data, control, and status information during reads and writes to the modem UART. This output pin can sink up to 20 mA. |
| STSCHG* | 119 | O | **STATUS CHANGE**: When low, this signal indicates that the modem has detected an incoming ring. This pin is tristated until both the CARD EN bit in the Card Configuration and RING IND bit in the Status register (CCSR) bit are set to '1'. |
| WE* | 2 | I | **WRITE ENABLE**: When WE*, REG*, and CE1* are low, the host can write to the PC card Card Configuration registers. |
| TP[0] | 116 | I | **MANUFACTURING TEST PIN**: This pin is used during Cirrus Logic manufacturing testing. This pin should be pulled up to $V_{CC}$ for all applications. |

### 6.4.3 DSμP NVRAM, DAA and General-Purpose I/O Interface Pin Descriptions

This group of pins contains NVRAM, DAA, general-purpose I/O, and DSP test functions that use the $GPV_{CC}$ and GPGND signals for power.

#### 6.4.3.1 DSμP DAA Pin Descriptions

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| OHREL* | 24 | 18 | O | **OFF-HOOK RELAY CONTROL**: This pin is used to control a relay connected to the telephone line. This output can sink up to 10 mA for a normally open relay.<br><br>***CAUTION:*** OHREL* and VOREL* should never be activated (that is, set to '1') at the same time, as VOREL* may be used to power-up a telephone for some applications. Therefore, activating both relay drivers may cause serious damage to the modem board. |
| RING* | 23 | 17 | I | **RING SIGNAL**: The ring signal from the DAA is fed into this input pin for ring detection. |

### 6.4.3.2 DSμP DAA Pin Descriptions *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| VOREL* | 25 | 19 | O | **VOICE RELAY CONTROL**: This pin is used to control a relay for recording a voice message. This output can sink up to 10 mA.<br>***CAUTION:*** OHREL* and VOREL* should never be activated (that is, set to '1') at the same time, as VOREL* may be used to power-up a telephone for some applications. Therefore, activating both relay drivers may cause serious damage to the modem board. |

### 6.4.3.3 DSμP General-Purpose Input Pin Descriptions

Eight input pins are provided to allow modem board customization. Most of these pins can be used as either a general-purpose input or a dedicated input. These pins are only accessible and usable in voice mode. The function of each pin can be defined by using the DSμP microcontroller configuration utility program. When configured as a dedicated input pin, the OEM can select a <DLE> character pair to be sent to the host whenever the signal at the pin changes from a low-to-high or a high-to-low transition, or the signal has one character pair sent for a low-to-high transition and another for a high-to-low transition. This feature is very useful for detecting information, such as local phone pick-up or hang-up.

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| GPI [0–7] | 44:41<br>39:36 | 38:35<br>33:30 | I | **GENERAL-PURPOSE INPUT 0–7**: These eight input pins are used to monitor external circuitry. The signal at each pin can be checked by using the AT#VIN? command. |

### 6.4.3.4 DSμP General-Purpose Output Pin Descriptions

Eight output pins are provided to allow modem board customization. Most of these pins can be used as either a general-purpose output or a relay control. The function of each pin can be defined by using the DSμP microcontroller configuration utility program. The AT#VOUT=n command is used to control those pins that are configured as general-purpose output pins. The value of the general-purpose output can be read using AT#VOUT?.

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| GPO0 | 34 | 28 | O | **GENERAL-PURPOSE OUTPUT 0**: This pin is a general-purpose output that can be controlled using AT#VOUT=n command (bit 0). This output can sink up to 10 mA, and powers up as a low signal. |
| GPO1 | 33 | 27 | O | **GENERAL-PURPOSE OUTPUT 1**: This pin is a general-purpose output that can be controlled using AT#VOUT=n command (bit 1). This output can sink up to 10 mA, and powers up as a high signal. |
| GPO2 | 31 | 25 | O | **GENERAL-PURPOSE OUTPUT 2:** This pin is a general-purpose output that can be controlled using AT#VOUT=n command (bit 2). This output can sink up to 10 mA, and powers up as a high signal. |

### 6.4.3.4 DSμP General-Purpose Output Pin Descriptions *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| GPO3/ POWERON | 30 | 24 | O | **GENERAL-PURPOSE OUTPUT 3 / POWER ON STATE INDICATOR**: This pin can be configured as a general-purpose output or as power on state indicator. When configured as a general-purpose output, this pin can be controlled using AT#VOUT=n command (bit 3). When configured as power on state indicator, a high-output signal indicates the modem device set is fully powered (that is, operational mode). A low output signal indicates the modem device set is in sleep or stop mode. This output can sink up to 10 mA, and powers up as a low signal. |
| GPO4 / A/ A1REL* | 29 | 23 | O | **GENERAL-PURPOSE OUTPUT 4 / KEY TELEPHONE HOLD INDICATOR**: This pin can be configured as a general-purpose output or as A/A1* relay control. When configured as a general-purpose output, this pin can be controlled using AT#VOUT=n command (bit 4). When configured as A/A1REL*, this output signal indicates to a multi-phone system that the modem has telephone-line control. This output can sink up to 10 mA for a normally-open relay.<br><br>***CAUTION:*** The A/A1 function should never be used on an RJ-11 telephone jack, since most homes provide a second telephone signal on RJ-11 pins 2 and 5.<br><br>This output can sink up to 10 mA and powers up as a high signal. |
| GPO5 / AUXREL* | 28 | 22 | O | **GENERAL-PURPOSE OUTPUT 5/AUXILIARY RELAY CONTROL**: This pin can be configured as a general-purpose output or as Auxiliary relay control. When configured as a general-purpose output, this pin can be controlled using AT#VOUT=n command (bit 5). When configured as AUXREL*, this output signal this pin can be used to control a general-purpose relay. AUXREL* is controlled by the AT#VLN=n command. This output can sink up to 10 mA and powers up as a high signal. |
| GPO6 / CIDREL* | 27 | 21 | O | **GENERAL-PURPOSE OUTPUT 6/CALLER ID RELAY CONTROL**: This pin can be configured as a general-purpose output or as Caller ID relay control. When configured as a general-purpose output, this pin can be controlled using AT#VOUT=n command (bit 6). When configured as CIDREL*, this output signal can control a relay for receiving Caller ID. This output can sink up to 10 mA and powers up as a high signal. |

#### 6.4.3.4 DSμP General-Purpose Output Pin Descriptions *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| GPO7/PFLASH | 26 | 20 | O | **GENERAL-PURPOSE OUTPUT 7 / PROGRAM FLASH CONTROL**: This pin can be configured as a general-purpose output or used to program an external flash ROM. When configured as a general-purpose output, this pin can be controlled using AT#VOUT=n command (bit 7). When configured as PFLASH, this output signal may be used to control circuitry for changing the flash ROM program $V_{CC}$ voltage. This output can sink up to 10 mA and powers up as a low signal. |

#### 6.4.3.5 DSμP NVRAM Pin Descriptions

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| NVCS | 20 | 14 | O | **NON-VOLATILE RAM CHIP SELECT**: This output pin provides the NVRAM chip select for reading and writing to the NVRAM. This signal should be connected to the NVRAM CS pin. |
| NVDIO | 22 | 16 | I/O | **NON-VOLATILE RAM SERIAL DATA INPUT/OUTPUT**: This pin receives the serial data stream from the NVRAM DO pin, and provides the serial data stream into the NVRAM DI pin. |
| NVSK | 21 | 15 | O | **NON-VOLATILE RAM SHIFT CLOCK**: This output pin provides the clock for the NVRAM serial data stream. This pin should be connected to the NVRAM SK pin. |

#### 6.4.3.6 DSμP General Pin Descriptions

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| $GPV_{CC}$ | 35 | 29 | PWR | **GENERAL-PURPOSE I/O +5-V POWER SUPPLY**: The DSμP requires only +5 V to perform all the digital processing. |
| GPGND | 32 | 26 | GND | **GENERAL-PURPOSE I/O DIGITAL GROUND**. |
| DADR/DATA | 45 | 39 | O | **DSP EXPANSION BUS ADDRESS LATCH SIGNAL**. |
| DEBR/W* | 48 | 42 | O | **DSP EXPANSION BUS DATA RAM READ/WRITE* LINE**: This pin selects whether the DSμP DSP is reading or writing to the external RAM. This signal works in conjunction with the DRCS* pin. |
| DIRCS* | 47 | 41 | O | **DSP INSTRUCTION RAM CHIP SELECT**. |
| GPIOEM | 50 | 44 | O | **GPIO EMULATION SIGNAL**: This pin is only used by Cirrus Logic emulator boards and is never used for any modem applications. |

**Table 6.4.3.6 DSμP General Pin Descriptions** *(cont.)*

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| RESERVED | 49 | 43 | – | **NO CONNECT:** This pin is reserved for future enhancements to the device set and should be left unconnected. |

### 6.4.4 DSμP Microcontroller Expansion Bus Interface Pin Descriptions

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| $MV_{CC}$ | 74 | 68 | PWR | **MICROCONTROLLER EXTERNAL BUS +5-V POWER SUPPLY**: The DSμP requires only +5 volts to perform all the digital processing |
| MGND | 60, 84 | 54, 78 | GND | **MICROCONTROLLER EXTERNAL BUS DIGITAL GROUND**. |
| DRCS* | 71 | 65 | O | **DATA RAM CHIP SELECT**: This output pin provides the chip select for external RAM. |
| EBAD[0–15] | 92:85<br>83:75 | 86:79<br>77:69 | O | **EXPANSION BUS ADDRESS LINES [0–15]**: These pins provide the addresses necessary for accessing the DSμP and external memory. |
| EBDA[0–15] | 69:65<br>63:61<br>59:58<br>56:51 | 63:59<br>57:55<br>53:52<br>50:45 | I/O | **EXPANSION BUS DATA LINES [0–15]**: This bus provides bidirectional data access between the DSμP and external memory. |
| EBRD* | 73 | 67 | O | **EXPANSION BUS READ LINE**: The DSμP microcontroller sets this signal low when it reads from an external device. |
| EBWR* | 72 | 66 | O | **EXPANSION BUS WRITE LINE**: The DSμP microcontroller sets this signal low when it writes to an external device. |
| IRCS* | 70 | 64 | O | **INSTRUCTION ROM CHIP SELECT**: This output pin provides the chip select for external ROM. |

### 6.4.5 DSμP–SAFE Interface Pin Descriptions (128-pin SQFP)

| Symbol | SQFP | Type | Description |
|---|---|---|---|
| AFEVCC | 16 | PWR | **SAFE INTERFACE +5 V POWER SUPPLY**: The DSμP requires only +5 V to perform all digital processing. |
| AFEGND | 14 | GND | **SAFE INTERFACE DIGITAL GROUND**. |
| AFECLK | 15 | O | **SAFE CLOCK**: This pin provides the clock source for the SAFE device. |
| TXDATA | 12 | O | **TX DATA**: This pin transmits serial data from the DSμP to the SAFE device. |

**Table 6.4.5 DSμP–SAFE Interface Pin Descriptions (128-pin SQFP)** *(cont)*

| Symbol | SQFP | Type | Description |
|---|---|---|---|
| TXENA | 13 | O | **TX ENABLE**: This pin enables the transmittal of data from the DSμP to the SAFE device. |
| TXSTRB* | 11 | O | **TRANSMIT STROBE**: This pin provides the DSμP with the necessary clock signal required to send the serial transmit data from the DSμP to the SAFE device. |
| RXDATA | 18 | I | **RX DATA**: Through this pin the DSμP receives serial data from the SAFE device. |
| RXSTRB* | 19 | O | **RECEIVE STROBE**: This pin provides the DSμP with the necessary clock signal required to receive the serial receive data from the SAFE device. |

### 6.4.6 DSμP CORE Power Pin Descriptions

| Symbol | SQFP | VQFP | Type | Description |
|---|---|---|---|---|
| CGND | 46, 64 | 40, 58 | GND | **CORE DIGITAL GROUND**. |
| $CV_{CC}$ | 40, 57, 104 | 34, 51 94 | PWR | **CORE +5 V POWER SUPPLY**: The DSμP requires only +5 V to perform all the digital processing. |

## 6.5 SAFE Pin Descriptions

### 6.5.1 SAFE General Pin Descriptions

| Symbol | VQFP | Type | Description |
|---|---|---|---|
| LDSPKR+<br>LDSPKR- | 17<br>20 | O<br>O | **LOUDSPEAKER OUTPUT**: These pins provide a differential output signal for driving an external loudspeaker. These pins can be connected directly to a ≥ 8-Ω speaker or a speaker amplifier. |
| MIC+ | 9 | I | **MICROPHONE + INPUT**: This input pin is a single-ended amplifier input for a microphone. It requires a 10-kΩ pull-up resistor to the SAFE VCM pin. If the microphone function is not used, then connect this pin to analog ground. |
| MIC– | 10 | I | **MICROPHONE – INPUT**: This pin provides a switched ground connection that interrupts the microphone bias current during power down. If the microphone function is not used or if disabling the microphone bias current during power down is not desirable, then connect this pin to analog ground. |

### 6.5.1 SAFE General Pin Descriptions *(cont.)*

| Symbol | VQFP | Type | Description |
|---|---|---|---|
| N/C | 32 | – | **NO CONNECT**: This pin should be left floating. |
| RESET | 14 | I | **SAFE RESET**: This pin is used to generate a SAFE reset. A reset is accomplished by pulsing the signal at the RESET pin from a low to high to low. The RESET input pin must be high for at least 10 µs. The SAFE requires 200 ms, after the high-to-low transition, before communicating with the DSµP. |

### 6.5.2 SAFE Power Supply Pin Descriptions (CL-MD1724)

| Symbol | VQFP | Type | Description |
|---|---|---|---|
| DGND | 23, 28, 29, 30, 33 | GND | **DIGITAL GROUND REFERENCE**. |
| DV+ | 27 | PWR | **DIGITAL SUPPLY** (5 V ±5%). |
| LSGND | 15,18, 19, 21, 22 | AGND | **LOUDSPEAKER ANALOG GROUND REFERENCE**. |
| LSV+ | 16 | PWR | **LOUDSPEAKER SUPPLY VOLTAGE** (5 V ±5%). |
| RXGND | 4, 6, 11,12 | AGND | **RECEIVER ANALOG GROUND REFERENCE**. |
| RXV+ | 13 | PWR | **RECEIVER ANALOG SUPPLY VOLTAGE** (5 V ±5%). |
| TXGND | 1, 38, 39, 41, 43, 44 | AGND | **TRANSMITTER ANALOG GROUND REFERENCE**. |
| TXV+ | 37 | PWR | **TRANSMITTER ANALOG SUPPLY VOLTAGE** (5 V ±5%). |
| VCM | 3 | I | **VOLTAGE COMMON MODE**: The SAFE provides an internal 2.5-V reference for the differential analog circuitry. This pin allows the reference to be bypassed using an external 1.0-µF capacitor. |
| VREF+ | 2 | I | **VOLTAGE REFERENCE BUFFER**: The SAFE incorporates an VREF-5 internal differential voltage reference. These pins allow the internal differential reference to be bypassed using an external 1.0-µF capacitors. |

### 6.5.3 SAFE—DSμP Interface Pin Descriptions (CL-MD1724)

| Symbol | VQFP | Type | Description |
|---|---|---|---|
| TXSTRB* | 11 | O | **TRANSMIT STROBE**: This pin provides the clock signal required for the SAFE device to receive the serial transmit data from the DSμP. |
| TXDATA | 12 | O | **TX DATA**: Through this pin the SAFE device receives serial data transmitted from the DSμP. |
| TXENA | 13 | O | **TX ENABLE**: This pin enables the transmittal of data from the DSμP to the SAFE device. |
| AFEGND | 14 | GND | **SAFE INTERFACE DIGITAL GROUND**. |
| AFECLK | 15 | O | **SAFE CLOCK**: This pin provides the clock source for the SAFE device. |
| AFEVcc | 16 | PWR | **SAFE INTERFACE +5 V POWER SUPPLY**: The DSμP requires only +5 V to perform all digital processing. |
| RXENA | 17 | I | **RX ENABLE**: This pin should be left unconnected. |
| RXDATA | 18 | I | **RX DATA**: This pin transmits the receive serial data from the SAFE device to the DSμP. |
| RXSTRB* | 19 | O | **RECEIVE STROBE**: This pin provides the clock signal required for the DSμP to receive the serial receive data from the SAFE device. |

### 6.5.4 SAFE DAA Interface Pin Descriptions (CL-MD1724)

| Symbol | VQFP | Type | Description |
|---|---|---|---|
| RX+<br>RX- | 7<br>8 | I<br>I | **RECEIVE ANALOG DATA**: These input pins receive the analog differential signals from the DAA. |
| TX+ | 40 | O | **TRANSMIT ANALOG DATA**: These pins provide the analog TX-42O transmitter differential output signals to the DAA. |

# 7. ELECTRICAL SPECIFICATIONS

## 7.1 Absolute Maximum Ratings

Supply voltage ($V_{CC}$) ..... +6.0 V
Input voltages, with respect to ground..... –0.3 Volts to $V_{CC}$ +0.5 V
Operating temperature ($T_A$)..... 0°C to 70°C
Storage temperature..... –65°C to 150°C

**NOTE**: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 7.2 Recommended Operating Conditions

Supply voltage ($V_{CC}$) ..... 5 V ±5%
Operating free air ambient temperature..... 0°C < $T_A$ < 70°C
Crystal frequencies ..... 22.1184 MHz

## 7.3 DC Electrical Characteristics — DSμP

(@ $V_{CC}$ = 5 V ±5%; $T_A$ = 0°C to 70°C; $V_{OL}$ for open-drain signals is 0.5 V @ 16 mA sinking; $V_{IH}$ is 2.7 V minimum on RESET.)

| Symbol | Parameter | MIN | TYP | MAX | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | –0.5 | – | 0.8 | V | |
| $V_{IH}$ | Input high voltage | 2.0 | – | $V_{CC}$ | V | |
| $V_{OL}$ | Output low voltage | | – | 0.4 | V | $I_{OL}$ = 2.4 mA |
| $V_{OH}$ | Output high voltage | 2.4 | – | | V | $I_{OH}$ = –400 μA |
| $I_{IL}$ | Input leakage current | –10 | – | 10 | μA | 0 < $V_{IN}$ < $V_{CC}$ |
| $I_{LL}$ | Data bus tristate leakage current | –10 | – | 10 | μA | 0 < $V_{OUT}$ < $V_{CC}$ |
| $I_{OC}$ | Open-drain output leakage current | –10 | – | 10 | μA | 0 < $V_{OUT}$ < $V_{CC}$ |
| $I_{CC}$ | Power supply current | – | 64 | 96 | mA | Operational mode CLK = 22.1184 MHz |
| $I_{HD[0–7]}$ | Host data bus | – | – | 16 | mA | 0 < $V_{OUT}$ < $V_{CC}$ |
| $I_{OD}$ $I_{OT}$ | IOCHRDY, WAIT* pin HINT, IREQ pins | – | – | 20 | mA | 0 < $V_{OUT}$ < $V_{CC}$ |
| $C_{IN}$ | Input capacitance | – | – | 10 | pF | |
| $C_{OUT}$ | Output capacitance | – | – | 10 | pF | |

## 7.4 AC/DC Electrical Characteristics — CL-MD1724 (SAFE)

(@ $V_{CC}$ = 5 V ± 5%, $T_A$ = 0°C to 70°C)

| Symbol | Parameter | MIN | TYP | MAX | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $P_D$ | Power dissipation | – | 130 | 195 | mW | Operational mode |
| $P_{Down}$ | Power dissipation (power-down mode) | – | – | 500 | µW | Loud speaker driver off |
| $I_A$ | Analog current (TV+, RV+) | – | 24 | – | mW | Loud speaker driver off |
| $I_D$ | Digital current (DV+) | – | 2 | – | mA | |
| $I_{IDS}$ | Loud speaker current (LDSPKR+, LDSPKR–) | – | – | 125 | mA | |
| $R_X$ | Loud speaker impedance | 8 | – | – | Ω | |

## 7.5 Index of Timing Information

**Table 7-1. Parallel Host Interface Timing (ADRDEC Pin Low) — Write Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | HA[0–2] setup time to HCS* low | 0 | – | ns |
| $t_2$ | HCS* low to HWR* low setup time | 10 | – | ns |
| $t_3$ | HD[0–7] valid from HWR* low | – | 10 | ns |
| $t_4$ | HWR* low to IOCHRDY low | – | 30 | ns |
| $t_5$ | HWR* low to IOCHRDY tristate | – | 250 | ns |
| $t_6$ | HWR* hold time after IOCHRDY high | 0 | – | ns |
| $t_7$ | HD[0–7] hold time after HWR* high | 0 | – | ns |
| $t_8$ | HCS* hold time after HWR* high | 0 | – | ns |
| $t_9$ | HA[0–2] hold time after HWR* high | 0 | – | ns |

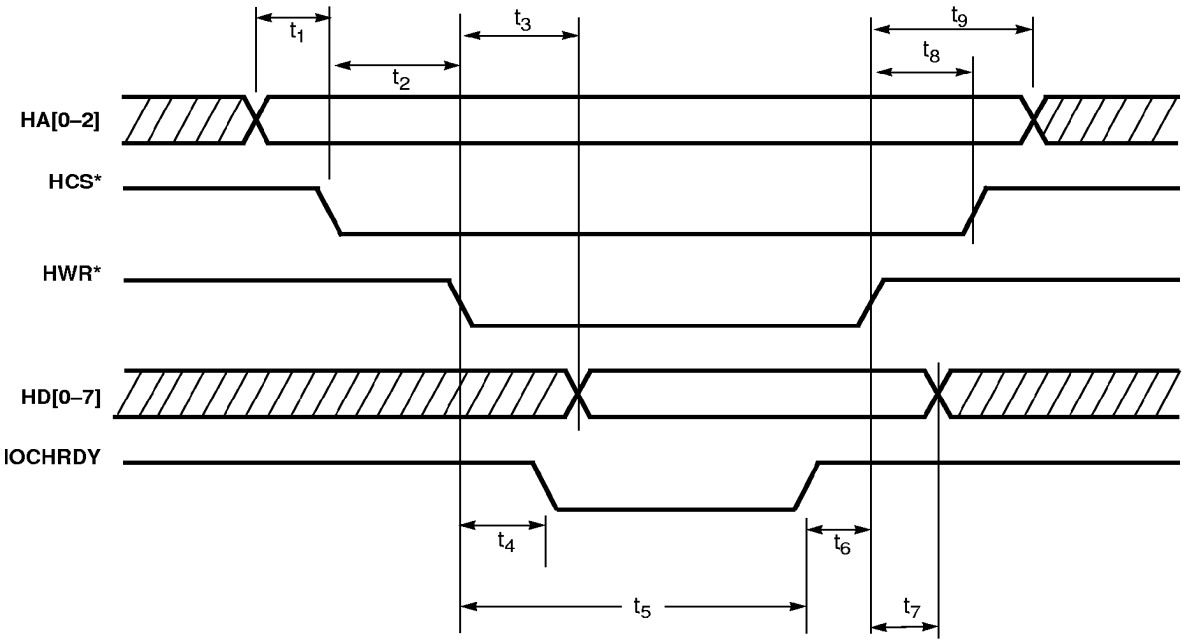



**Figure 7-1. Parallel Host Interface Timing Diagram (ADRDEC Pin Low) — Write Cycle**

**Table 7-2. Parallel Host Interface Timing (ADRDEC Pin High) — Write Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | HA[0–9], AEN setup time to HWR* low | 10 | – | ns |
| $t_2$ | HD[0–7] valid from HWR* low | – | 10 | ns |
| $t_3$ | HWR* low to IOCHRDY low | – | 30 | ns |
| $t_4$ | HWR* low to IOCHRDY tristate | – | 250 | ns |
| $t_5$ | HWR* hold time after IOCHRDY high | 0 | – | ns |
| $t_6$ | HD[0–7] hold time after HWR* high | 0 | – | ns |
| $t_7$ | HA[0–9], AEN hold time after HWR* high | 0 | – | ns |

**NOTE**: HCS* must be connected high when ADRDEC is connected high.

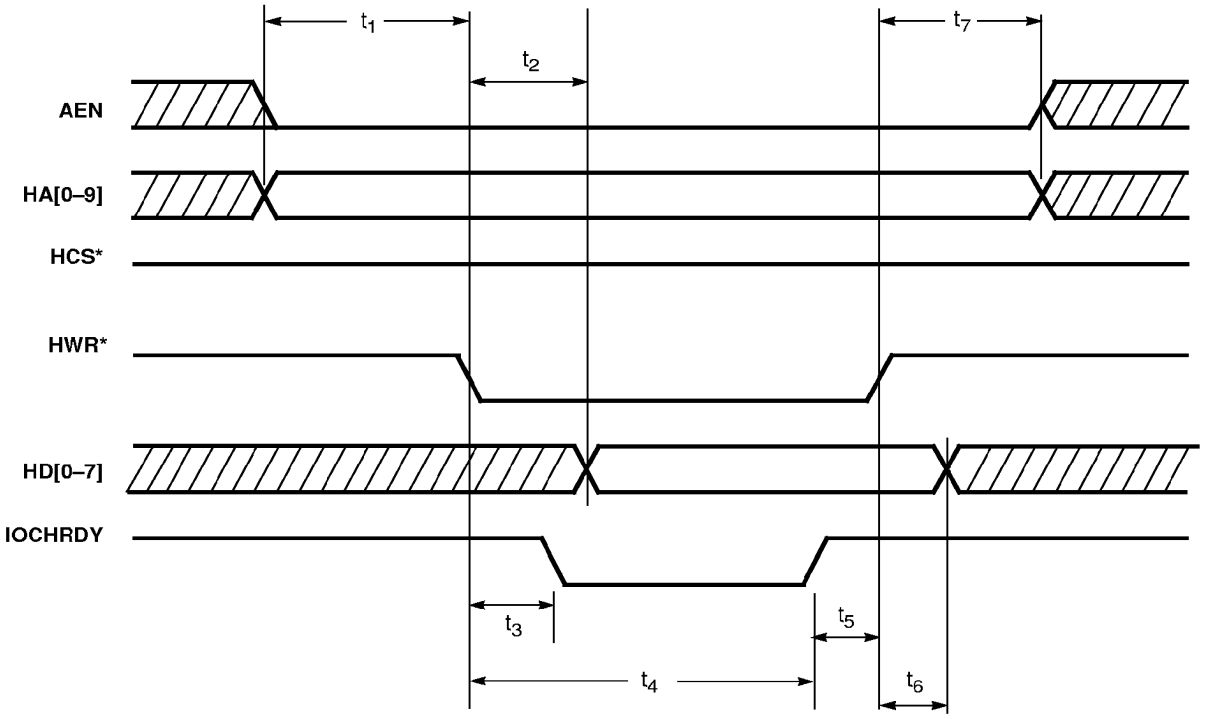



**Figure 7-2. Parallel Host Interface Timing Diagram (ADRDEC Pin High) — Write Cycle**

**Table 7-3. Parallel Host Interface Timing (ADRDEC Pin Low) — Read Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | HA[0–2] setup time to HCS* low | 0 | – | ns |
| $t_2$ | HCS* setup time to HRD* low | 10 | – | ns |
| $t_3$ | HD[0–7] valid after HRD* low | – | 250 | ns |
| $t_4$ | HRD* low to IOCHRDY low | – | 30 | ns |
| $t_5$ | HRD* low to IOCHRDY tristate | – | 250 | ns |
| $t_6$ | HRD* hold time after IOCHRDY high | 0 | – | ns |
| $t_7$ | HRD* high to HD[0–7] tristate | – | 30 | ns |
| $t_8$ | HCS* hold time after HRD* high | 0 | – | ns |
| $t_9$ | HA[0–2] hold time after HRD* high | 0 | – | ns |

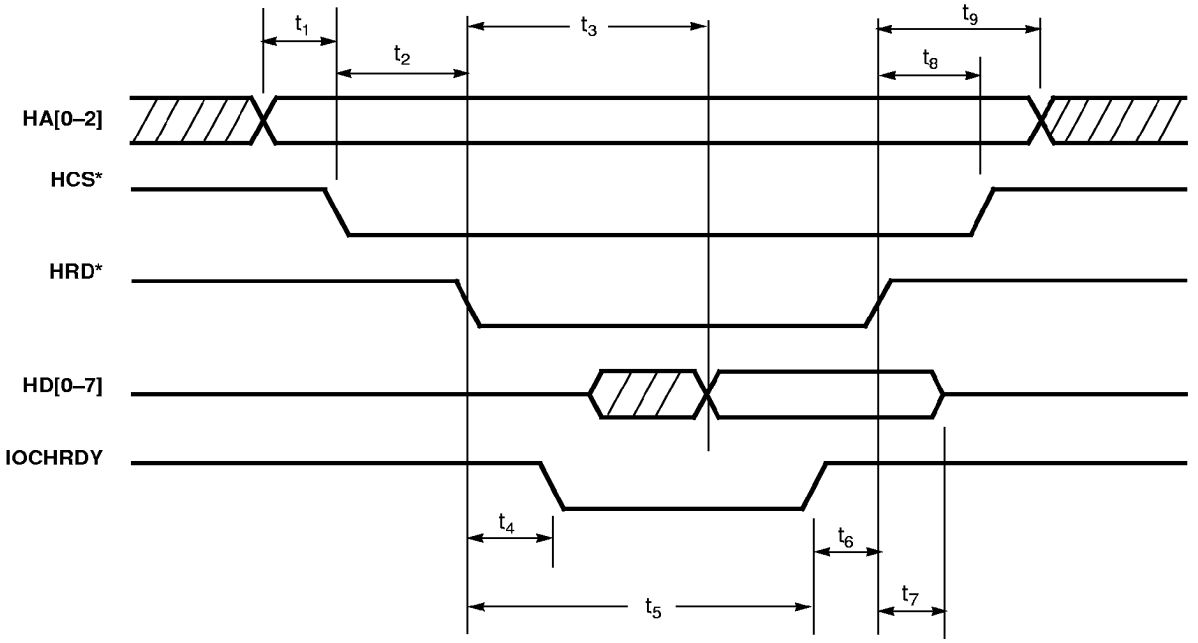



**Figure 7-3. Parallel Host Interface Timing Diagram (ADRDEC Pin Low) — Read Cycle**

**Table 7-4. Parallel Host Interface Timing (ADRDEC Pin High) — Read Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | HA[0–9], AEN setup time to HRD* low | 10 | – | ns |
| $t_2$ | HD[0–7] valid after HRD* low | – | 250 | ns |
| $t_3$ | HRD* low to IOCHRDY low | – | 30 | ns |
| $t_4$ | HRD* low to IOCHRDY tristate | – | 250 | ns |
| $t_5$ | HRD* hold time after IOCHRDY high | 0 | – | ns |
| $t_6$ | HRD* high to HD[0–7] tristate | – | 30 | ns |
| $t_7$ | HA[0–9], AEN hold time after HRD* high | 0 | – | ns |

**NOTE**: HCS* must be connected high when ADRDEC is connected high.

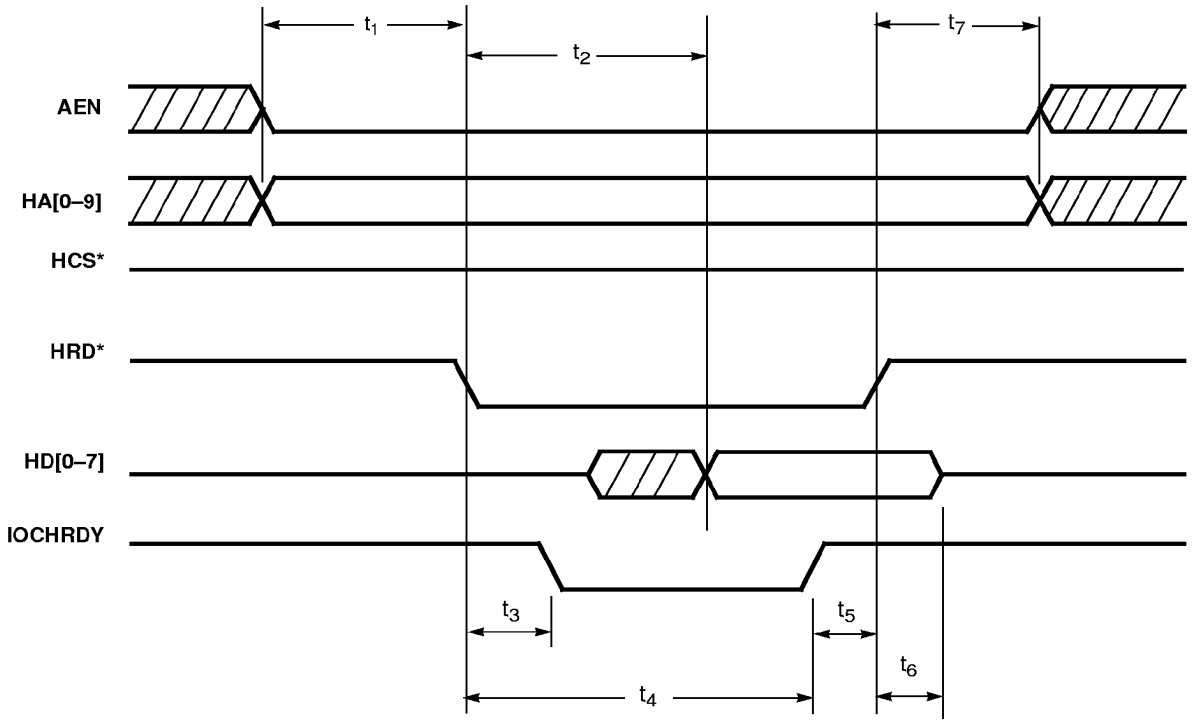



**Figure 7-4. Parallel Host Interface Timing Diagram (ADRDEC Pin High) — Read Cycle**

**Table 7-5. Parallel Host Interface DMA Timing — Write Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | DRQ low from HWR* low | – | 45 | ns |
| $t_2$ | HD[0–7] valid before HWR* goes high | 45 | – | ns |
| $t_3$ | HWR* active duration | 100 | – | ns |
| $t_4$ | HD[0–7] hold time after HWR* high | 10 | – | ns |
| $t_5$ | DACK* hold time after HWR* high | 10 | – | ns |

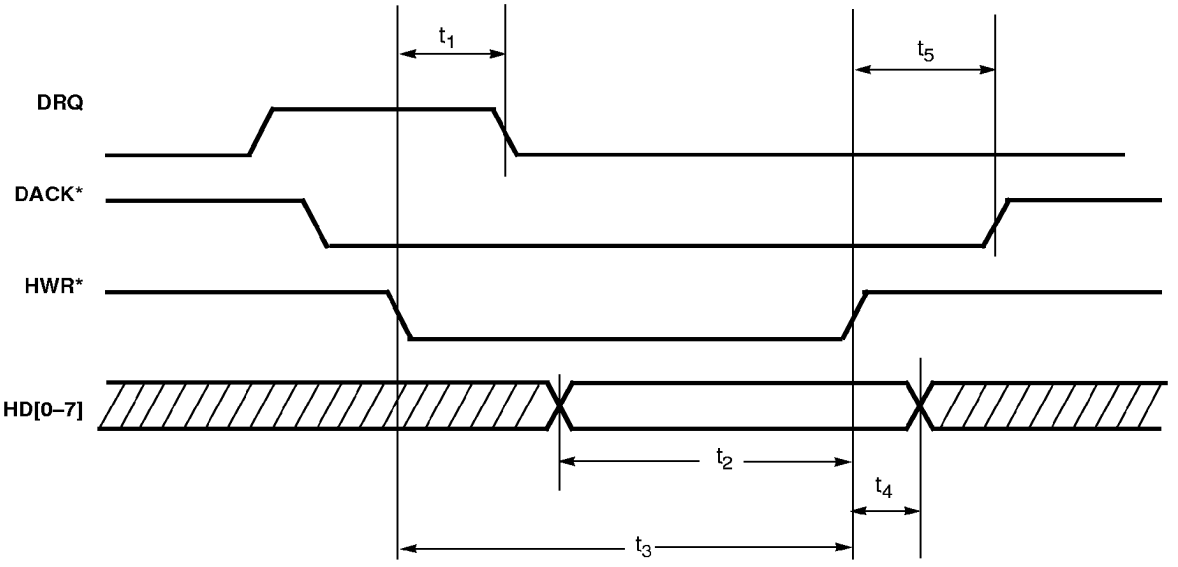



**Figure 7-5. Parallel Host Interface DMA Timing Diagram — Write Cycle**

**Table 7-6. Parallel Host Interface DMA Timing — Read Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | DRQ low from HRD* low | – | 45 | ns |
| $t_2$ | HD[0–7] valid after HRD* goes low | – | 45 | ns |
| $t_3$ | HRD* active duration | 100 | – | ns |
| $t_4$ | HD[0–7] hold time after HRD* high | – | 0 | ns |
| $t_5$ | DACK* hold time after HRD* high | 10 | – | ns |

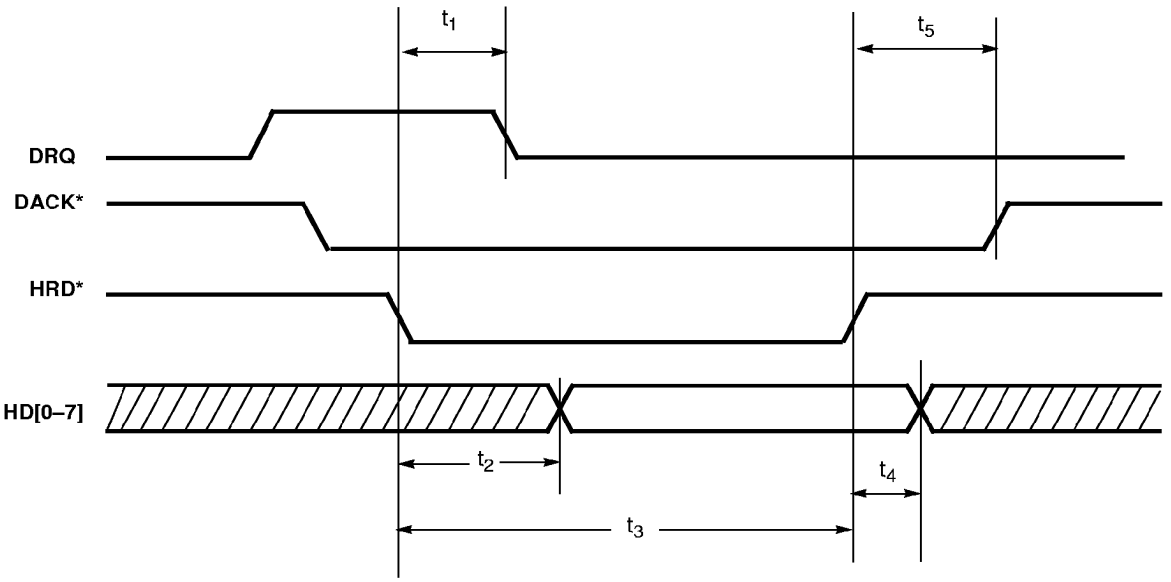



**Figure 7-6. Parallel Host Interface DMA Timing Diagram — Read Cycle**

**Table 7-7. PC Card UART Interface Timing — Write Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | HA[0–2] setup time to IOWR* low | 10 | – | ns |
| $t_2$ | REG* and CE1* low to IOWR* low setup time | 10 | – | ns |
| $t_3$ | HD[0–7] valid from IOWR* low | – | 10 | ns |
| $t_4$ | IOWR* low to WAIT* low | – | 35 | ns |
| $t_5$ | IOWR* low to WAIT* high | – | 250 | ns |
| $t_6$ | IOWR* hold time after WAIT* high | 0 | – | ns |
| $t_7$ | HD[0–7] hold time after IOWR* high | 0 | – | ns |
| $t_8$ | REG* and CE1* hold time after IOWR* high | 0 | – | ns |
| $t_9$ | HA[0–2] hold time after IOWR* high | 0 | – | ns |
| $t_{10}$ | IOWR* low to INPACK* low | – | 45 | ns |
| $t_{11}$ | INPACK* hold time after IOWR* high | – | 45 | ns |

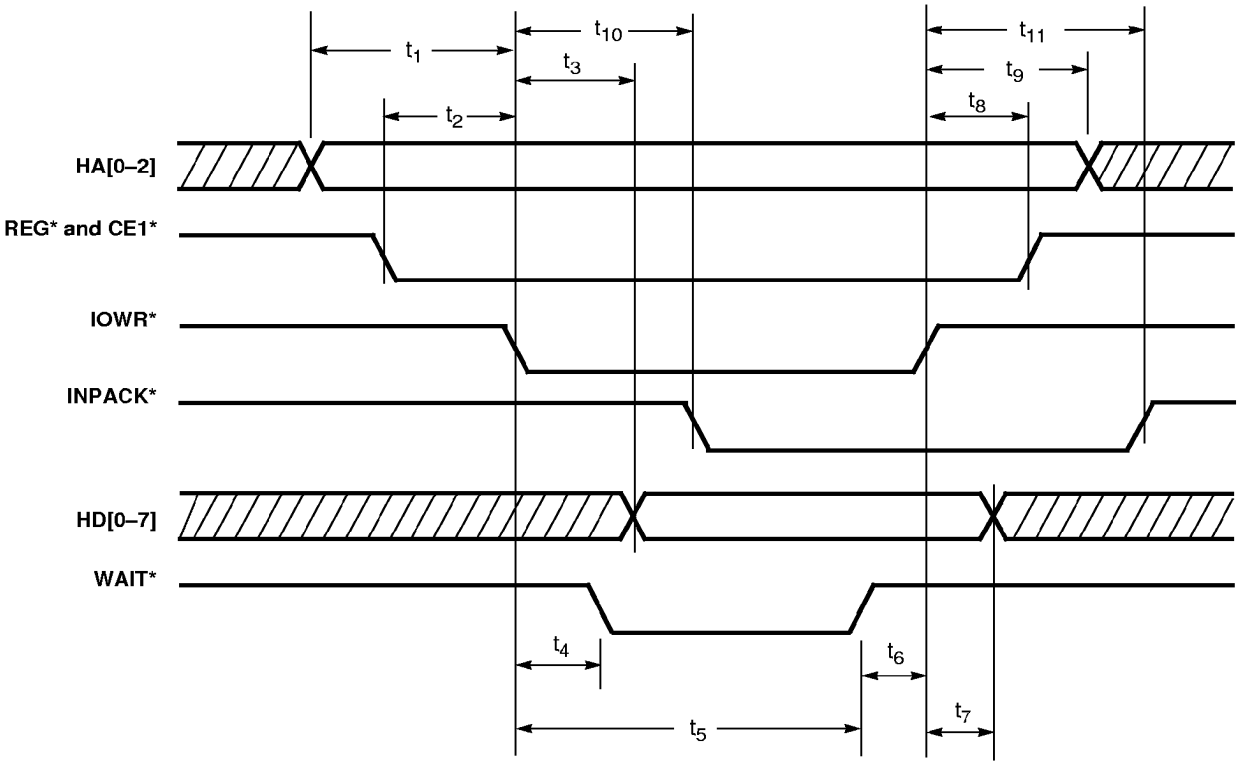



**Figure 7-7. PC Card UART Interface Timing Diagram — Write Cycle**

**Table 7-8. PC Card UART Interface Timing — Read Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | HA[0–2] setup time to IORD* low | 10 | – | ns |
| $t_2$ | REG* and CE1* setup time to IORD* low | 10 | – | ns |
| $t_3$ | HD[0–7] valid after IORD* low | – | 250 | ns |
| $t_4$ | IORD* low to WAIT* low | – | 35 | ns |
| $t_5$ | IORD* low to WAIT* high | – | 250 | ns |
| $t_6$ | IORD* hold time after WAIT* high | 0 | – | ns |
| $t_7$ | IORD* high to HD[0–7] tristate | – | 30 | ns |
| $t_8$ | REG* and CE1* hold time after IORD* high | 0 | – | ns |
| $t_9$ | HA[0–2] hold time after IORD* high | 0 | – | ns |
| $t_{10}$ | IORD* low to INPACK* low | – | 45 | ns |
| $t_{11}$ | INPACK* hold time after IORD* high | – | 45 | ns |

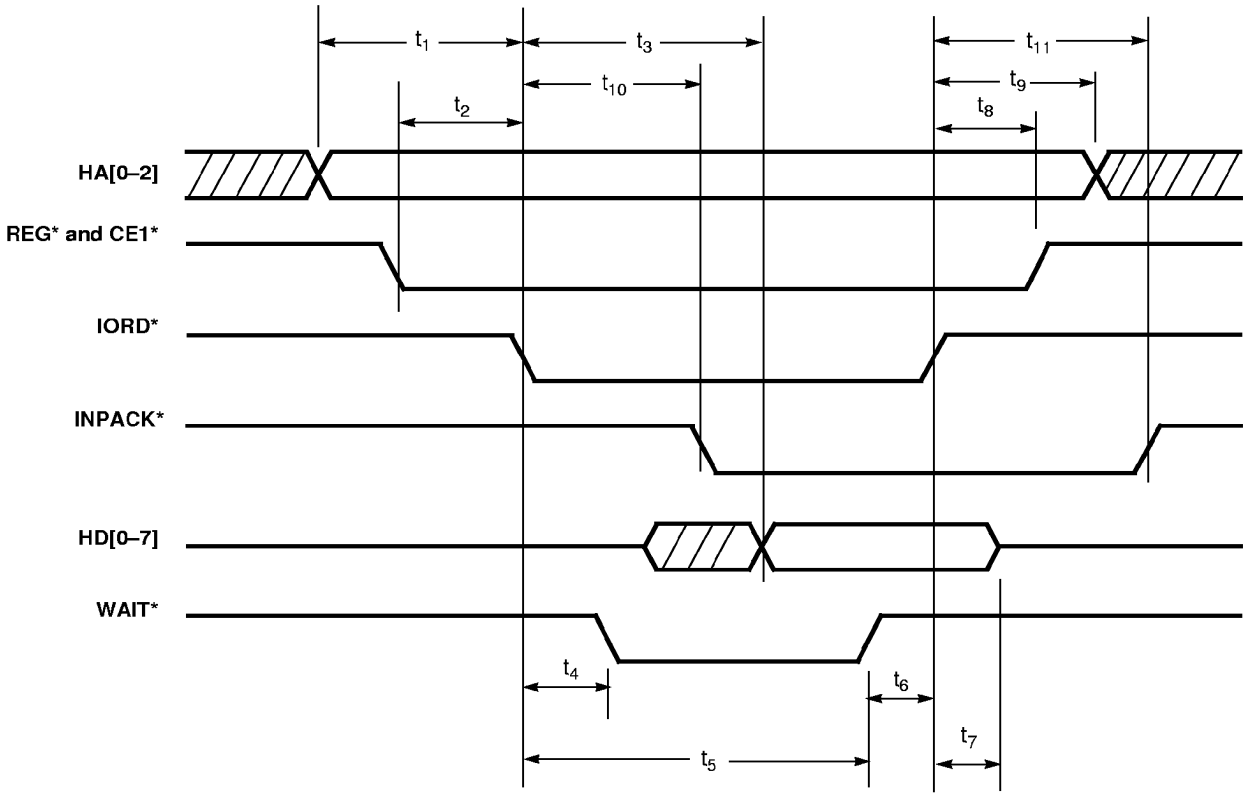



**Figure 7-8. PC Card UART Interface Timing Diagram — Read Cycle**

**Table 7-9. PC Card Configuration Register Interface Timing — Write Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | HA[0–2] setup time to REG* and CE1* low | 0 | – | ns |
| $t_2$ | REG* and CE1* low to WE* low setup time | 10 | – | ns |
| $t_3$ | HD[0–7] valid before WE* high | 40 | – | ns |
| $t_4$ | WE* active duration | 60 | – | ns |
| $t_5$ | HD[0–7] hold time after WE* high | 15 | – | ns |
| $t_6$ | REG* and CE1* hold time after WE* high | 10 | – | ns |
| $t_7$ | HA[0–2] hold time after WE* high | 15 | – | ns |
| $t_8$ | WE* low to INPACK* low | – | 45 | ns |
| $t_9$ | INPACK* hold time after WE* high | – | 45 | ns |

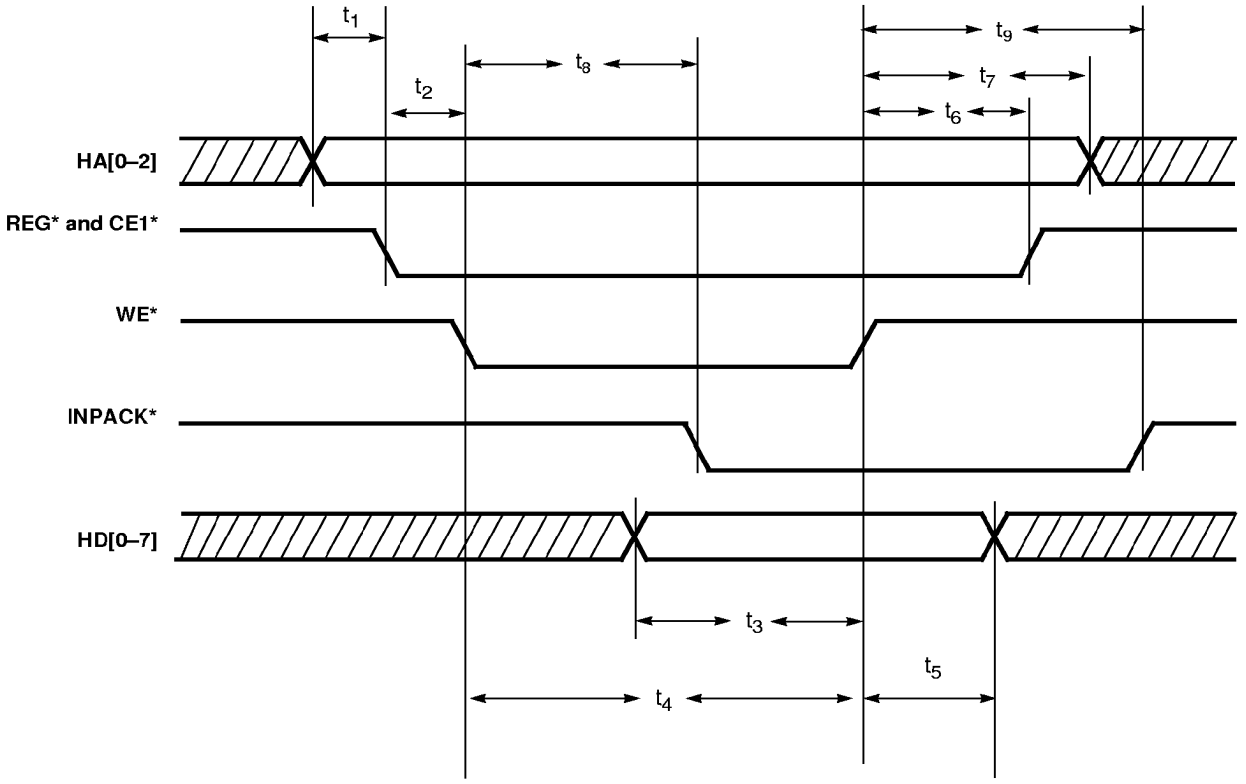



**Figure 7-9. PC Card Configuration Register Interface Timing Diagram — Write Cycle**

**Table 7-10. PC Card CIS and Configuration Register Interface Timing — Read Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | HA[0–2] setup time to REG* and CE1* low | 0 | – | ns |
| $t_2$ | REG* and CE1* low to OE* low setup time | 10 | – | ns |
| $t_3$ | HD[0–7] valid after OE* low | – | 50 | ns |
| $t_4$ | OE* active duration | 60 | – | ns |
| $t_5$ | HD[0–7] hold time after OE* high | – | 40 | ns |
| $t_6$ | REG* and CE1* hold time after OE* high | 10 | – | ns |
| $t_7$ | HA[0–2] hold time after OE* high | 15 | – | ns |
| $t_8$ | OE* low to INPACK* low | – | 45 | ns |
| $t_9$ | INPACK* hold time after OE* high | – | 45 | ns |

**NOTE**: The timing information is defined for the internal CIS ROM. However, if an external CIS ROM is used, then the timing information must be calculated based on the following: $t_3$, $t_6$, access time of the external CIS ROM used, and the PC Card 2.1 specification.

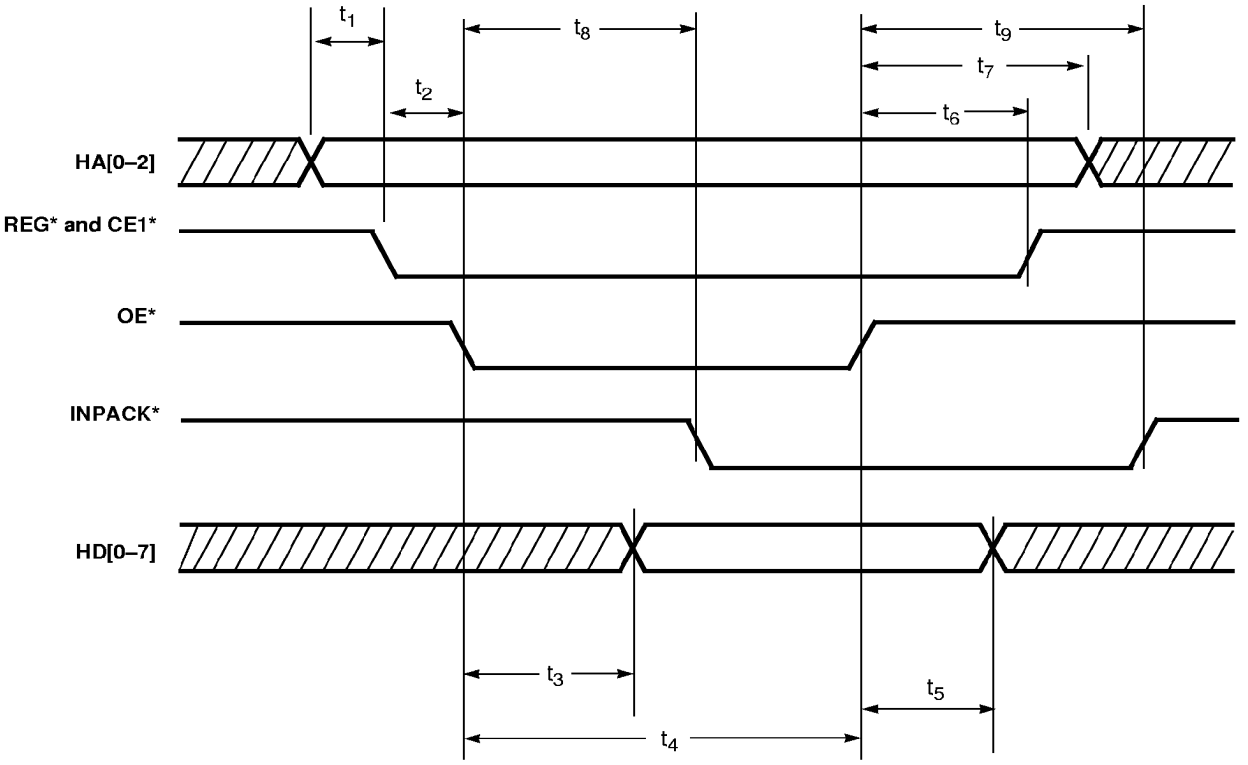



**Figure 7-10. PC Card CIS and Configuration Register Interface Timing Diagram — Read Cycle**

**Table 7-11. Expansion Bus Timing — Write Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | DRCS*, DACCS* setup time before EBR/W* low | 10 | – | ns |
| $t_2$ | EBAD[0–15] setup time before EBR/W* low | 10 | – | ns |
| $t_3$ | EBAD[0–15] hold time after EBR/W* high | 10 | – | ns |
| $t_4$ | EBDA[0–15] valid before EBR/W* high | 40 | – | ns |
| $t_5$ | EBR/W* active duration | 70 | – | ns |
| $t_6$ | DRCS*, DACCS* high after EBR/W* high | 10 | – | ns |
| $t_7$ | EBDA[0–15] hold time after EBR/W* | 2 | – | ns |

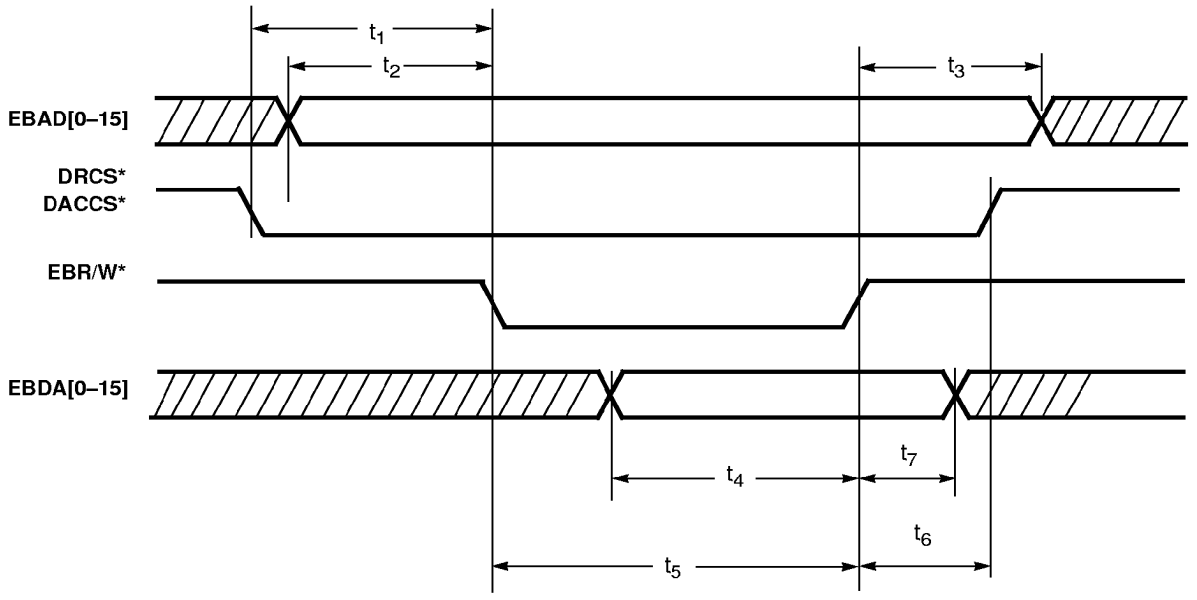



**Figure 7-11. Expansion Bus Timing Diagram — Write Cycle**

**Table 7-12. Expansion Bus Timing — Read Cycle**

| Symbol | Parameter | MIN | MAX | Units |
|---|---|---|---|---|
| $t_1$ | DRCS*, DACCS*, EBAD[0–15] active duration | 165 | – | ns |
| $t_2$ | EBDA[0–15] stable after DRCS*, DACCS* high | – | 120 | ns |
| $t_3$ | EBDA[0–15] setup time before DRCS*, DACCS* high | 45 | – | ns |
| $t_4$ | EBDA[0–15] hold time after DRCS* DACCS* high | 2 | – | ns |

**NOTE**: The expansion bus read access times are:
≤ 55 ns for an external ROM.
≤ 120 ns for an SRAM.

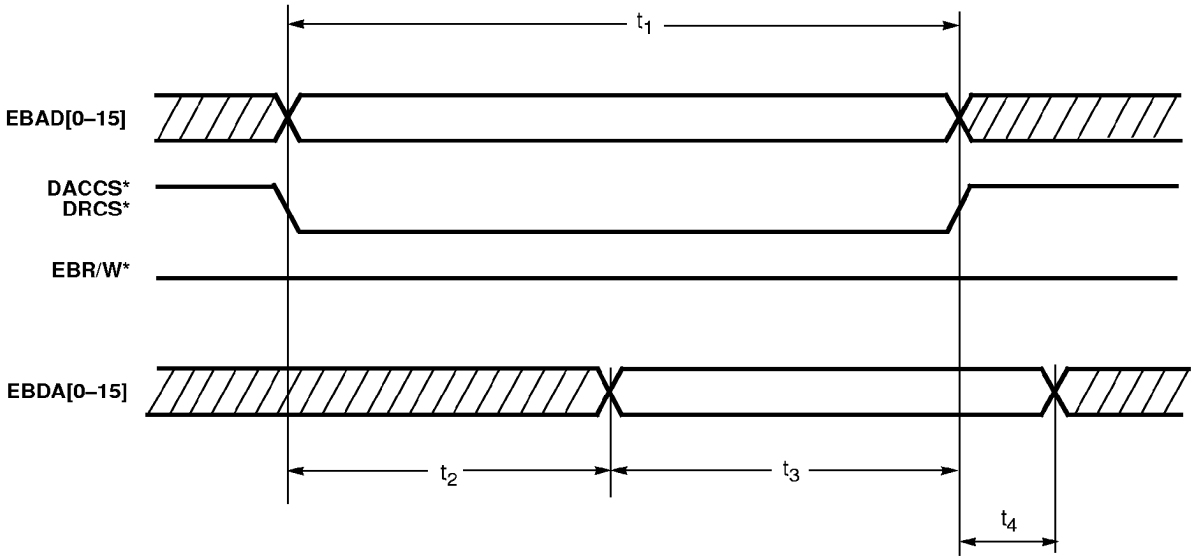
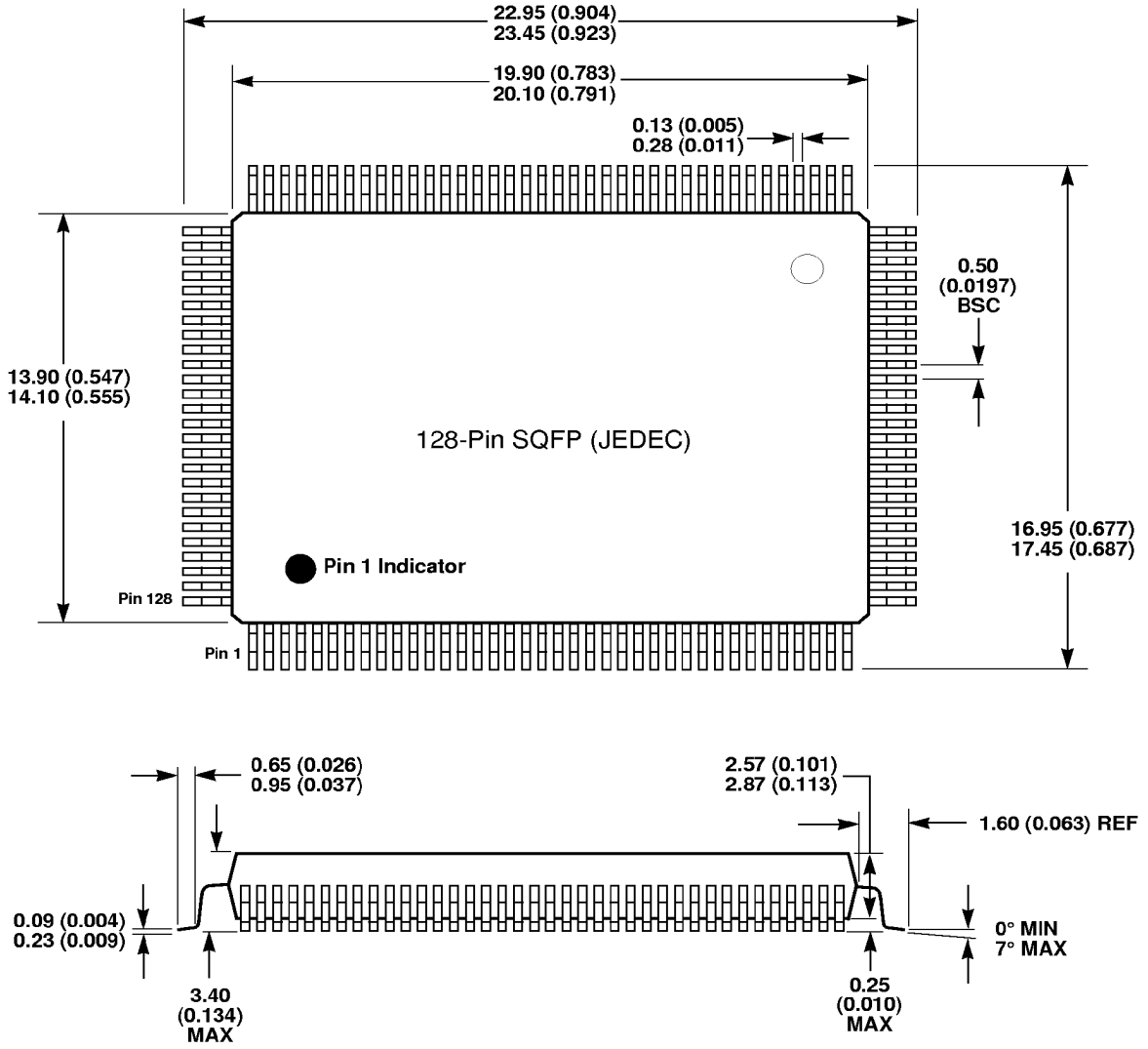



**Figure 7-12. Expansion Bus Timing Diagram — Read Cycle**

# 8. SAMPLE PACKAGE INFORMATION

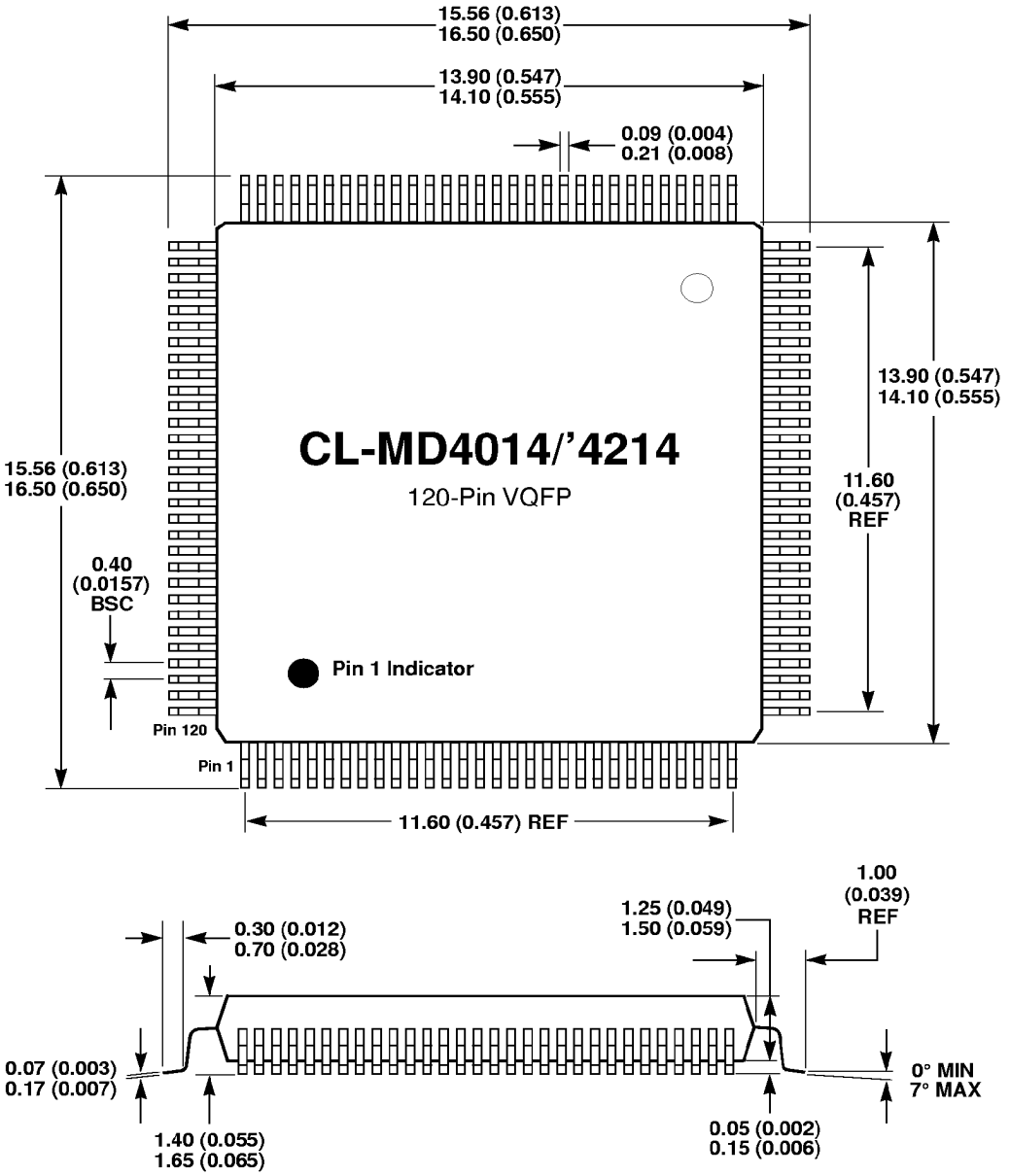
## 8.1 128-Pin SQFP (JEDEC) Package Outline Drawing




**NOTES:**

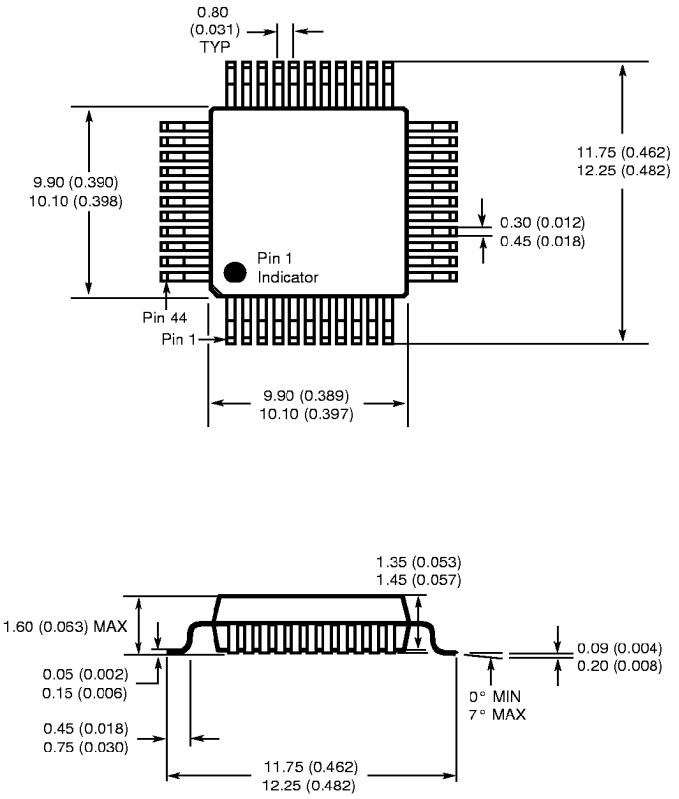
1) Dimensions are expressed in millimeters (inches); the controlling dimension is expressed in millimeters.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

## 8.2 120-Pin VQFP Package Outline Drawing




1) Dimensions are expressed in millimeters (inches); the controlling dimension is expressed in millimeters.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

## 8.3 44-Pin VQFP Package Outline Drawing




**NOTES**:

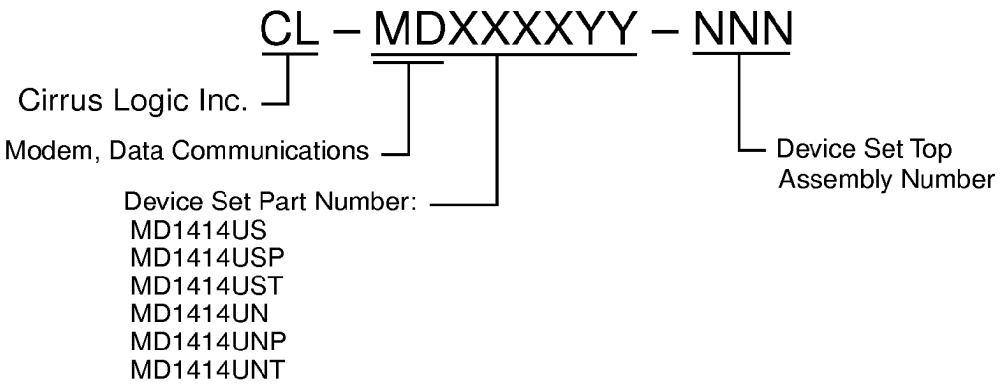
1) Dimensions are expressed in millimeters (inches); the controlling dimension is expressed in millimeters.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

# 9. ORDERING INFORMATION

### *Device Set Composition*

| Market | Parallel/Serial Host Interface | PC card (PCMCIA) Host Interface | Plug-and-Play Interface |
|---|---|---|---|
| United States | **CL-MD1414US**<br>DSμP (CL-MD4214)<br>SAFE (CL-MD1724) | **CL-MD1414USP**<br>DSμP (CL-MD4914)<br>SAFE (CL-MD1724) | **CL-MD1414UST**<br>DSμP (CL-MD4314)<br>SAFE (CL-MD1724) |
| International (including U.S.) | **CL-MD1414UN**<br>DSμP (CL-MD4014)<br>SAFE (CL-MD1724) | **CL-MD1414UNP**<br>DSμP (CL-MD4814)<br>SAFE (CL-MD1724) | **CL-MD1414UNT**<br>DSμP (CL-MD4514)<br>SAFE (CL-MD1724) |

### *Device Set Information*



### *Device Information*

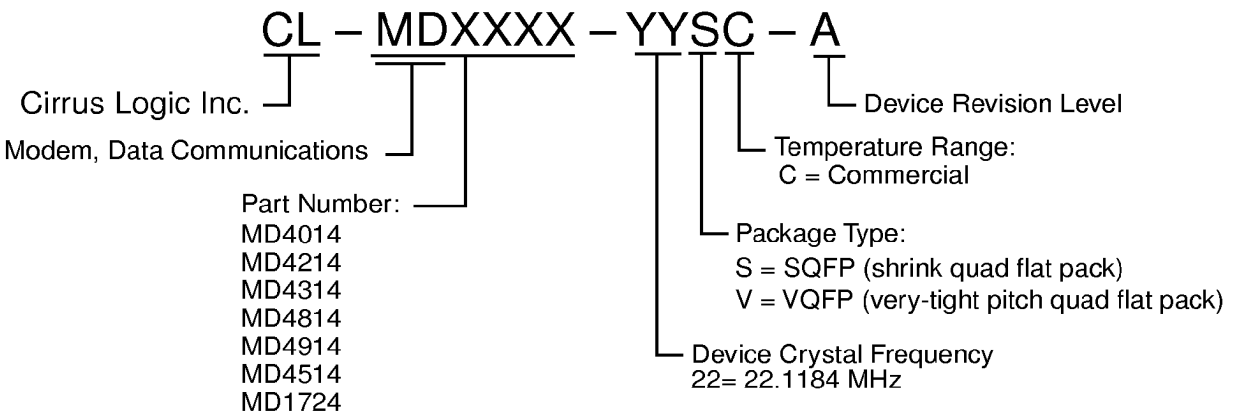



Table 9-1 below is a list of the Cirrus Logic family of modem products that are available now. A brief description of each device set is provided.

**Table 9-1. Cirrus Logic Modem Products**

| Number of Devices | Device Set | Features |
|---|---|---|
| 3 | CL-MD1414ECT | High-speed modem that provides 14,400-bps data mode, and 14,400-bps fax and voice modes (with two built-in DTE interfaces — serial RS232 and parallel 16C450A/16C550-compatible interface registers that can be connected directly to an ISA bus). Error correction (V.42 and MNP 2–4), data compression (V.42 bis and MNP 5), a microphone interface, and Telephone-Emulation mode are also provided. |
| | CL-MD1414ECP | Same features as the CL-MD1414ECT, except built-in PC card interface with 16C450/16C550-compatible registers, (that is, it does not support parallel ISA bus and serial RS232 host interfaces). |

**Table 9-1. Cirrus Logic Modem Products** *(cont.)*

| | | |
|---|---|---|
| 2 | CL-MD1414US | Same features as CL-MD1414ECT plus flash memory interface for downloadable firmware upgrades, cellular ready, voice mode DMA, new voice sample rates (4.8K, 7.2K, 11.025K, and 22.050K), new voice compression formats (8-bit and 16-bit linear, and ADPCM with timing marks), Caller ID, and message forwarding features. |
| | CL-MD1414USP | Same features as the CL-MD1414US, except built-in PC card interface with 16C450/16C550-compatible registers, (that is, it does not support parallel ISA bus and serial RS232 host interfaces). |
| | CL-MD1414UST | Same features as the CL-1414US, but adds a Windows® 95-compatible plug-and-play interface. |
| | CL-MD1414UN | Same features as CL-MD1414US plus international functions. |
| | CL-MD1414UNP | Same features as the CL-MD1414UN, except built-in PC card interface with 16C450/16C550-compatible registers (that is, it does not support parallel ISA bus and serial RS232 host interfaces). |
| | CL-MD1414UNT | Same features as the CL-MD1414UN, but adds a Windows® 95-compatible plug-and-play interface. |

# 10. SCHEMATICS

This section provides several modem design examples. The key segments for a typical modem are divided into separate figures or circuits. These individual circuits may then be combined to form a modem for a specific application. Contact Cirrus Logic for current schematics. For example,

1) An internal modem with local record/playback: Figures 10-1a, 10-2, 10-3b, and 10-5.

2) A single internal modem board that supports jumpered COM ports, software programmable COM ports, and plug-and-play mode with local record/playback: Figures 10-1c, 10-2, 10-3b, and 10-5.

3) A box modem with local record/playback: Figures 10-7, 10-2, 10-3b, and 10-5.

4) PC card modem with handset for local record/playback: Figures 10-8, 10-2, and 10-9.

**NOTE:** Since the DSµP device pin diagram for the CL-MD1414UXX and the CL-MD9624XX are identical except for one pin, a single board can be designed to support both device sets.

Following is a list of the circuits provided:

Figure 10-1a. Parallel host interface and DSµP-SAFE interface (jumpered COM ports)

Figure 10-1b. Parallel host interface and DSµP-SAFE interface (plug and play)

Figure 10-2. Flash ROM, SRAM, and Caller ID interface schematics

Figure 10-3a. DAA design for data/fax/voice without local voice recording

Figure 10-3b. DAA design for data/fax/voice with local phone powered by modem (allows local record/playback)

Figure 10-4. A/A1 circuit — not recommended for U.S. home market

Figure 10-5a. Direct-connect speaker circuit

Figure 10-5b. Amplified speaker circuit

Figure 10-6. Microphone circuit

Figure 10-7. Serial host interface (RS-232); refer to Figure 10-1 for DSµP-SAFE interface

Figure 10-8. PC card host interface with internal CIS

Figure 10-9. PC card DAA with external handset for local playback and record