NEC
NEC Electronics Inc.

μPD42280
NTSC and PAL Field Buffer

T-77-07-13

Description

The μPD42280 is a 262,224-word by 8-bit dual-port field buffer fabricated with a silicon-gate CMOS process. The device can execute synchronous and asynchronous serial write and serial read operation at a 33.3-MHz clock frequency. In asynchronous mode, the device can be used as a data storage (communication) buffer, a time axis converter, and a digital delay line of up to 262,224 bits (200 bits minimum at any frequency). In synchronous mode, the minimum delay is 3 bits at any frequency when used as a fixed-length delay line.

Applications include NTSC/PAL TV/VCR systems, video processing, digital plain paper copiers, and systems requiring serial data streams like printers, optical scanners, and local area networks.

The serial write and read function simplifies interframe luminance (Y) and chrominance (C) separation, interfield noise reduction, frame synchronization, and time base correction. Refreshing is performed automatically by an internal circuit, so the device operates like a static RAM.

All inputs and outputs, including clocks, are TTL compatible. The plastic package is a 28-pin SOP (450-mil) or ZIP (400-mil), and operation is guaranteed in an ambient temperature range of −20 to +70°C.

Features

- 262,224-word x 8-bit organization
- Dual-port operation
- Asynchronous, simultaneous reading/writing
- Output enable function
- Variable field length
  - — 200 to 262,224 bits as an elastic (asynchronous) delay line
  - — 3 to 262,224 bits as a fixed-length (full synchronous) delay line
- One-cycle address pointer reset and immediate write/read access function
- Automatic refreshing (full static interface)
- Direct connection with NEC line buffers (μPD42101/42102/42505)
- 4M-bit DRAM COMS technology
- Full TTL-compatible inputs, outputs, and clocks
- Three-state outputs
- Single +5-volt power supply
- On-chip substrate bias generator
- 28-pin SOP (450-mil) and ZIP (400-mil) plastic packaging

Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42280GU-30	25 ns	30 ns	28-pin plastic SOP
GU-40	30 ns	40 ns	
GU-60	40 ns	60 ns	
μPD42280V-30	25 ns	30 ns	28-pin plastic ZIP
V-40	30 ns	40 ns	
V-60	40 ns	60 ns	

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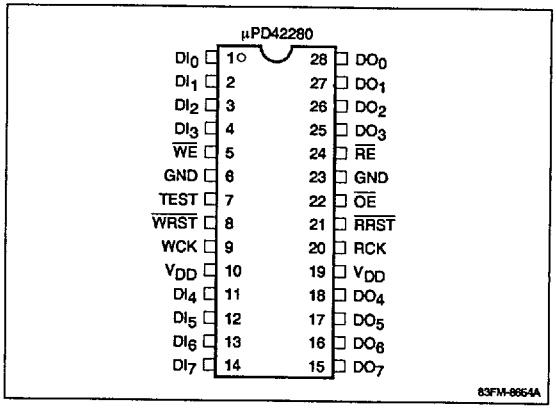
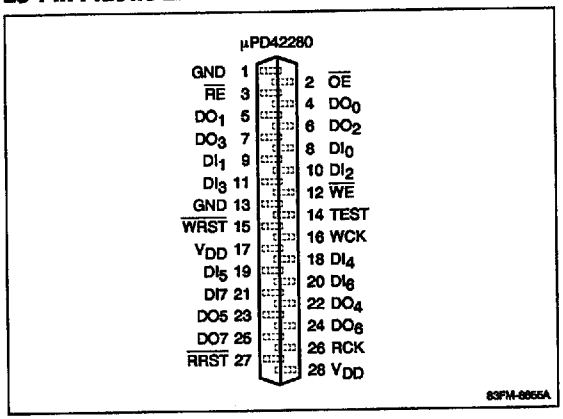
Pin Configurations

28-Pin Plastic SOP



Pin Configurations

28-Pin Plastic ZIP



Pin Identification

Symbol	Function
DI_0 - DI_7	Write data inputs
DO_0 - DO_7	Read data outputs
$\overline{OE}$	Output enable input
RCK	Read clock input
$\overline{RE}$	Read enable input
$\overline{RRST}$	Read address reset input
WCK	Write clock input
$\overline{WE}$	Write enable input
$\overline{WRST}$	Write address reset input
TEST	Test pin (connect to GND in system)
GND	Ground
V_{DD}	+5-volt power supply

PIN FUNCTIONS

DI_0 - DI_7 (Data Inputs)

These pins function as write data inputs; for example, for $4f_{SC}$ composite color or brightness signals.

DO_0 - DO_7 (Data Outputs)

These pins are three-state read outputs.

$\overline{OE}$ (Output Enable Input)

This signal controls read data output. When $\overline{OE}$ is low, read data is output on DO_0 - DO_7. When $\overline{OE}$ is high, DO_0 - DO_7 are in a state of high impedance. The read address pointer is incremented by RCK, regardless of the signal level of $\overline{OE}$. The state of $\overline{OE}$ is strobed by the rising edge of RCK.

RCK (Read Clock Input)

All read cycles are executed synchronously with RCK. The states of both $\overline{RRST}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 262,223 to 0 and begin increasing again.

$\overline{RE}$ (Read Enable Input)

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

$\overline{RRST}$ (Read Address Reset Input)

This signal is strobed by the rising edge of RCK and resets the internal read address to 0.

WCK (Write Clock Input)

All write cycles are executed synchronously with WCK. The states of both $\overline{WRST}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 262,223 to 0 and begin increasing again.

$\overline{WE}$ (Write Enable Input)

This input controls write operation. If $\overline{WE}$ is low, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to the register and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{WRST}$ (Write Address Reset Input)

Bringing this signal low resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

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OPERATION

Reset

The μPD42280 requires initialization of internal circuits using the $\overline{WRST}$/$\overline{RRST}$ reset signals before starting operation (after power on). A reset cycle can be executed at any time and does not depend on the state of $\overline{WE}$, $\overline{RE}$, and $\overline{OE}$. However, $\overline{WRST}$ and $\overline{RRST}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

After the reset cycle, write and read operation can be started immediately.

Write

Write cycles are executed in synchronization with WCK as $\overline{WE}$ is held low. In the write cycle operation, the internal write address pointer is automatically incremented. When $\overline{WE}$ is high at the rising edge of WCK, write operation is disabled and the internal write address pointer does not increment with successive write clocks.

Write data must satisfy setup and hold times as specified from the rising edge of WCK.

After the reset operation, bits are input sequentially into an 80 x 8-bit SRAM buffer. Then, new bits are input sequentially into one of the two halves of the 128 x 8-bit data register before being transfered to the storage array. The register data is transferred into the array in blocks of 64 x 8 bits.

Read

Read cycles are executed in synchronization with RCK while $\overline{RE}$ and $\overline{OE}$ are held low.

In the read cycle operation, the internal read address pointer is automatically incremented as $\overline{RE}$ is held low. When $\overline{RE}$ is high at the rising edge of RCK, the internal read address pointer does not increment with successive read clocks.

The $\overline{OE}$ input controls the output state of DO_0 - DO_7 pins. When $\overline{OE}$ is low at the rising edge of RCK, the DO_0 - DO_7 pins are low-impedance state. When $\overline{OE}$ is high at the rising edge of RCK, the DO_0 - DO_7 pins are high-impedance state with successive read clocks.

The access time of a read cycle is measured from the rising edge of RCK by t_{AC} for an access of any internal read address. Stored data is read nondestructively; data can be read repeatedly at any time (cell data hold time is endless).

New data written to a particular internal address is available for reading after 200 write cycles maximum. This value depends on write cycle time and the write/read operation control method.

DIGITAL DELAY LINE

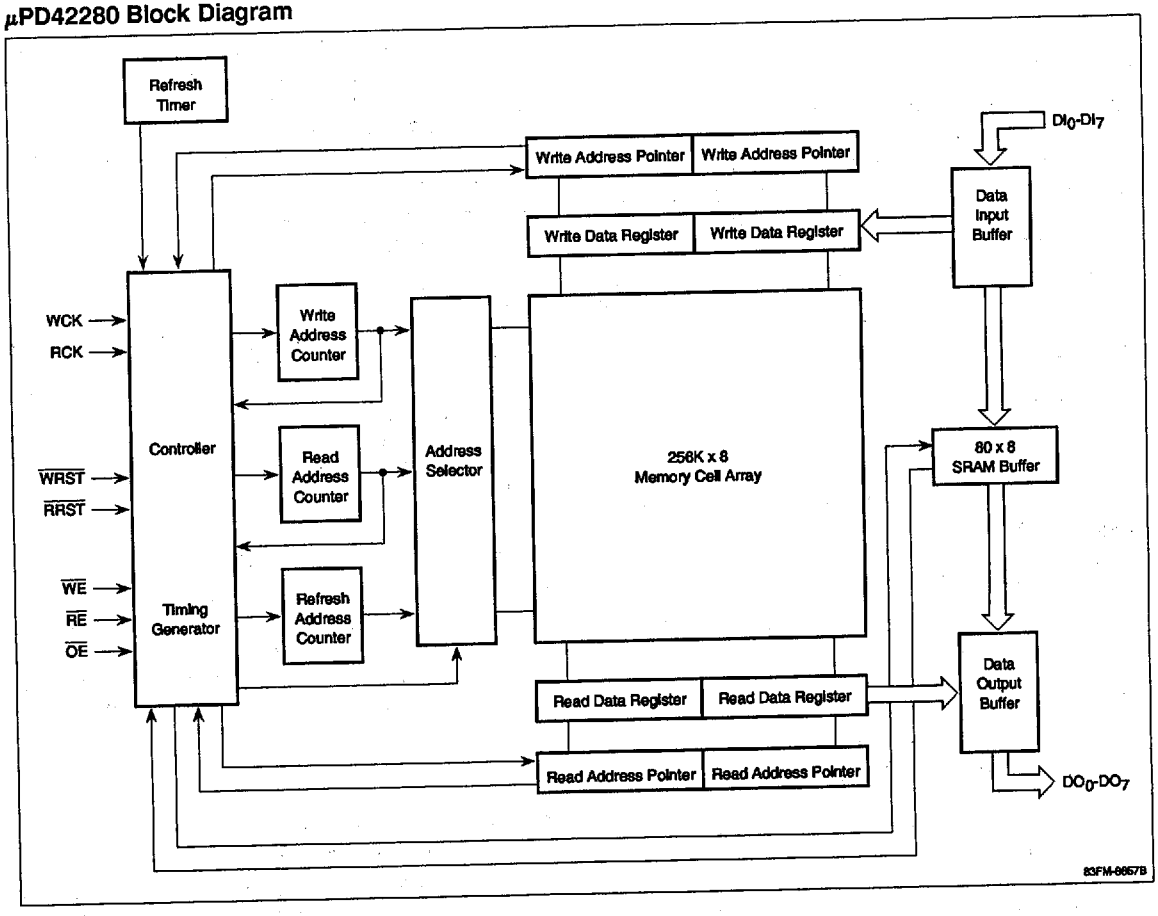
The μPD42280 can be easily used as a digital delay line of 262,224 bits or less. The two operating modes are elastic (asynchronous) and fixed-length (full-synchronous).

Elastic (Asynchronous) Delay Line

Delay length of the elastic delay line is from 200 bits minimum (at any frequency) to 262,224 bits maximum. The minimum delay length does not depend on clock frequency.

Figures 1 and 2 show control timings for the elastic delay line. Write and read cycles are synchronized to

μPD42280 Block Diagram



their respective WCK/RCK inputs and executed individually. The difference (n) between the internal write address pointer and the internal read address pointer must fall between 199 and 262,223.

Fixed-Length (Full-Synchronous) Delay Line

The length of the delay line is specified as 3 to 262,224 bits. It does not depend on clock frequency

Figure 3 shows control timing for the fixed-length delay line. The same signal is used for WCK and RCK so that $\overline{WRST}$ and $\overline{RRST}$ are controlled together. The data, written after a reset signal, is read out after the next reset signal in the order it was written. This interval determines the delay length. For example, if the reset signal is input every 239,330 (263 x 910) cycles, the delay length is 239,330 cycles.

Figure 1. Elastic Delay Line No. 1

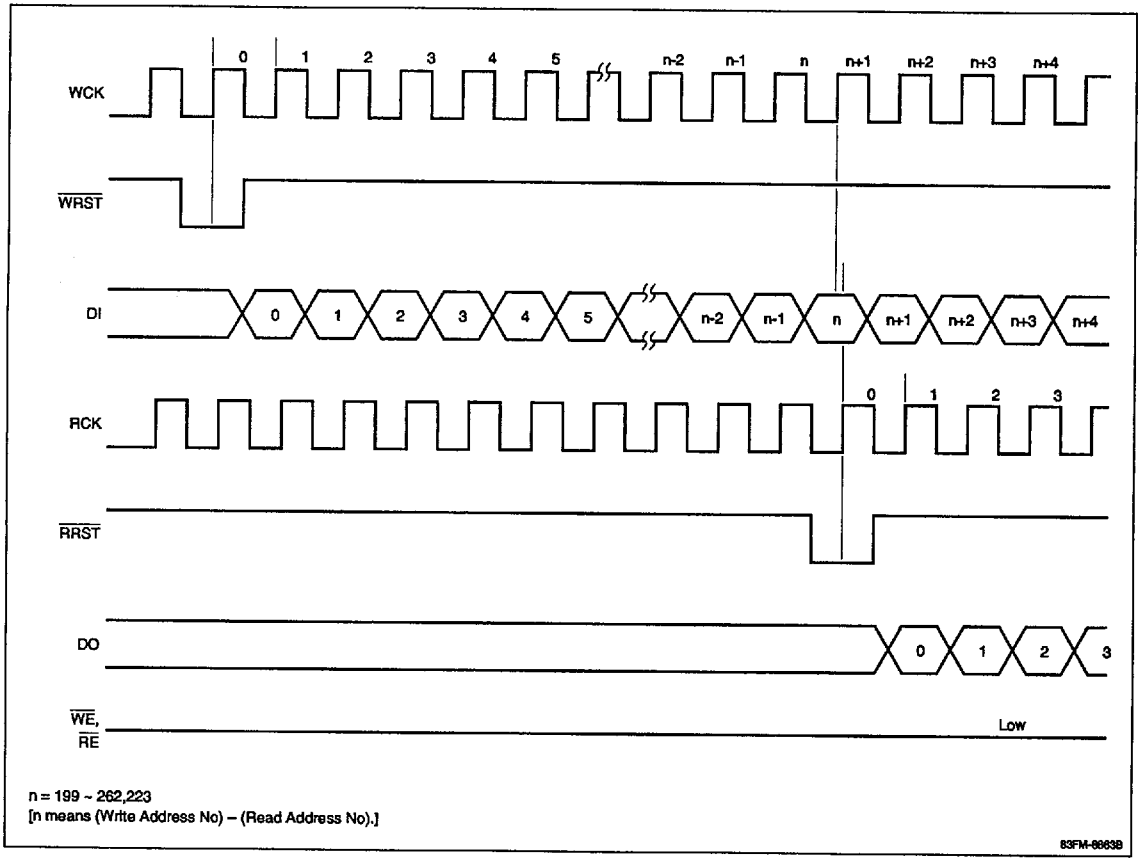
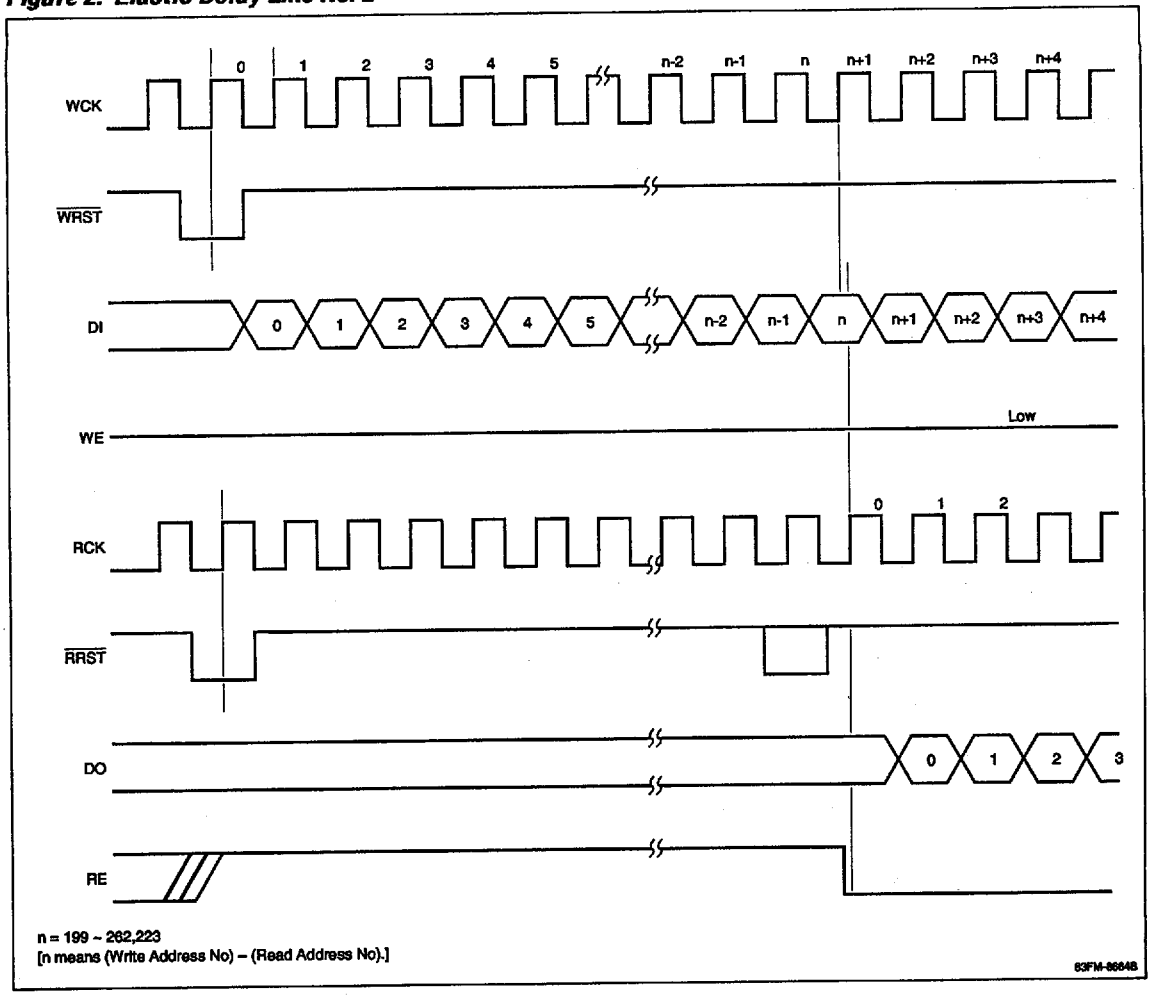


Figure 2. Elastic Delay Line No. 2



n = 199 ~ 262,223
[n means (Write Address No) – (Read Address No).]

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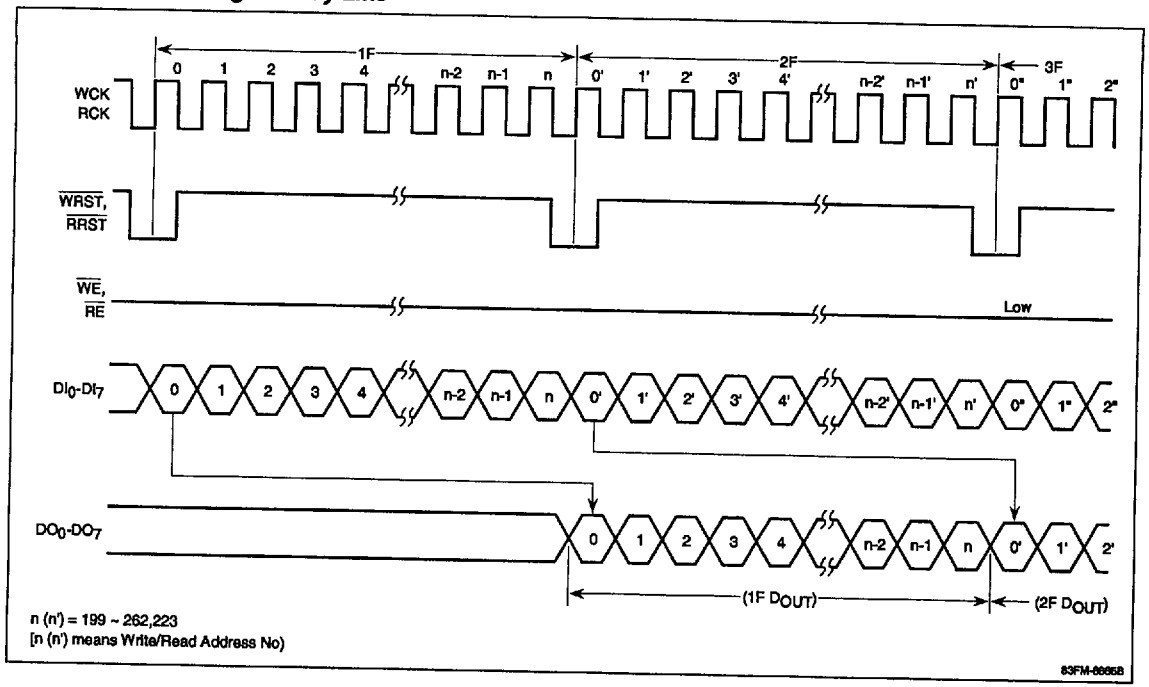
Figure 3. Fixed-Length Delay Line



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SPECIFICATIONS

Absolute Maximum Ratings

Supply voltage, V_{DD}	−1.0 to +7.0 V
Voltage on any input pin, V_I	−1.0 to V_{DD} + 0.5 V (+7.0 V max)
Voltage on any output pin, V_O	−1.0 to V_{DD} + 0.5 V (+7.0 V max)
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{DD} + 0.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	−20		+70	°C

Capacitance

T_A = 25°C; V_{DD} = +5.0 V ±10%; f = 1 MHz

Parameter †	Symbol	Min	Max	Unit	Pins Under Test
Input capacitance	C_I		5	pF	$\overline{WE}$, $\overline{RE}$, $\overline{OE}$ WCK, RCK, $\overline{WRST}$, $\overline{RRST}$, DI_0 - DI_7
Output capacitance	C_O		7	pF	DO_0 - DO_7

† Capacitance is sampled and not 100% tested.

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DC Characteristics

T_A = −20 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Operating current	I_{CC1}		50	90	mA	t_{WCK}, t_{RCK} = 30 ns
Standby current	I_{CCS}		4	10	mA	WCK, RCK = V_{IL}
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{DD}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_O disabled; V_O = 0 to V_{DD}
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA

* Voltages are referenced to GND.

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD42280-30		μPD42280-40		μPD42280-60			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Access time	t_{AC}		25		30		40	ns	
Data-in hold time	t_{DH}	3		3		3		ns	
Data-in setup time	t_{DS}	7		10		12		ns	
Output disable time	t_{HZ}	5	25	5	30	5	40	ns	(Note 4)
Output active time	t_{LZ}	5	25	5	30	5	40	ns	(Note 4)
Output enable hold time	t_{OEH}	3		3		3		ns	(Note 9)
Output enable high delay from RCK	t_{OEN1}	3		3		3		ns	(Note 10)
Output enable low delay from RCK	t_{OEN2}	7		10		12		ns	(Note 10)
Output enable setup time	t_{OES}	7		10		12		ns	(Note 9)
Output hold time	t_{OH}	5		5		5		ns	
Read clock cycle time	t_{RCK}	30		40		60		ns	
RCK precharge time	t_{RCP}	12		14		20		ns	
RCK pulse width	t_{RCW}	12		14		20		ns	
Read enable hold time	t_{REH}	3		3		3		ns	(Note 7)
Read enable high delay from RCK	t_{REN1}	3		3		3		ns	(Note 8)
Read enable low delay to RCK	t_{REN2}	7		10		12		ns	(Note 8)
Read enable setup time	t_{RES}	7		10		12		ns	(Note 7)
Read disable pulse width	t_{REW}	0		0		0		ns	
Reset active hold time	t_{RH}	3		3		3		ns	(Note 5)
Reset inactive setup time	t_{RN1}	3		3		3		ns	(Note 6)
Reset inactive hold time	t_{RN2}	7		10		12		ns	(Note 6)
Read reset time	t_{RRST}	0		0		0		ns	
Reset active setup time	t_{RS}	7		10		12		ns	(Note 5)
Transition time	t_T	3	35	3	35	3	35	ns	
Write clock cycle time	t_{WCK}	30		40		60		ns	
WCK precharge time	t_{WCP}	12		14		20		ns	
WCK pulse width	t_{WCW}	12		14		20		ns	
Write enable hold time	t_{WEH}	3		3		3		ns	(Note 7)

AC Characteristics (cont)

Parameter	Symbol	μPD42280-30 Min	μPD42280-30 Max	μPD42280-40 Min	μPD42280-40 Max	μPD42280-60 Min	μPD42280-60 Max	Unit	Test Conditions
Write enable high delay from WCK	t_{WEN1}	3		3		3		ns	(Note 8)
Write enable low delay to WCK	t_{WEN2}	7		10		12		ns	(Note 8)
Write enable setup time	t_{WES}	7		10		12		ns	(Note 7)
Write disable pulse width	t_{WEW}	0		0		0		ns	
Write reset time	t_{WRST}	0		0		0		ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = 0.4 to 2.4 V. Transition times are measured between 2.4 and 0.4 V. See figure 4.

(3) Input timing reference levels = 1.5 V. Output timing reference levels are 0.8 and 2.0 V. See figure 4.

(4) This delay is measured at 200 mV from the steady-state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(6) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(7) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(8) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(9) If either t_{OES} or t_{OEH} is less than the specified value, output disable operations are not guaranteed.

(10) If either t_{OEN1} or t_{OEN2} is less than the specified value, internal output disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(11) To read new data just written, the write address must precede the read address by at least 200 addresses.

(12) During a reset operation, the levels of $\overline{WE}$ and $\overline{RE}$ are "dont care."

(13) Addresses 0-79 (80 words x 8 bits) are stored in an SRAM buffer. Addresses 80-262,223 are stored in dynamic cells and transferred in 64 x 8-bit increments. The "143" in the equation below comes from 79 + 64 = 143.

When $\overline{WRST}$ goes low (active) at address n, the write data from address n to address m is not guaranteed because partial data stored in the write registers (< 64 bits) will not be transferred to the DRAM array.

(13 cont)

$$m = 143 + \frac{n - 80}{64} \times 64$$

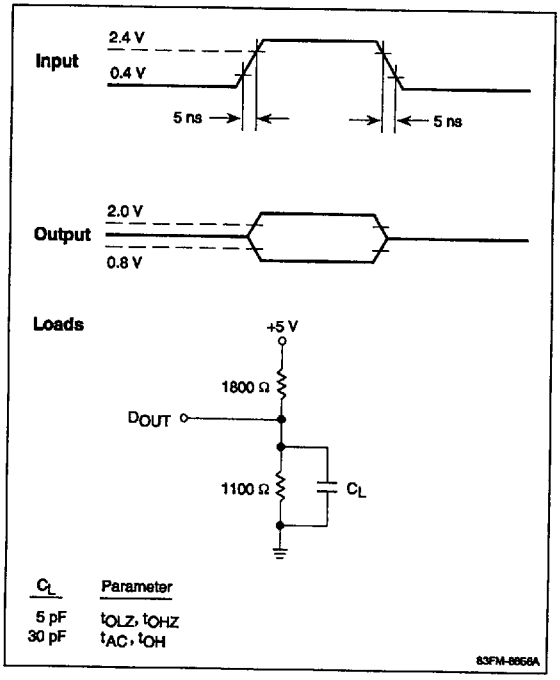
$\frac{n-80}{64}$ means the nearest whole number

For example, if n = 280, then $\frac{n-80}{64} = 3.125 = 3$

$$m = 143 + (3 \times 64)$$
$$= 143 + 192$$
$$= 335$$

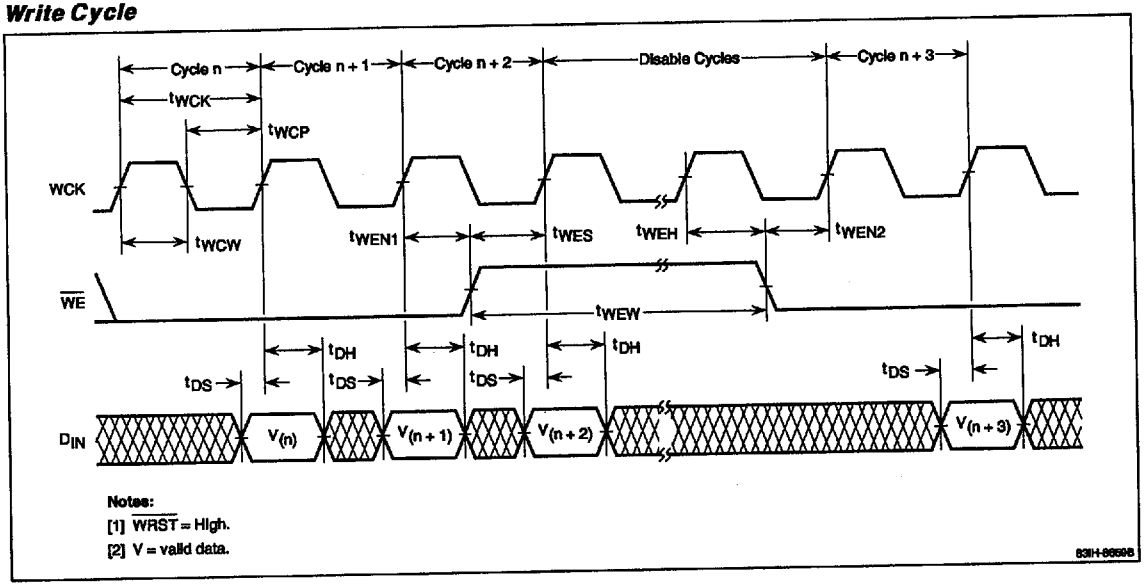
So, data transfer from address 280 to address 335 is not guaranteed.

Figure 4. AC Test Conditions



Timing Waveforms

Write Cycle



Notes:
[1] $\overline{WRST}$ = High.
[2] V = valid data.

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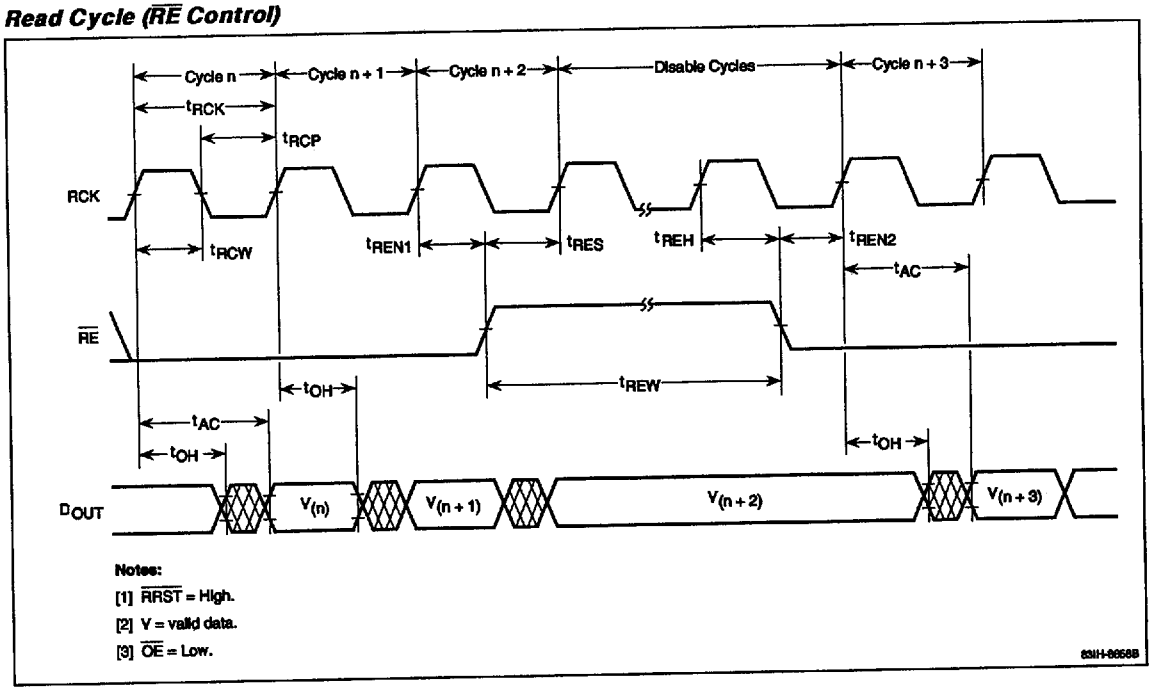
Read Cycle ($\overline{RE}$ Control)



Notes:
[1] $\overline{RRST}$ = High.
[2] V = valid data.
[3] $\overline{OE}$ = Low.

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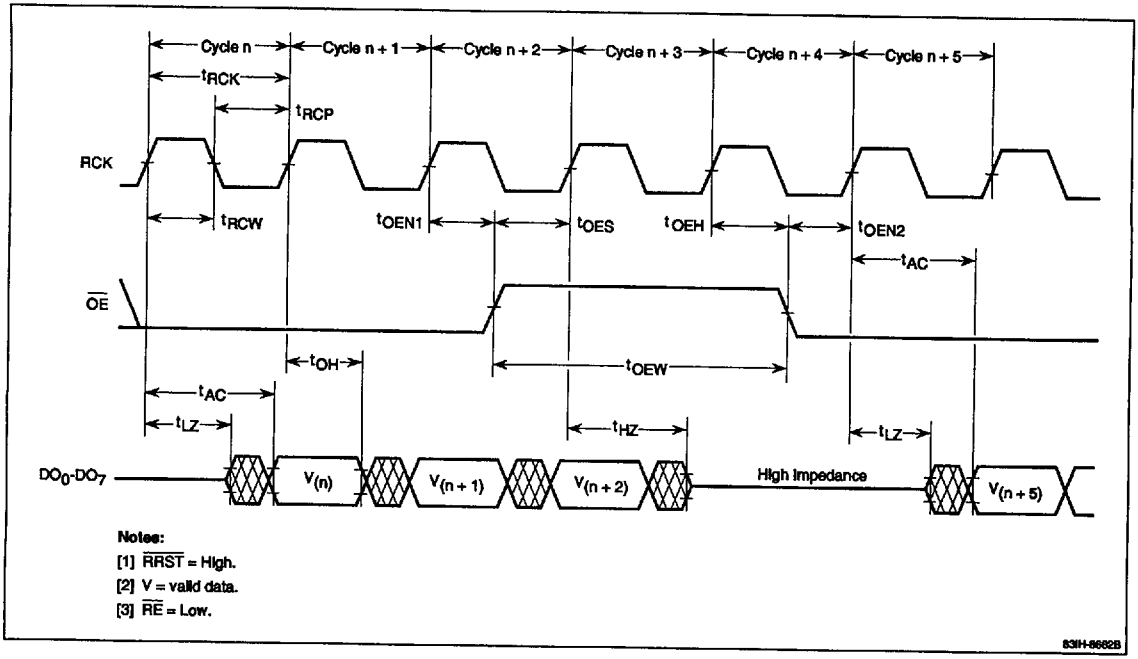
Timing Waveforms (cont)

Read Cycle ($\overline{OE}$ Control)



Notes:
[1] $\overline{RRST}$ = High.
[2] V = valid data.
[3] $\overline{RE}$ = Low.

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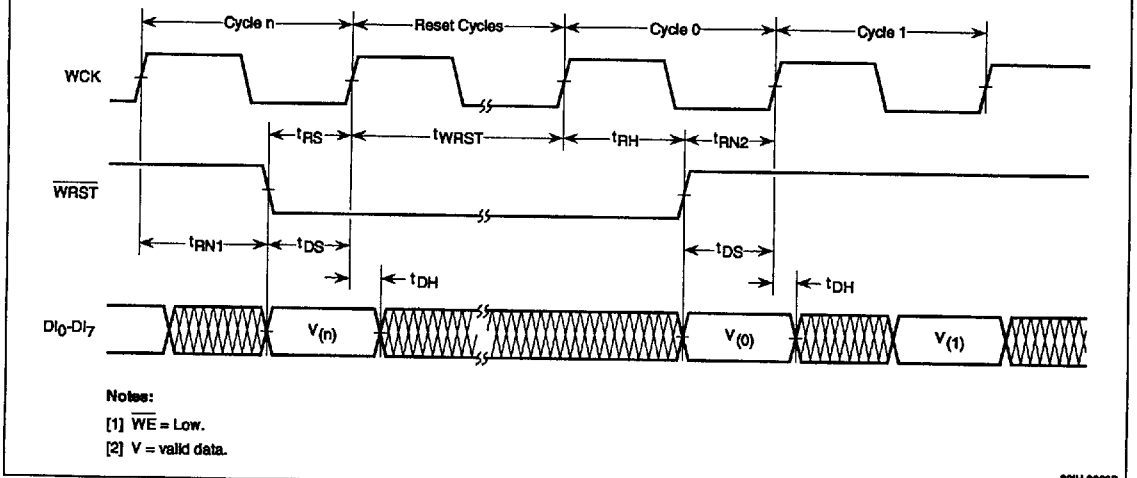
Write Reset Cycle



Notes:
[1] $\overline{WE}$ = Low.
[2] V = valid data.

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Timing Waveforms (cont)

Read Reset Cycle