SM5956A

6-channel Asynchronous Sample Rate Converter

OVERVIEW

The SM5956A is a digital audio signal, asynchronous sample rate converter LSI. It reads 6-channel 16/20/24-bit word length input data, and 16/20/24-bit word length output data. It also features a built-in digital deemphasis filter, direct muting and digital audio interface output.

FEATURES

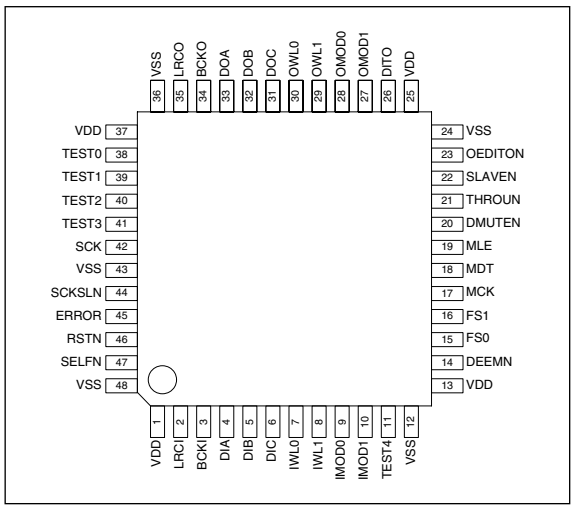
Functions

- L/R 6-channel processing
  (2-channel stereo, 3-system processing)
- Input sample rate range: 10kHz to 200kHz
- Output sample rate range: 30kHz to 50kHz
- Operating sample rate conversion ratio (fso/fsi)*1
  - 0.45 to 4.41 (SCKSLN = L, 512fso operation)
  - 0.225 to 4.41 (SCKSLN = H, 768fso operation)

  *1: fsi = input sample rate
  fso = output sample rate
- Asynchronous input timing and output timing clock inputs
- System clock input
  - Input system clock: 1fsi (LRCI)
  - Output-system clock: 512fso/768fso (input on SCK)
- Deemphasis filter function
  - IIR filter structure
  - 44.1kHz, 48kHz, 32kHz input sample rate fsi compatible
- Direct mute function
- Through mode
  - Input data passed directly to the outputs
- Digital audio interface output
  - DIA input data undergoes sample rate conversion and is output biphase mark encoded
- Output data clocks (LRCO, BCKO)
  - LRCO rate: 1fso
  - BCKO rate: 64fso (SCKSLN = L, 512fso operation)
    48fso (SCKSLN = H, 768fso operation)
  - Slave mode: Data is output at a rate dictated by an externally input signal
  - Master mode: Sample rate is generated internally from the output-system clock, and supplied as an output
- MCU interface
  - 3-wire serial interface
- 5V tolerant inputs for direct connection to 5V devices
- 3.3V single supply
- Package: 48-pin QFP

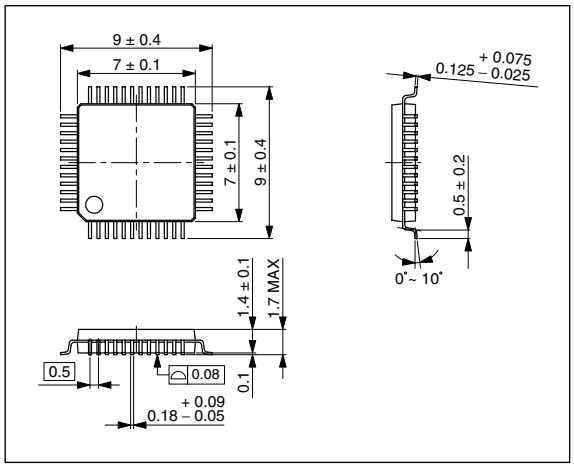
PINOUT

(Top view)



PACKAGE DIMENSIONS

(Unit: mm)



Note. Dimensions without tolerance are reference values.

ORDERING INFORMATION

Device	Package
SM5956AF	48-pin QFP

FEATURES

Interfaces

- Input data format
  - 2s-complement, MSB-first, L/R alternating serial IIS/non-IIS formats

Format	IMOD1	IMOD0
IIS	L	L
MSB-first left-justified	L	H
MSB-first right-justified	H	L
MSB-first right-justified	H	H

- Input word length
  - 16/20/24-bit

Input word length	IWL1	IWL0
16 bits	L	L
20 bits	L	H
24 bits	H	L
24 bits	H	H

- Output data format
  - 2s-complement, MSB-first, L/R alternating serial IIS/non-IIS format
  - Continuous bit clock (64fso/48fso)

Format	OMOD1	OMOD0
IIS	L	L
MSB-first left-justified	L	H
MSB-first right-justified	H	L
MSB-first right-justified	H	H

- Output word length
  - 16/20/24-bit

Output word length	OWL1	OWL0
16 bits	L	L
20 bits	L	H
24 bits	H	L
24 bits	H	H

Structure

- Silicon-gate CMOS process

Applications

- Sample rate conversion between digital audio equipment (AV amplifiers, CD-R/RW, MD, DVC etc.)
- Sample rate conversion in commercial recording/editing equipment

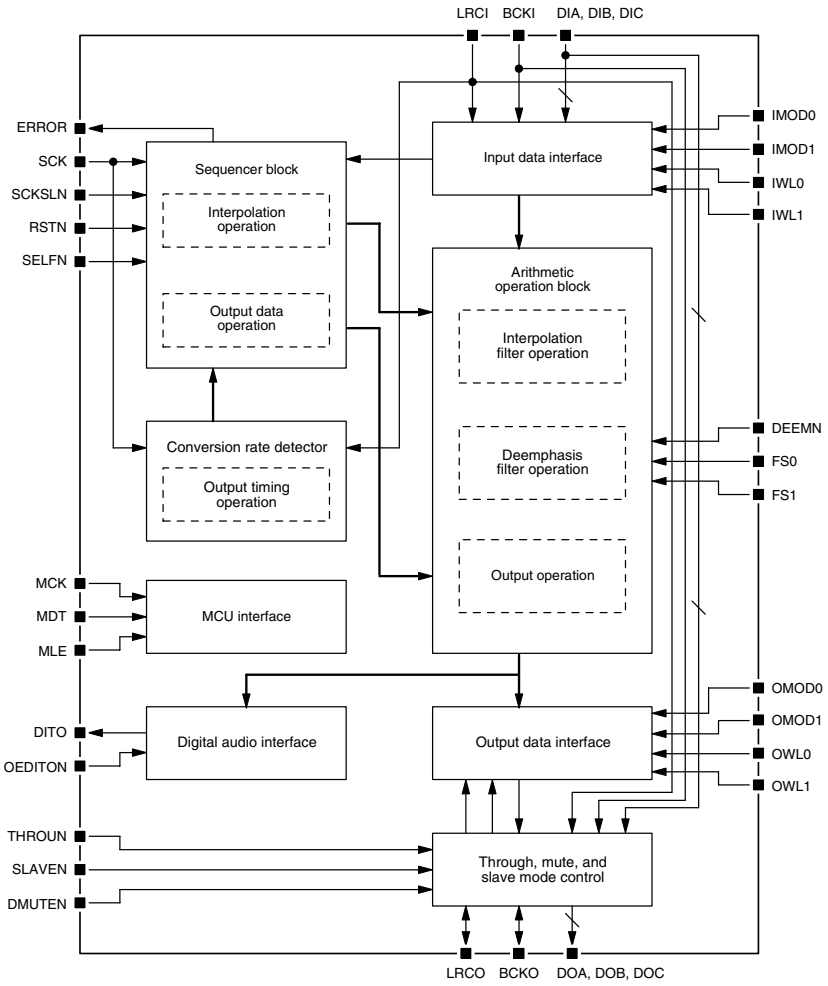
Converter Performance

- Internal data word length: 20 bits
- Deemphasis filter characteristics (IIR filter)
  - Gain deviation from ideal filter characteristic: ± 0.03dB
- Anti-aliasing LPF characteristics
  - Passband ripple: ± 0.0001dB
  - Stopband attenuation: > 98dB
- Converter noise levels
  - Internal calculation noise: ≤ –96dB
  - Output round-off noise:
    16-bit output mode : –98dB
    20-bit output mode : –122dB
    24-bit output mode : –146dB

Combined theoretical S/N

Output word length	Input word length		
	16 bits	20 bits	24 bits
16 bits	–92.3dB	–94.0dB	–94.0dB
20 bits	–94.0dB	–96.0dB	–96.0dB
24 bits	–94.1dB	–96.1dB	–96.2dB

BLOCK DIAGRAM



PIN DESCRIPTION

No.	Name	I/O[1]	Function	HIGH	LOW
1	VDD	–	VDD supply (3.3V)	–	–
2	LRCI	Is	Sample rate clock input (fsi)	–	–
3	BCKI	Is	Bit clock input (32fsi to 64fsi)	–	–
4	DIA	Is	Data input A	–	–
5	DIB	Is	Data input B	–	–
6	DIC	Is	Data input C	–	–
7	IWL0	I	Input word length select 0	See “Input Interface Settings”	
8	IWL1	I	Input word length select 1		
9	IMOD0	I	Input format select 0		
10	IMOD1	I	Input format select 1		
11	TEST4	Id	Test input	Test	Normal
12	VSS	–	Ground (0V)	–	–
13	VDD	–	VDD supply (3.3V)	–	–

No.	Name	I/O[1]	Function	HIGH	LOW
14	DEEMN	I	Deemphasis select	OFF	ON
15	FS0	I	Deemphasis frequency select 0	See “Sample Rate Conversion”	
16	FS1	I	Deemphasis frequency select 1		
17	MCK	Is	MCU interface clock input	–	–
18	MDT	Is	MCU interface data input	–	–
19	MLE	Is	MCU interface latch enable input	–	–
20	DMUTEN	Id	Direct mute select	Output	Mute
21	THROUN	Id	Through-mode select	SRC	Through
22	SLAVEN	Id	Slave-mode select	Master	Slave
23	OEDITON	Id	DIT output enable select	L	Output
24	VSS	–	Ground (0V)	–	–
25	VDD	–	VDD supply (3.3V)	–	–
26	DITO	O	Digital audio interface output	–	–
27	OMOD1	I	Output format select 1	See “Output Interface Settings”	
28	OMOD0	I	Output format select 0		
29	OWL1	I	Output word length select 1		
30	OWL0	I	Output word length select 0		
31	DOC	O	Data output C	–	–
32	DOB	O	Data output B	–	–
33	DOA	O	Data output A	–	–
34	BCKO	I/O	Bit clock input/output (48fso/64fso)	–	–
35	LRCO	I/O	Sample rate clock input/output (fso)	–	–
36	VSS	–	Ground (0V)	–	–
37	VDD	–	VDD supply (3.3V)	–	–
38	TEST0	Id	Test input	Test	Normal
39	TEST1	Id	Test input	Test	Normal
40	TEST2	Id	Test input	Test	Normal
41	TEST3	Id	Test input	Test	Normal
42	SCK	I	Output-system clock input (512fso/768fso)	–	–
43	VSS	–	Ground (0V)	–	–
44	SCKSLN	Id	Output-system clock select	768fso	512fso
45	ERROR	O	Input error detector output	–	–
46	RSTN	Id	Reset input	–	Reset
47	SELFN	Id	Reset mode select	External	Automatic
48	VSS	–	Ground (0V)	–	–

1. I = input, O = output, Id = input with pull-down, Is = Schmitt input, – = supply

ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V, VDD pins = V_{DD}

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 to 4.6	V
Input voltage	V_I	–0.3 to 5.5	V
Output voltage	V_O	–0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	–55 to 125	°C
Power dissipation	P_W	700	mW

Note. Ratings also apply when power is turned ON/OFF.

RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V, VDD pins = V_{DD}

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating temperature	T_{OPR}	–40	25	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{SS} = 0V, V_{DD} = 3.0 to 3.6V, Ta = –40 to 85°C

Parameter	Pin	Symbol	Condition	Rating			Unit
				min	typ	max	
Current consumption	VDD	I_{DD}	(*A)	–	75	90	mA
			(*B)	–	100	125	
Input voltage	(*1)(*2) (*3)(*5)	V_{IH}		2.0	–	5.5	V
		V_{IL}		0	–	0.7	V
			BCKO, LRCO only	0	–	0.4	V
Output voltage	(*4)(*5)	V_{OH}	I_{OH} = –2.0mA	2.4	–	V_{DD}	V
		V_{OL}	I_{OL} = 2.0mA	0	–	0.4	V
Input leakage current	(*1)(*2) (*5)	I_{LH}	V_{IN} = V_{DD}	–1.0	–	1.0	µA
		I_{LL}	V_{IN} = 0V	–1.0	–	1.0	µA
Input current	(*3)	I_{IH}	V_{IN} = V_{DD}	12.5	33.0	90.0	µA
		I_{IL}	V_{IN} = 0V	–1.0	–	1.0	µA
Pull-down resistance	(*3)	R_{PD}		40	100	240	kΩ
Input load capacity	(*1)(*2) (*3)(*5)	C_{LDI}		–	10	–	pF

(*A) All outputs no load, system clock frequency F_{SCK} = 24.576MHz, input word clock frequency F_{LRCI} = 48kHz, SCKSLN = L (512fso), supply voltage V_{DD} = 3.3V

(*B) All outputs no load, system clock frequency F_{SCK} = 36.864MHz, input word clock frequency F_{LRCI} = 48kHz, SCKSLN = H (768fso), supply voltage V_{DD} = 3.3V

Note. See “Pin Classification” below for description of pins.

Pin classification

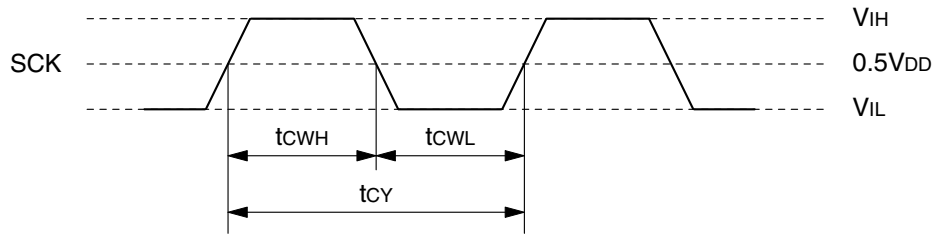
Symbol	Type	Names
(*1)	Inputs	SCK, IMOD0, IMOD1, IWL0, IWL1, DEEMN, FS0, FS1, OMOD0, OMOD1, OWL0, OWL1
(*2)	Schmitt inputs	LRCI, BCKI, DIA, DIB, DIC, MCK, MDT, MLE
(*3)	Pull-down inputs	TEST0, TEST1, TEST2, TEST3, TEST4, DMUTEN, THROUN, SLAVEN, OEDITON, RSTN, SELFN, SCKSLN
(*4)	Outputs	DOA, DOB, DOC, DITO, ERROR
(*5)	Input/Outputs	BCKO, LRCO

Note. The input and input/output pins are all 5V tolerant. The maximum input voltage that can be applied to these pins are 5.5V, if supply voltage is within the recommended operating voltage. If the input voltage is between 5.5V and VDD which is smaller than the recommended operating voltage, the device doesn’t breakdown itself, but it maybe generate reverse current from the input pins to the supply voltage (VDD). Although input/output pins in input mode can accept 5.5V as the maximum input voltage, the maximum output voltage in output mode is VDD level. It is forbidden to add more voltage than VDD to output mode bidirectional pins (external pull-up or other means).

AC Characteristics

Output-system clock (SCK input)

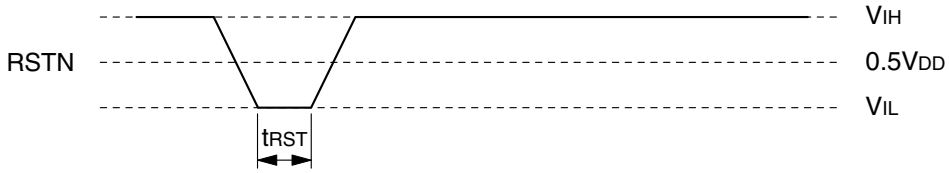
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock pulse cycle time	t_{CY}	SCKSLN = L	39.0	–	65.1	ns
		SCKSLN = H	26.0	–	43.4	
HIGH-level clock pulsewidth	t_{CWH}	SCKSLN = L	15.6	–	39.1	ns
		SCKSLN = H	10.4	–	26.0	
LOW-level clock pulsewidth	t_{CWL}	SCKSLN = L	15.6	–	39.1	ns
		SCKSLN = H	10.4	–	26.0	
Clock pulse duty			40	–	60	%



Reset input (RSTN input)

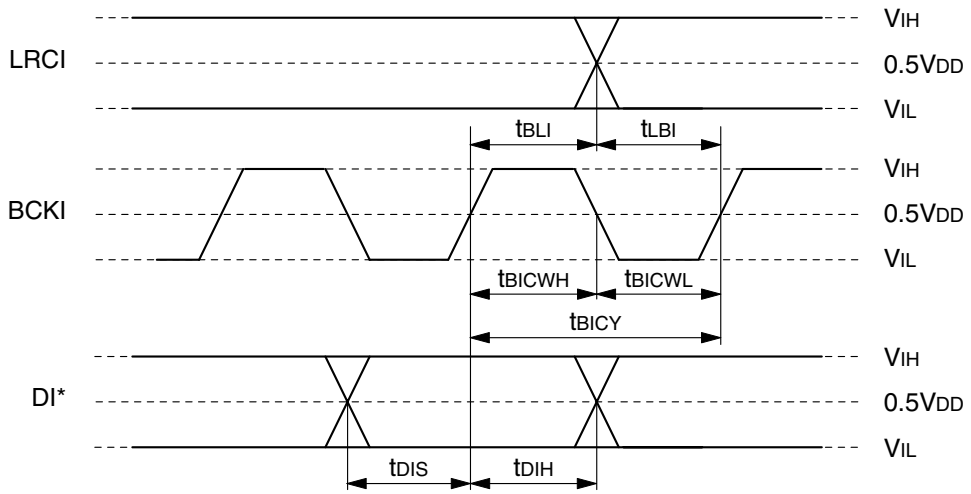
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RSTN pulsewidth	t_{RST}		$4t_{CY}$	–	–	ns

Note. t_{CY} = output-system clock (SCK input) cycle time



Serial inputs (LRCI, BCKI, DI* inputs)

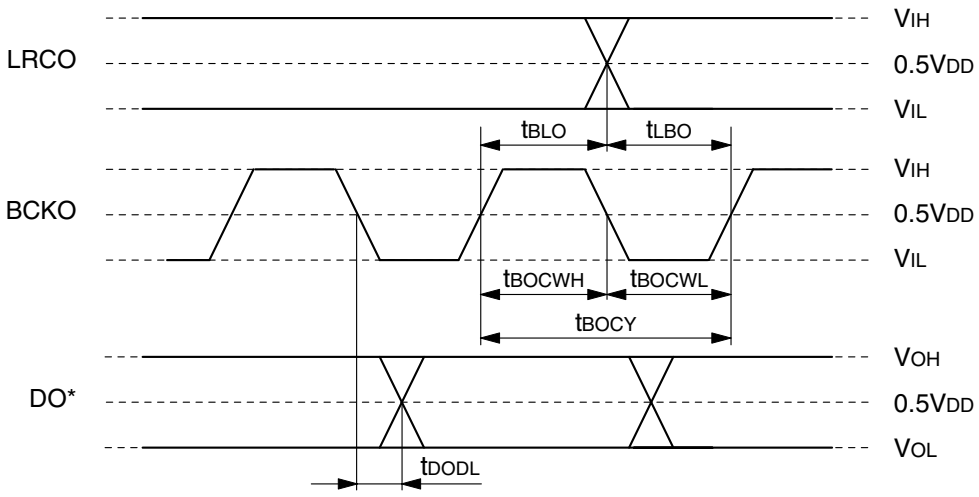
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LRCI cycle time	t_{LICY}		5	–	100	µs
BCKI pulse cycle time	t_{BICY}		78	–	3125	ns
BCKI HIGH-level pulsewidth	t_{BICWH}		30	–	–	ns
BCKI LOW-level pulsewidth	t_{BICWL}		30	–	–	ns
DI* setup time	t_{DIS}		30	–	–	ns
DI* hold time	t_{DIH}		30	–	–	ns
Last BCKI rising edge → LRCI edge	t_{BLI}		30	–	–	ns
LRCI edge → first BCKI rising edge	t_{LBI}		30	–	–	ns



Note. DI*: DIA, DIB, DIC pins

Serial outputs (SLAVEN = L: LRCO, BCKO inputs, DO* outputs)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LRCO cycle time	t_{LOCY}		20	–	33.34	µs
BCKO pulse cycle time	t_{BOCY}	SCKSLN = L	312.5	–	520.8	ns
		SCKSLN = H	416.6	–	694.4	
BCKO HIGH-level pulsewidth	t_{BOCWH}	SCKSLN = L	93.7	–	–	ns
		SCKSLN = H	125	–	–	
BCKO LOW-level pulsewidth	t_{BOCWL}	SCKSLN = L	93.7	–	–	ns
		SCKSLN = H	125	–	–	
Last BCKO rising edge → LRCO edge	t_{BLO}		30	–	–	ns
LRCO edge → first BCKO rising edge	t_{LBO}		30	–	–	ns
DO* output delay	t_{DODL}	C_L = 15pF	–	–	30	ns

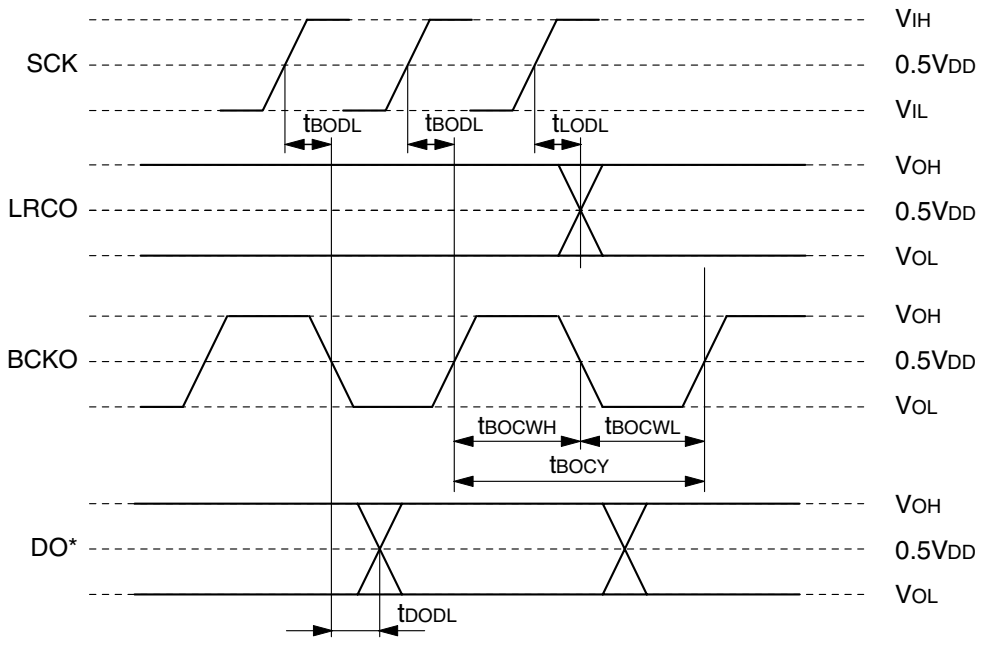


Note. DO*: DOA, DOB, DOC pins

Serial outputs (SLAVEN = H: LRCO, BCKO, DO* outputs)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LRCO cycle time	t_{LOCY}	SCKSLN = L	–	512	–	t_{CY}
		SCKSLN = H	–	768	–	
LRCO HIGH-level pulsewidth	t_{LOCWH}	SCKSLN = L	–	256	–	t_{CY}
		SCKSLN = H	–	384	–	
LRCO LOW-level pulsewidth	t_{LOCWL}	SCKSLN = L	–	256	–	t_{CY}
		SCKSLN = H	–	384	–	
BCKO pulse cycle time	t_{BOCY}	SCKSLN = L	–	8	–	t_{CY}
		SCKSLN = H	–	16	–	
BCKO HIGH-level pulsewidth	t_{BOCWH}	SCKSLN = L	–	4	–	t_{CY}
		SCKSLN = H	–	8	–	
BCKO LOW-level pulsewidth	t_{BOCWL}	SCKSLN = L	–	4	–	t_{CY}
		SCKSLN = H	–	8	–	
BCKO output delay	t_{BODL}	C_L = 15pF	–	–	30	ns
LRCO output delay	t_{LODL}	C_L = 15pF	–	–	30	ns
DO* output delay	t_{DODL}	C_L = 15pF	–	–	30	ns

Note. t_{CY} = output-system clock (SCK input) cycle time

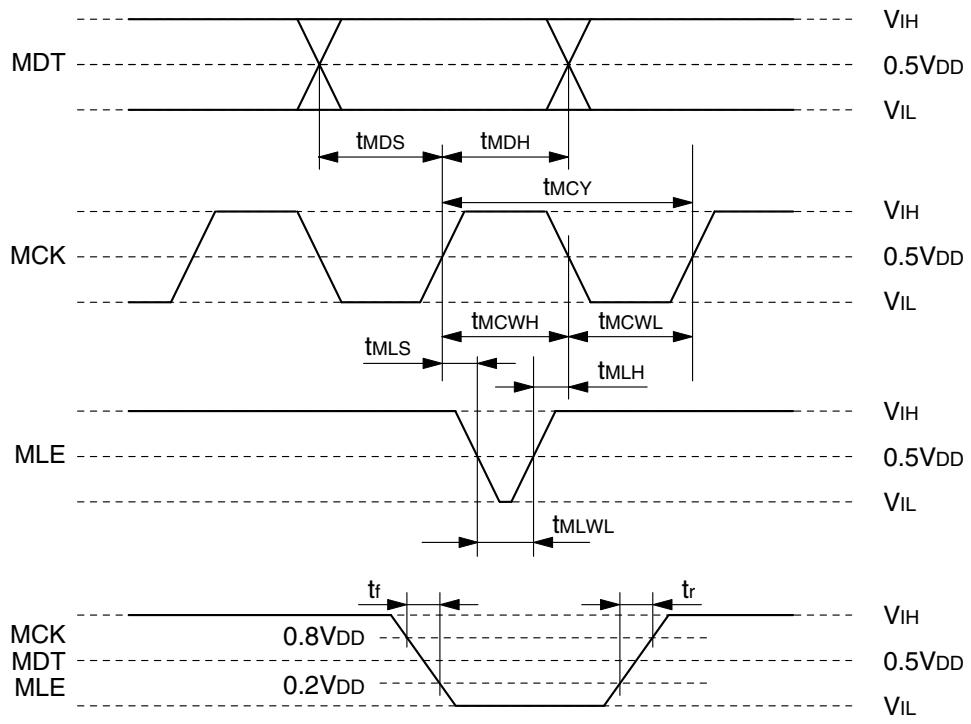


Note. DO*: DOA, DOB, DOC pins

MCU interface (MCK, MDT, MLE inputs)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
MCK cycle time	t_{MCY}		$60 + 4t_{CY}$	–	–	ns
MCK HIGH-level pulsewidth	t_{MCWH}		$30 + 2t_{CY}$	–	–	ns
MCK LOW-level pulsewidth	t_{MCWL}		$30 + 2t_{CY}$	–	–	ns
MDT setup time	t_{MDS}		$30 + t_{CY}$	–	–	ns
MDT hold time	t_{MDH}		$30 + t_{CY}$	–	–	ns
MLE LOW-level pulsewidth	t_{MLWL}		$30 + 2t_{CY}$	–	–	ns
MLE setup time	t_{MLS}		$30 + t_{CY}$	–	–	ns
MLE hold time	t_{MLH}		$30 + t_{CY}$	–	–	ns
Rise time	t_r		–	–	100	ns
Fall time	t_f		–	–	100	ns

Note. t_{CY} = output-system clock (SCK input) cycle time



FUNCTIONAL DESCRIPTION

Input Interface Setting (IMOD0, IMOD1, IWL0, IWL1 pins)

■ Input data format
- 2s-complement, MSB-first, L/R alternating serial IIS/non-IIS format

Format	IMOD1	IMOD0
IIS	L	L
MSB-first left-justified	L	H
MSB-first right-justified	H	L
MSB-first right-justified	H	H

■ Input word length
- 16/20/24-bit

Input word length	IWL1	IWL0
16 bits	L	L
20 bits	L	H
24 bits	H	L
24 bits	H	H

Input timing

See the timing for each of the input formats in figures 1 to 9.

Output Interface Settings (OMOD0, OMOD1, OWL0, OWL1, THROUN, SLAVEN pins)

■ Output data format
- 2s-complement, MSB-first, L/R alternating serial IIS/non-IIS format
- Continuous bit clock (64fso/48fso)

Format	OMOD1	OMOD0
IIS	L	L
MSB-first left-justified	L	H
MSB-first right-justified	H	L
MSB-first right-justified	H	H

■ Output word length
- 16/20/24-bit

Output word length	OWL1	OWL0
16 bits	L	L
20 bits	L	H
24 bits	H	L
24 bits	H	H

Output mode select

Pins		Function		
THROUN	SLAVEN	Mode	Description	LRCO, BCKO pin state
H	H	Master	LRCO, BCKO are derived by frequency division of the SCK input clock.	Outputs
	L	Slave	LRCO, BCKO are supplied externally. When SCKSLN = L, BCKO is set to 64fso. When SCKSLN = H, BCKO is set to 48fso.	Inputs
L	L or H	Through	The LRCI, BCKI, DIA, DIB, DIC inputs are fed directly to the LRCO, BCKO, DO* outputs. The DITO output is LOW-level.	Outputs

Output timing

See the timing for each of the output formats in figures 10 to 18. In slave mode, note that the LRCO and BCKO as timing shown in figures 10 to 14 must be inputted externally. In through mode, note that the LRCI, BCKI, DI* inputs are passed to the outputs as-is, regardless of the output data format setting, and that DITO is a LOW-level output.

Note. DI*: DIA, DIB, DIC pins
DO*: DOA, DOB, DOC pins

Output-System Clock (SCK, SCKSLN pins)

The output-system clock input must have a frequency of either 512fso or 768fso, where fso is the output-system sampling frequency. In master mode, the LRCO and BCKO signals are derived from this clock input by frequency division. This clock is also used as the system clock by the internal processing circuits.

SCKSLN	SCK input
L	512fso (fso = output-system sampling frequency) LRCO rate → 1fso BCKO rate → 64fso
H	768fso (fso = output-system sampling frequency) LRCO rate → 1fso BCKO rate → 48fso

System Reset (ERROR, RSTN pins)

Under the following conditions, the system must be reset for normal conversion operation. Reset occurs using a LOW-level pulse input on the RSTN pin.

- When power is applied
  The reset should be released (RSTN = L → H) after the supply voltage and LRCI, BCKI, SCK (and LRCO, BCKO in slave mode) clocks have stabilized.
- When the SCK clock is not continuous
  A reset is required when the SCK clock is dynamically switched or is not continuous, such as when switching the sampling frequency or when the clock momentarily stops due to the state of another IC. The reset should be released (RSTN = L → H) after the SCK clock has stabilized.
- When the LRCI, BCKI inputs are not continuous (SELFN = H)
  A reset is required when the LRCI and BCKI clocks are dynamically switched or are not continuous, such as when switching the sampling frequency or when the clock momentarily stops due to the state of another IC. The ERROR pin goes L → H to indicate the presence of an input problem, but the LSI continues to operate. The output generated as a result of the non-continuous clocks is not guaranteed, and it is recommended that the outputs be muted externally using DMUTEN or other means. The reset should be released (RSTN = L → H) after the LRCI and BCKI clocks have stabilized.
- When the LRCO, BCKO inputs (in slave mode) are not continuous (SELFN = H)
  A reset is required when the LRCO and BCKO clocks are dynamically switched or are not continuous, such as when switching the sampling frequency or when the clock momentarily stops due to the state of another IC. The ERROR pin goes L → H to indicate the presence of a slave input problem, but the LSI continues to operate. The output generated as a result of the non-continuous clocks is not guaranteed, and it is recommended that the outputs be muted externally using DMUTEN or other means. The reset should be released (RSTN = L → H) after the LRCO and BCKO clocks have stabilized.
  A reset is required, in such cases where the error is generated, when the input/output sample rate conversion ratio is set to an incorrect value based on the non-continuous clock, resulting in incorrect output data.
- Output state during the reset interval
  The DOA, DOB, DOC, and DITO are tied LOW (See “Direct Mute” for operation after reset is released). In master mode, the LRCO and BCKO pins are also tied LOW.
- The required time to detect ERROR
  The ERROR detection block counts input-clock and output-clock for a given times (SLAVEN = L). ERROR pin changes HIGH-level when the observed counts does not agree with the expected counts. Therefore it needs some time for ERROR to reflect a condition of the clock (see table below). In the case of SELFN = L, the same time is required to change H → L.

Output frequency [kHz]	The ERROR by LRCI, BCKI stopping		The ERROR by LRCO, BCKO stopping	
	min [ms]	max [ms]	min [μs]	max [μs]
32	6.0	8.0	93.8	125.0
44.1	4.3	5.8	68.0	90.7
48	4.0	5.3	62.5	83.3

Reset Mode (SELFN pin)

The operation after a non-continuous LRCI/BCKI input clock or LRCO/BCKO input clock (in slave mode) is detected, as described in "System Reset" above, is selected by the SELFN pin.

SELFN	Function
L	Automatic self reset when non-continuous input/output clocks are detected. The outputs are directly muted from the time when the non-continuous state is detected until the self reset is released.
H	The ERROR output goes L → H when non-continuous input/output clocks are detected. The output continues as-is during the time an external reset input is applied and released. Accordingly, to prevent incorrect output it is recommended that the outputs be directly muted using DMUTEN or other means.

Direct Mute (DMUTEN pin)

Direct mute ON/OFF

DMUTEN	Function
L	0 data is output from the next output word.
H	Audio data is output from the next output word.

Other mute operations

Direct mute is also applied during reset input cycles.

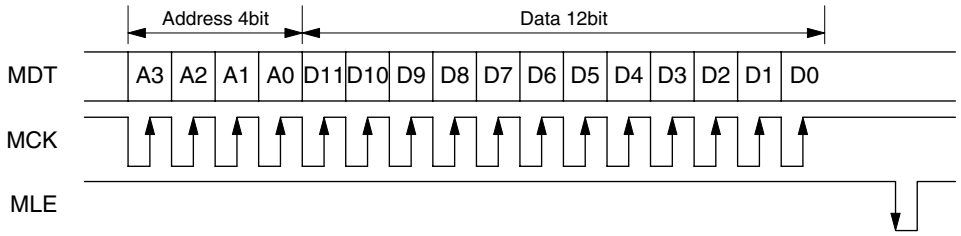
RSTN	Function
L	0 data is output from the next output word.
H	Processor data is output after the 8th output word after RSTN goes HIGH.

MCU Interface (MDT, MCK, MLE pins)

The SM5956A has a 3-wire serial MCU interface that is used to set the digital audio interface channel status data.

Command format

The commands from a microcontroller are input using the data input (MDT), bit clock (MCK), and load signal (MLE) inputs in bit serial format.



Write command format

Register table

■ Address: 0/H

Bit	Flag name	Description	Default
D11	Not used	Set to 0 for normal operation	0
D10	Not used	Set to 0 for normal operation	0
D9	Not used	Set to 0 for normal operation	0
D8	Not used	Set to 0 for normal operation	0
D7	Not used	Set to 0 for normal operation	0
D6	DMUTEN	Direct mute flag	1
D5	THROUN	Through mode flag	1
D4	SLAVEN	Slave mode flag	1
D3	OEDITON	DIT output enable flag	1
D2	DEEMN	Deemphasis select flag	1
D1	FS1	Deemphasis frequency select flag 1	0
D0	FS0	Deemphasis frequency select flag 0	0

Note. Each flag operates using logic-OR with its corresponding external input pin of the same name. If only the MCU interface is used for control, all the pins corresponding to the flags must be set to their inactive level. When the flags are set to their default level, control using external pins is enabled.

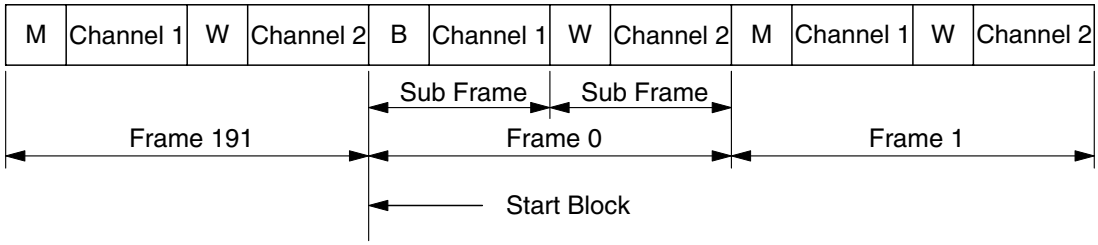
■ Address: 1/H

Bit	Flag name	Description		Default
D11	CNTL0	Channel status bit 0		0
D10	CNTL1	Channel status bit 1		0
D9	CNTL2	Channel status bit 2. COPY flag		0
D8	CNTL3	Channel status bit 3. EMP flag		0
D7	CATGY0	Category code set flag 0	(CATGY1, CATGY0) = category (0, 0) = “100 0000L” (CD) (0, 1) = “100 1100L” (DVD) (1, 0) = “100 0100L” (VCD) (1, 1) = “010 1100L” (SRC)	0
D6	CATGY1	Category code set flag 1		0
D5	Not used			0
D4	LBIT	Channel status bit 15		0
D3	CFS1	Channel status bit 24		0
D2	CFS2	Channel status bit 25		0
D1	CP1	Channel status bit 28		0
D0	CP2	Channel status bit 29		0

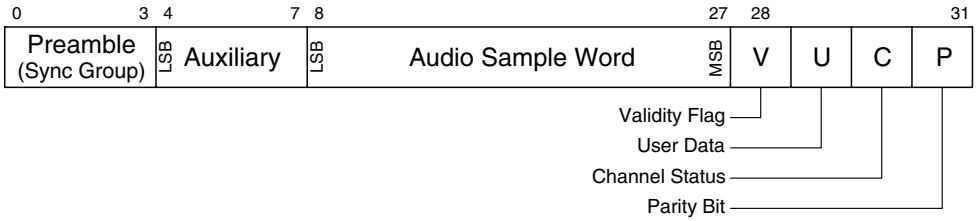
Note. This LSI can accept 4 type category codes shown in the table.

Digital Audio Interface

When the OEDITON pin is LOW, the digital audio interface output on DITO pin is enabled. The input signal on DIA is sample rate converted, then a preamble is added and biphase mark encoded to form the output. In through mode, the DITO pin is forcibly tied LOW-level. When the SM5956A is operating in slave mode, the digital interface does not operate whenever the LRCO/BCKO are not operating as inputs.



Frame Format



Subframe Format

Preamble

The preamble is a specific pattern used for subframe and block synchronization and discrimination. It is assigned to the first four time slots (0 to 3) and is represented by 8 consecutive states when biphase mark encoded at the transfer rate. There are 3 preamble patterns. The leading subframe within a block has a B pattern preamble. All other channel 1 subframes have an M pattern preamble, and all channel 2 subframes have a W pattern preamble.

Preamble	Channel coding	
	Leading symbol: 0	Leading symbol: 1
B	11101000	00010111
M	11100010	00011101
W	11100100	00011011

Note. This LSI starts with a 0, therefore only the preamble for a 0 leading symbol is used.

Audio sample word and auxiliary data

The audio sample word is represented by 20 bits in the digitized audio signal. The auxiliary data has various uses, including ancillary information or audio sample word length extension. The SM5956A audio data, however, is structured in 16-bit words, so bits 4 to 11 are output as 0 data. The audio data is output in bit positions 12 to 27 with the LSB first.

Validity flag

The validity flag is set to 0 when the audio sample word transferred is valid, and is set to 1 when the data is invalid. The SM5956A sets the validity flag to 1 when direct mute is turned ON.

User data

The user data are user-defined bits originally provided in the standard in response to user requests, but the SM5956A sets all user data bits to 0.

	0	1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:	:
1164	0	0	0	0	0	0	0	0	0	0	0	0

Channel status

The channel status bits can be used to transfer various information, including audio sample word length, pre-emphasis, sampling frequency, time codes, source numbers, and destination codes. The SM5956A sets only 9 bits: CP1, CP2, LBIT, CNTL0 to 3, CFS1, and CFS2. The 15th bit of the 8th to 15th bit in the category code can be used to set LBIT status bit but 8th to 14th bit were determined by the category codes CATGY0, 1 (See "Register table"). All other bits are set to 0.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	CNTL0	CNTL1	CNTL2	CNTL3	0	0	0	0	×	×	×	×	×	0	0	LBIT
16	0	0	0	0	L = 1	R = 1	0	0	CFS1	CFS2	0	0	CP1	CP2	0	0
32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
48	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
80	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
96	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
112	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
128	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
144	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
160	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
176	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Parity bit

The parity bit is used to indicate when an odd number of errors occur due to interface problems. The SM5956A sets the parity bit to 1 if the number of 1 bits in the other 27 data bits of the digital audio interface (excluding the preamble) is odd, and sets the parity bit to 0 if the number of 1 bits is even, thereby insuring that the number of 1 bits in the 28-bit data is always even.

Sample Rate Conversion

The input-to-output sample rate conversion ratio can be arbitrarily set to any value between 0.45 to 4.41 (SCKSLN = L, 512fso operation) or 0.225 to 4.41 (SCKSLN = H, 768fso operation). The input-system sample rate (fsi) range is 10kHz to 200kHz, and the output-system sample rate (fso) range is 30kHz to 50kHz. However, note that due to system clock frequency limitations, fsi = 44.1kHz to fso = 192kHz conversion for example is not supported.

Converter performance

Internal data word length: 20 bits
Deemphasis filter gain deviation from ideal characteristic: ± 0.03dB
Anti-aliasing filter characteristic: Passband ripple ± 0.0001dB
Stopband attenuation > 98dB

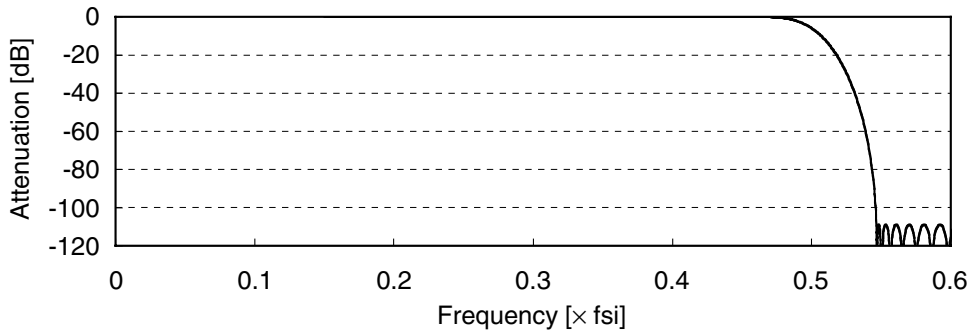
Conversion noise levels

- Internal quantization noise: ≤ –96dB
- Output rounding-off noise: 16-bit output –98dB
  20-bit output –122dB
  24-bit output –146dB

Combined output theoretical S/N

Output word length	Input word length		
	16 bits	20 bits	24 bits
16 bits	–92.3dB	–94.0dB	–94.0dB
20 bits	–94.0dB	–96.0dB	–96.0dB
24 bits	–94.1dB	–96.1dB	–96.2dB

Anti-aliasing filter characteristics



Anti-aliasing filter frequency response

Deemphasis (DEEMN pin)

Traditional deemphasis filters employ an analog circuit construction. This device uses an IIR digital filter that faithfully reproduces the gain and phase response of analog filters. The filter coefficients are selected to match the input sample rate fsi (44.1kHz, 48.0kHz, 32.0kHz), set by the FS0 and FS1 pins.

Deemphasis ON/OFF

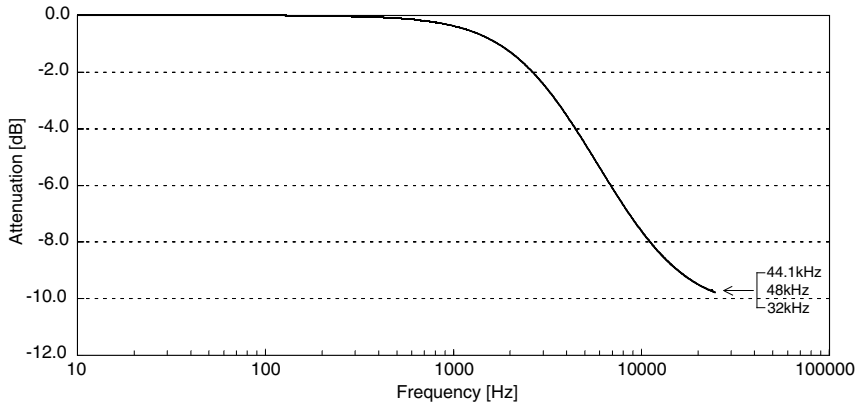
DEEMN = L : Deemphasis ON
DEEMN = H: Deemphasis OFF

Deemphasis filter coefficient selection

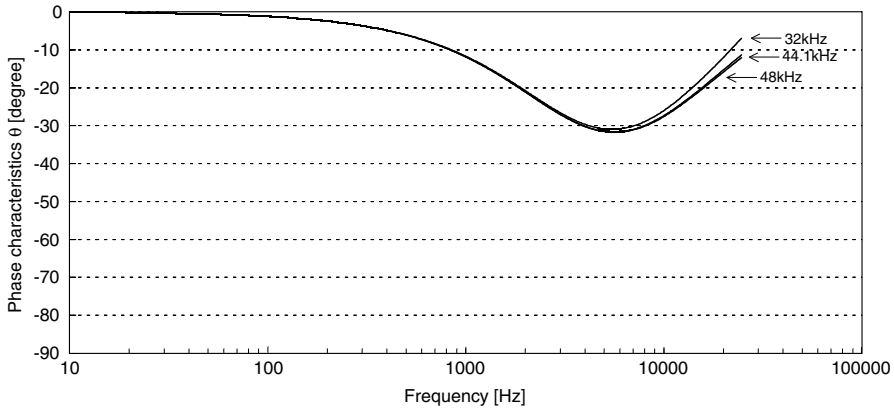
The deemphasis filter coefficients are selected by the FS0 and FS1 pins.

fsi	FS0	FS1
44.1kHz	L	L
44.1kHz	H	L
48.0kHz	L	H
32.0kHz	H	H

Deemphasis filter characteristics



Deemphasis filter frequency response

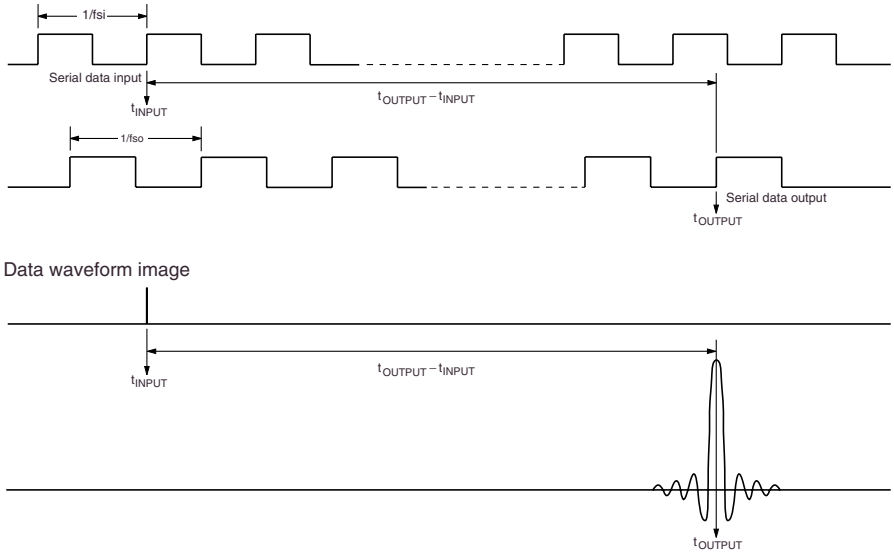


Deemphasis filter phase response

Group Propagation Delay

t_{INPUT} : Serial input data (fsi rate) read end timing (LRCI clock rising edge)
t_{OUTPUT} : Serial output data (fso rate) output start timing (LRCO clock rising edge)
Cratio : Sample rate conversion ratio (fsi/fso)

$t_{OUTPUT} - t_{INPUT} = ((51.791 \times Cratio + 41.557) \pm 36)/fso$ (at SCKSLN = H, 768fso operation)
$t_{OUTPUT} - t_{INPUT} = ((51.122 \times Cratio + 38.647) \pm 36)/fso$ (at SCKSLN = L, 512fso operation)



Response Time

A certain amount of time is required to calculate the sample rate conversion ratio in the conversion rate detector. Assuming as a prerequisite that the SM5956A is supplied with a stable input-system sampling frequency (fsi: input on LRCI) and a stable output-system sampling frequency (fso: derived from the SCK clock), the time required after system reset to determine the sample rate conversion ratio with 16-bit precision is defined as the minimum response time, given by:

Response time = 28140/fso (638ms at fso = 44.1kHz)

Input frequency fsi [kHz]	Output frequency fso [kHz]	Response time [ms]	
		SCKSLN = L	SCKSLN = H
32	44.1	594	285
32	48	557	263
44.1	32	822	406
44.1	48	473	228
48	32	799	403
48	44.1	478	302
32	32	447	395
44.1	44.1	325	287
48	48	298	264

TIMING DIAGRAMS

Input Timing (LRCI, BCKI, DIA, DIB, DIC pins)

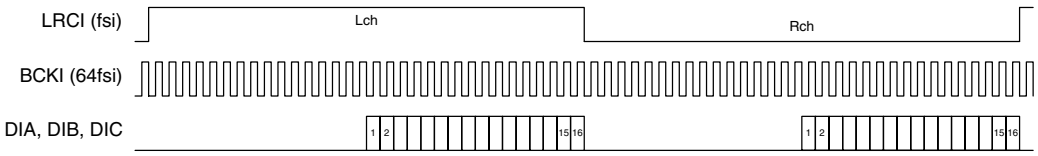


Figure 1. 16-bit MSB-first right-justified (IMOD1 = H, IMOD0 = H, IWL1 = L, IWL0 = L)
BCKI = 32fsi to 64fsi

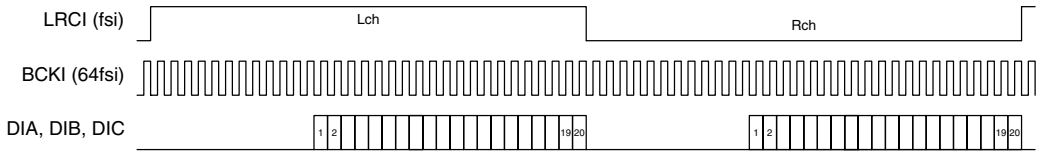


Figure 2. 20-bit MSB-first right-justified (IMOD1 = H, IMOD0 = H, IWL0 = L, IWL0 = H)
BCKI = 40fsi to 64fsi

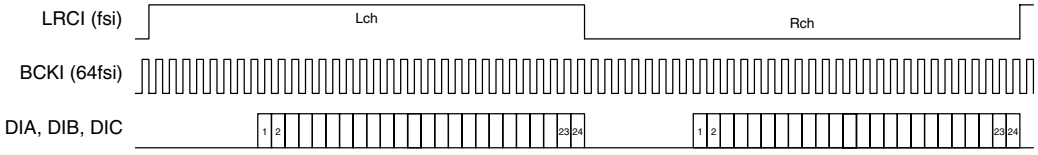


Figure 3. 24-bit MSB-first right-justified (IMOD1 = H, IMOD0 = H, IWL1 = H, IWL0 = H)
BCKI = 48fsi to 64fsi

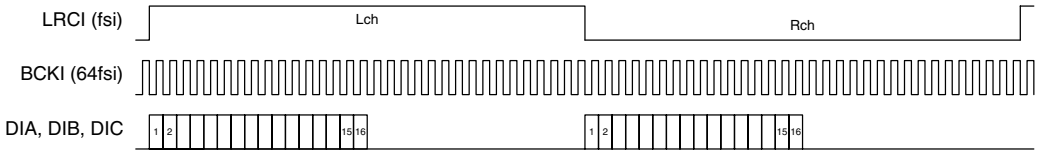


Figure 4. 16-bit MSB-first left-justified (IMOD1 = L, IMOD0 = H, IWL1 = L, IWL0 = L)
BCKI = 32fsi to 64fsi

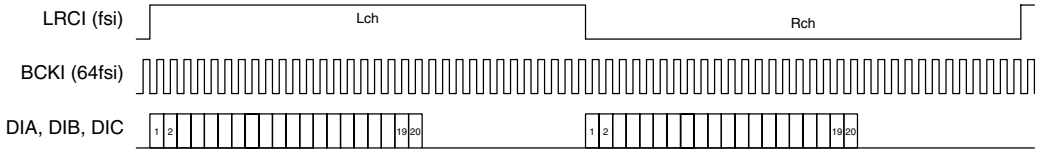


Figure 5. 20-bit MSB-first left-justified (IMOD1 = L, IMOD0 = H, IWL1 = L, IWL0 = H)
BCKI = 40fsi to 64fsi

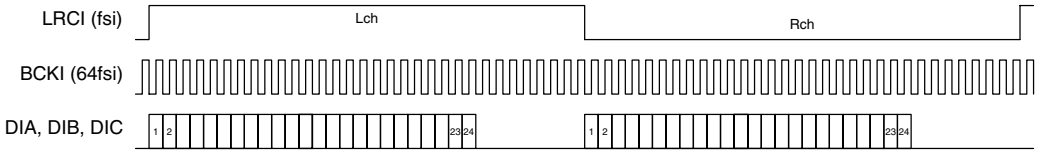


Figure 6. 24-bit MSB-first left-justified (IMOD1 = L, IMOD0 = H, IWL1 = H, IWL0 = H)
BCKI = 48fsi to 64fsi

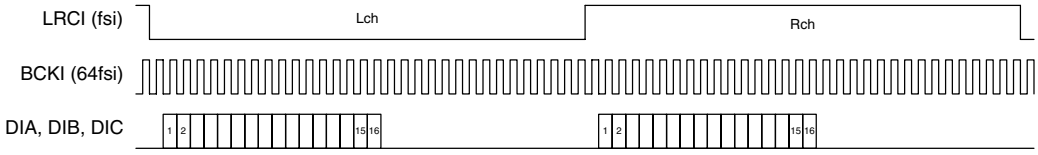


Figure 7. 16-bit IIS (IMOD1 = L, IMOD0 = L, IWL1 = L, IWL0 = L)
BCKI = 64fsi only

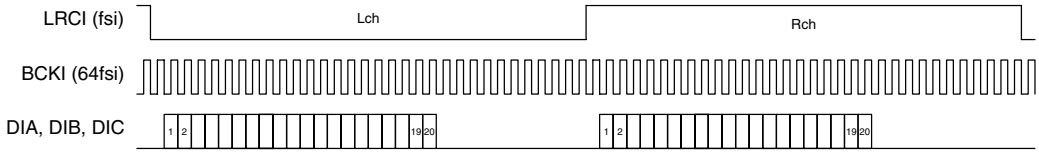


Figure 8. 20-bit IIS (IMOD1 = L, IMOD0 = L, IWL1 = L, IWL0 = H)
BCKI = 64fsi only

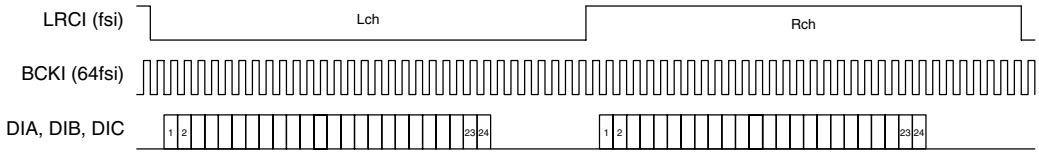


Figure 9. 24-bit IIS (IMOD1 = L, IMOD0 = L, IWL1 = H, IWL0 = H)
BCKI = 64fsi only

Output Timing (LRCO, BCKO, DOA, DOB, DOC pins)

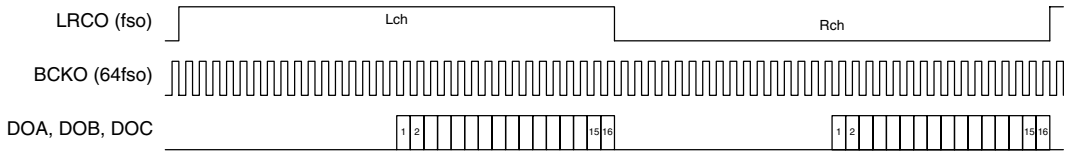


Figure 10. 16-bit MSB-first right-justified (OMOD1 = H, OMOD0 = H, OWL1 = L, OWL0 = L)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

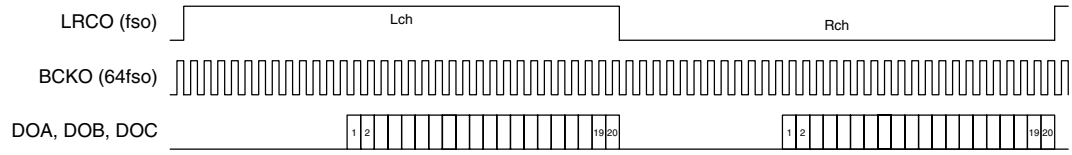


Figure 11. 20-bit MSB-first right-justified (OMOD1 = H, OMOD0 = H, OWL1 = L, OWL0 = H)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

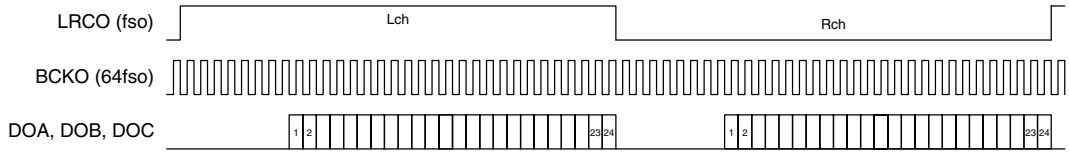


Figure 12. 24-bit MSB-first right-justified (OMOD1 = H, OMOD0 = H, OWL1 = H, OWL0 = H)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

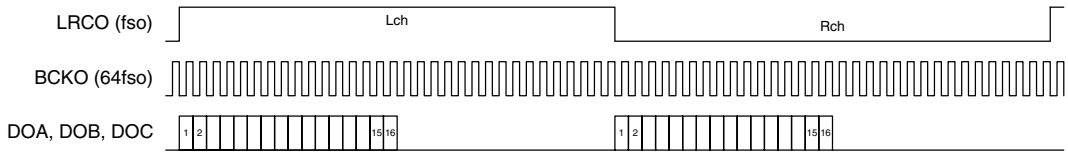


Figure 13. 16-bit MSB-first left-justified (OMOD1 = L, OMOD0 = H, OWL1 = L, OWL0 = L)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

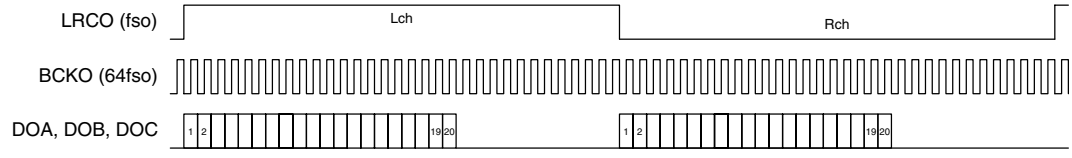


Figure 14. 20-bit MSB-first left-justified (OMOD1 = L, OMOD0 = H, OWL1 = L, OWL0 = H)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

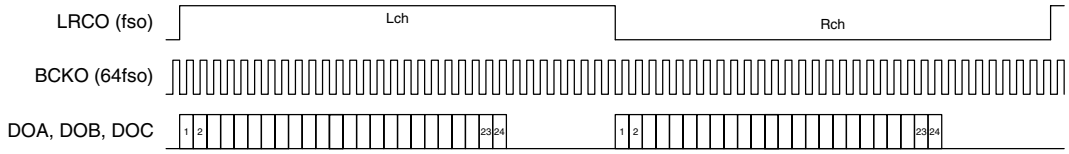


Figure 15. 24-bit MSB-first left-justified (OMOD1 = L, OMOD0 = H, OWL1 = H, OWL0 = H)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

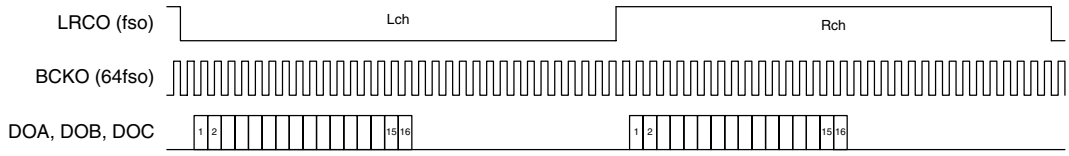


Figure 16. 16-bit IIS (OMOD1 = L, OMOD0 = L, OWL1 = L, OWL0 = L)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

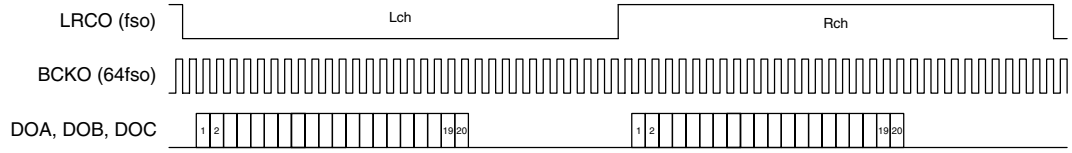


Figure 17. 20-bit IIS (OMOD1 = L, OMOD0 = L OWL1 = L, OWL0 = H)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

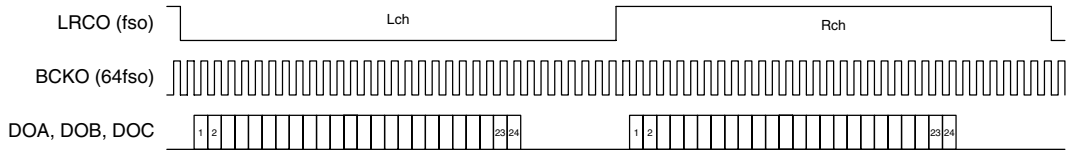
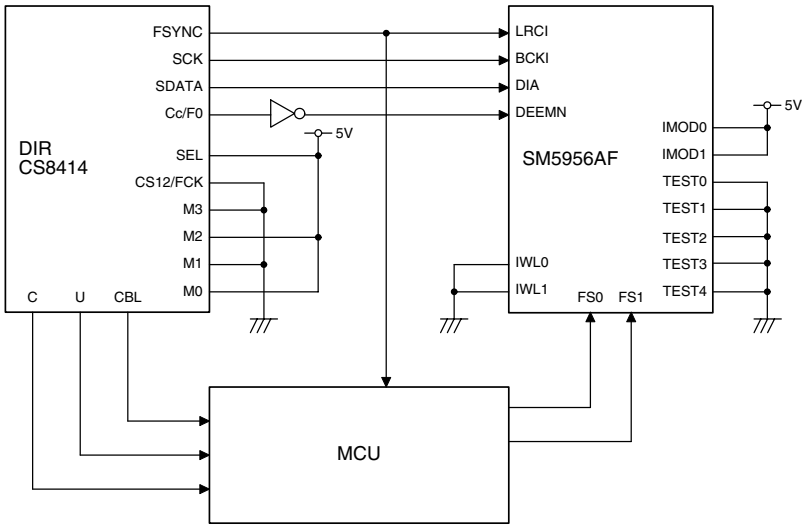


Figure 18. 24-bit IIS (OMOD1 = L, OMOD0 = L, OWL1 = H, OWL0 = H)
BCKO = 48fso (SCKSLN = H), 64fso (SCKSLN = L, the above)

TYPICAL APPLICATION CIRCUITS

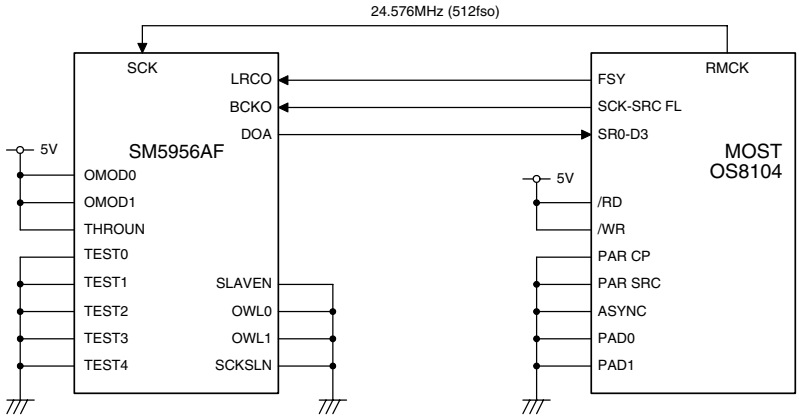
Input Interface Connection Example

Connection with digital audio interface receiver (DIR: CS8414)



Output Interface Connection Example

Connection with a MOST interface transceiver (OS8104)



Please pay your attention to the following points at time of using the products shown in this document.

The products shown in this document (hereinafter "Products") are not intended to be used for the apparatus that exerts harmful influence on human lives due to the defects, failure or malfunction of the Products. Customers are requested to obtain prior written agreement for such use from SEIKO NPC CORPORATION (hereinafter "NPC"). Customers shall be solely responsible for, and indemnify and hold NPC free and harmless from, any and all claims, damages, losses, expenses or lawsuits, due to such use without such agreement. NPC reserves the right to change the specifications of the Products in order to improve the characteristic or reliability thereof. NPC makes no claim or warranty that the contents described in this document dose not infringe any intellectual property right or other similar right owned by third parties. Therefore, NPC shall not be responsible for such problems, even if the use is in accordance with the descriptions provided in this document. Any descriptions including applications, circuits, and the parameters of the Products in this document are for reference to use the Products, and shall not be guaranteed free from defect, inapplicability to the design for the mass-production products without further testing or modification. Customers are requested not to export or re-export, directly or indirectly, the Products to any country or any entity not in compliance with or in violation of the national export administration laws, treaties, orders and regulations. Customers are requested appropriately take steps to obtain required permissions or approvals from appropriate government agencies.

NPC

SEIKO NPC CORPORATION

15-6, Nihombashi-kabutocho, Chuo-ku,
Tokyo 103-0026, Japan
Telephone: +81-3-6667-6601
Facsimile: +81-3-6667-6611
http://www.npc.co.jp/
Email: sales@npc.co.jp

NC0412BE 2006.04