HARRIS

HI-1818A/883
HI-1828A/883

Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers

July 1987

T-51-11

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low On Resistance (Max. Over Temp.).....500Ω
- Wide Analog Signal Range .....±15V
- Very Low Power Consumption.....< 30mW
- Access Time (Max. Over Temp.).....1000ns
- Break-Before-Make Switching

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

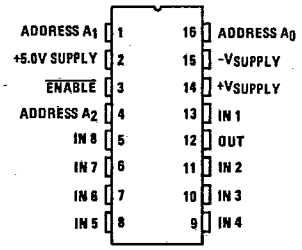
The HI-1818A/883 and HI-1828/883 are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (250nA max.) and low channel ON resistance (500Ω max.) assure optimum performance in low level or current mode applications.

The HI-1818A/883 is a single-ended 8 channel multiplexer, while the HI-1828A/883 is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

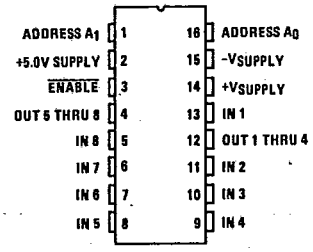
5 CMOS ANALOG MULTIPLEXERS

Pinouts

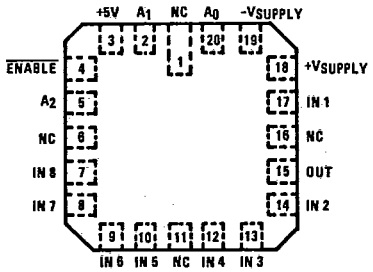
HI1-1818A/883 (CERAMIC DIP)
TOP VIEW



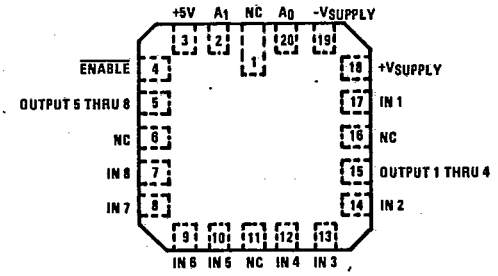
HI1-1828A/883 (CERAMIC DIP)
TOP VIEW



HI4-1818A/883 (CERAMIC LCC)
TOP VIEW

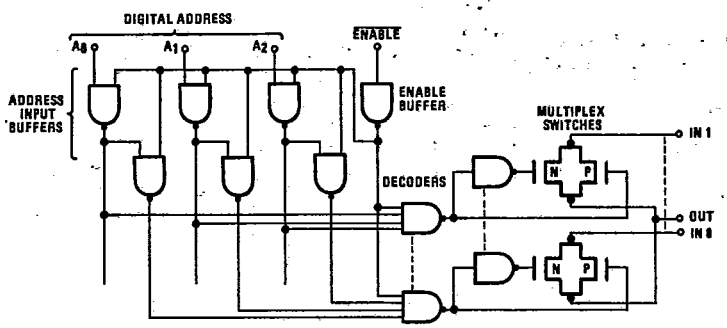


HI4-1828A/883 (CERAMIC LCC)
TOP VIEW

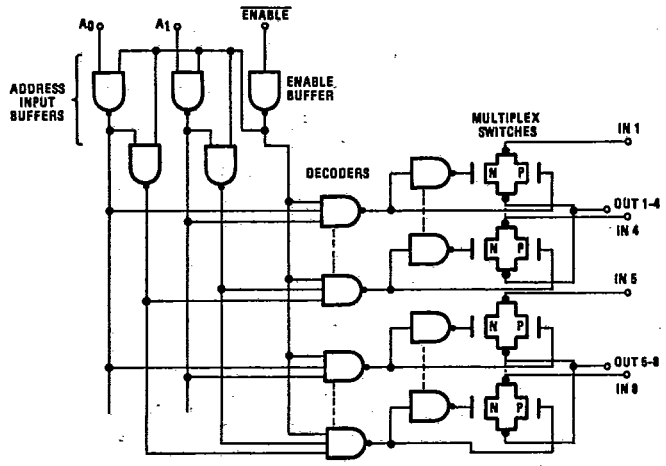


Functional Diagrams

HI-1818A/883



HI-1828A/883



TRUTH TABLES

HI-1818A/883

ADDRESS				"ON"
A_2	A_1	A_0	$\overline{EN}$	CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	None

HI-1828A/883

ADDRESS			"ON"
A_1	A_0	$\overline{EN}$	CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	None

Absolute Maximum Ratings

Voltage Between Supply Pins 40V
$+V_{SUPPLY}$ to Ground 20V
$-V_{SUPPLY}$ to Ground 20V
V_L to GND 30V
Analog Input Voltage
$+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Digital Input Voltage
$+V_{\overline{EN}}$, $+V_A$ ..... $+V_{SUPPLY}$
$-V_{\overline{EN}}$, $-V_A$ ..... $-V_{SUPPLY}$
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max.) 40mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... 275°C
Junction Temperature ..... +175°C
Thermal Resistance, Junction-to-Case (θjc)
Ceramic DIP Package ..... 35°C/W
Ceramic LCC Package ..... 25°C/W
Thermal Resistance, Junction-to-Ambient (θja)
Ceramic DIP Package ..... 90°C/W
Ceramic LCC Package ..... 83°C/W
Power Dissipation (@ 75°C)
Ceramic DIP Package 1.11W
Ceramic LCC Package 1.20W
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package ..... 11.1mW/°C
Ceramic LCC Package ..... 12.0mW/°C
ESD Classification ..... ≤ 2000V

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Analog Input Voltage (V_S) ..... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) ..... 0V to 0.4V
Logic High Level (V_{AH}) ..... 4.0V to $+V_{SUPPLY}$
+5.0V Supply (V_L) ..... +5.0V
Max RMS Current, S or D 11mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, $V_{\overline{EN}}$ = 0.4V, V_L = +5V Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect all Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
	I_{IL}	Measure Inputs Sequentially, Connect all Unused Inputs to 5V	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, $V_{\overline{EN}}$ = 4.0V All Unused Inputs = -10V	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, $V_{\overline{EN}}$ = 4.0V All Unused Inputs = +10V	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, $V_{\overline{EN}}$ = 4.0V All Unused Inputs = -10V HI-1818A/883	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-250	+250	nA
		HI-1828A/883	2, 3	+125°C, -55°C	-125	+125	nA
	$-I_{D(OFF)}$	V_D = -10V, $V_{\overline{EN}}$ = 4.0V All Unused Inputs = +10V HI-1818A/883	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-250	+250	nA
		HI-1828A/883	2, 3	+125°C, -55°C	-125	+125	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = +10V, $V_{\overline{EN}}$ = 0.4V All Unused Inputs = -10V HI-1818A/883	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-250	+250	nA
		HI-1828A/883	2, 3	+125°C, -55°C	-125	+125	nA
	$-I_{D(ON)}$	V_S = V_D = -10V, $V_{\overline{EN}}$ = 0.4V All Unused Inputs = +10V HI-1818A/883	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-250	+250	nA
		HI-1828A/883	2, 3	+125°C, -55°C	-125	+125	nA
Positive Supply Current	I(+)	$V_{\overline{EN}}$ = 0.4V, V_{AL} = 0.4V, V_{AH} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	—	0.5	mA
Negative Supply Current	I(-)	$V_{\overline{EN}}$ = 0.4V V_{AL} = 0.4V, V_{AH} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0	—	mA
Logic Supply Current	I_L	$V_{\overline{EN}}$ = 0.4V V_{AL} = 0.4V, V_{AH} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	—	1.0	mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V I_D = 1mA	1	+25°C	—	400	Ω
			2, 3	+125°C, -55°C	—	500	Ω
	$-R_{DS1}$	V_S = -10V I_D = -1mA	1	+25°C	—	400	Ω
			2, 3	+125°C, -55°C	—	500	Ω
Logic Level Voltage	V_{AL}	Applied to all Digital Inputs for all DC Tests	1, 2, 3	+25°C, +125°C, -55°C	—	0.4	V
	V_{AH}	Applied to all Digital Inputs for all DC Tests	1, 2, 3	+25°C, +125°C, -55°C	4.0	—	V

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, $\overline{V_{EN}}$ = 0.4V, V_L = +5V Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 200Ω, C_L = 12.5pF	9	+25°C	5	—	ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 12.5pF	9	+25°C	—	500	ns
			10, 11	+125°C, -55°C	—	1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 200Ω, C_L = 12.5pF	9	+25°C	—	500	ns
	$t_{OFF(EN)}$	R_L = 200Ω, C_L = 12.5pF	10, 11	+125°C, -55°C	—	1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, $\overline{V_{EN}}$ = 0.4V, V_L = +5V Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address	C_A	V+ = V- = 0V, f = 1MHz	1	+25°C	—	10	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V, f = 1MHz HI-1818A/883	1	+25°C	—	50	pF
		HI-1828A/883	1	+25°C	—	25	pF
Capacitance: Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	1	+25°C	—	10	pF
Charge Transfer Error	V_{CTE}	V_S = GND, V_{GEN} = 0V to 5V	1	+25°C	—	10	mV
Off Isolation	V_{ISO}	$\overline{V_{EN}}$ = 4.0V, R_L = 1k, C_L = 15pF, V_S = 7V_{RMS}, f = 100kHz	1	+25°C	-50	—	dB

NOTE: 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

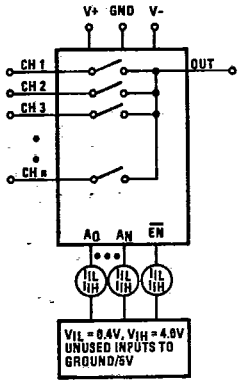
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

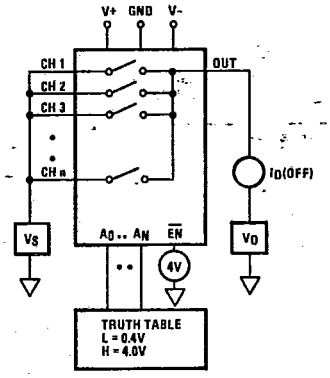
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

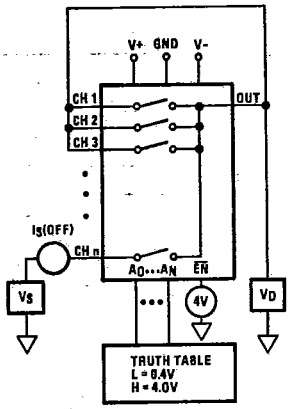
INPUT LEAKAGE CURRENT



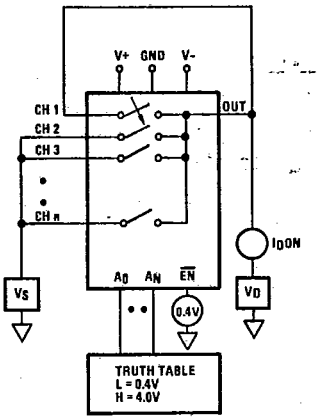
ID(OFF)



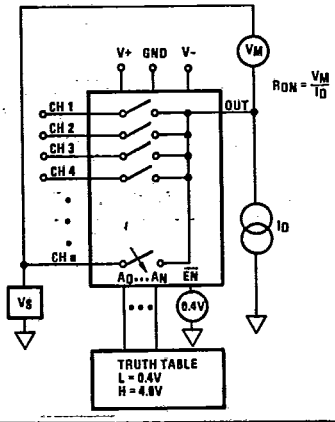
IS(OFF)



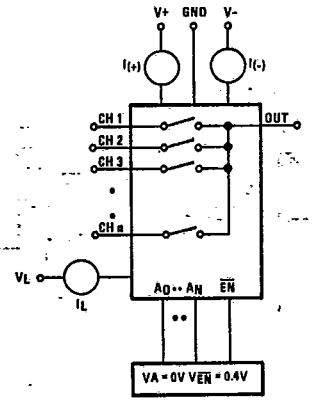
ID(ON)



RDS



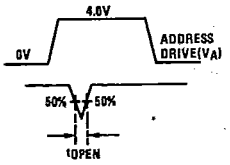
SUPPLY CURRENTS



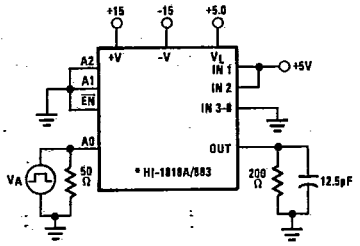
5 CMOS ANALOG MULTIPLEXERS

Switching Waveforms

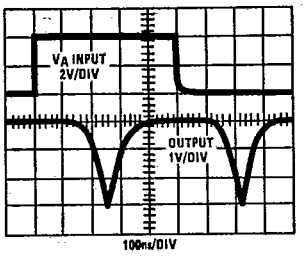
ADDRESS DRIVE



BREAK-BEFORE-MAKE DELAY (tOPEN)

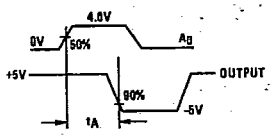


BREAK-BEFORE-MAKE DELAY (tOPEN)

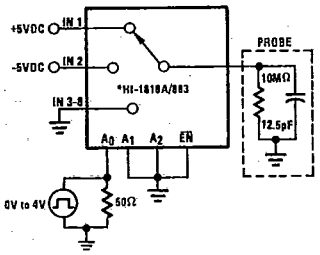


*Similar Connection for HI-1828A/883

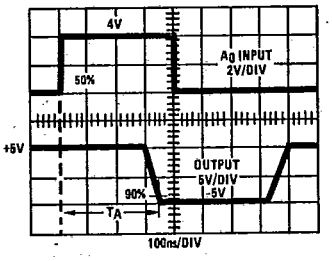
ADDRESS DRIVE



ACCESS TIME

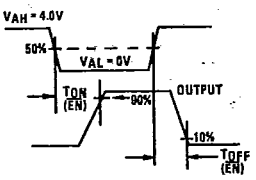


ACCESS TIME

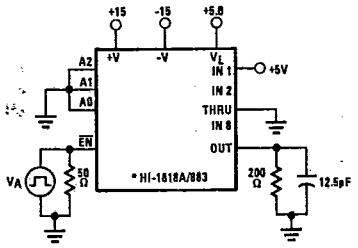


*Similar Connection for HI-1828A/883

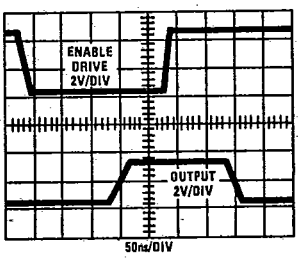
ENABLE DRIVE



ENABLE DELAY tON(EN), tOFF(EN)



ENABLE DELAY tON(EN), tOFF(EN)



*Similar Connection for HI-1828A/883

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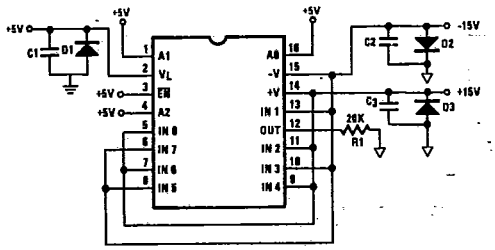
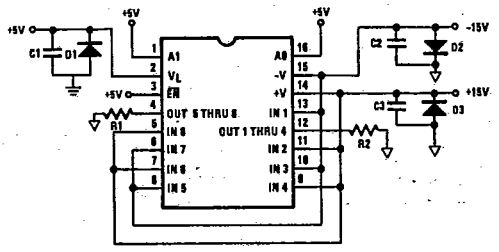
Burn-In Circuits

HI-1818A/883 CERAMIC DIP



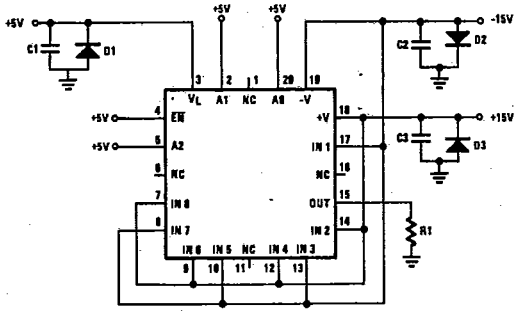
NOTES:
R_1 = 20kΩ ± 5%, 1/2 or 1/4W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 (or equivalent) (per board)

HI-1828A/883 CERAMIC DIP



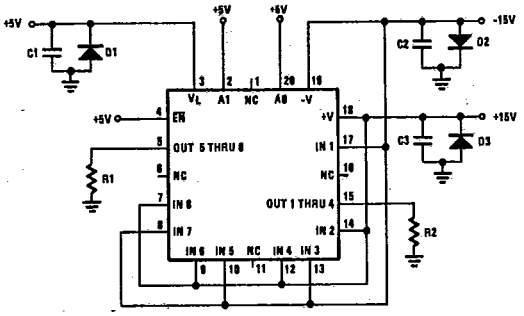
NOTES:
R_1, R_2 = 20kΩ ± 5%, 1/2 or 1/4W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 (or equivalent) (per board)

HI-1818A/883 CERAMIC LCC



NOTES:
R_1 = 20kΩ ± 5%, 1/4 or 1/2W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 (or equivalent) (per board)

HI-1828A/883 CERAMIC LCC



NOTES:
R_1, R_2 = 20kΩ ± 5%, 1/4 or 1/2W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 (or equivalent) (per board)

Schematic Diagrams

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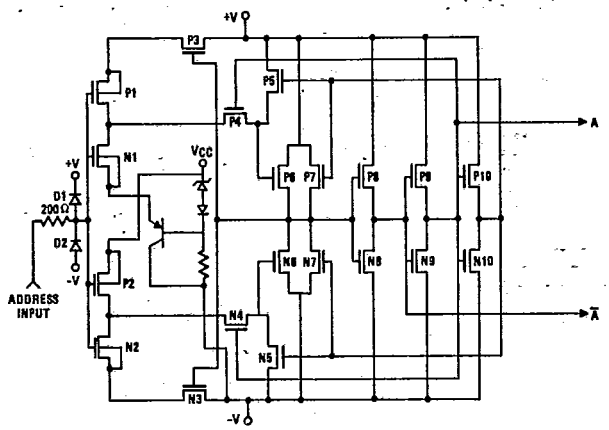
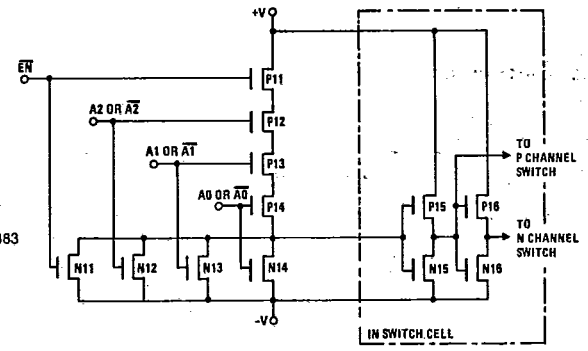
ADDRESS INPUT BUFFER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated



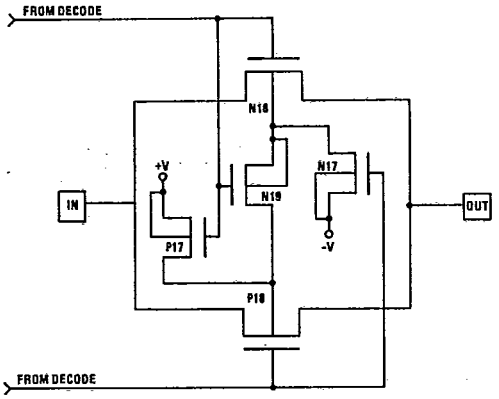
ADDRESS DECODER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
A_2 or $\overline{A_2}$ not used for HI-1828A/883



MULTIPLEX SWITCH

All N- Channel Bodies to V-
All P- Channel Bodies to V+
Unless Otherwise Indicated



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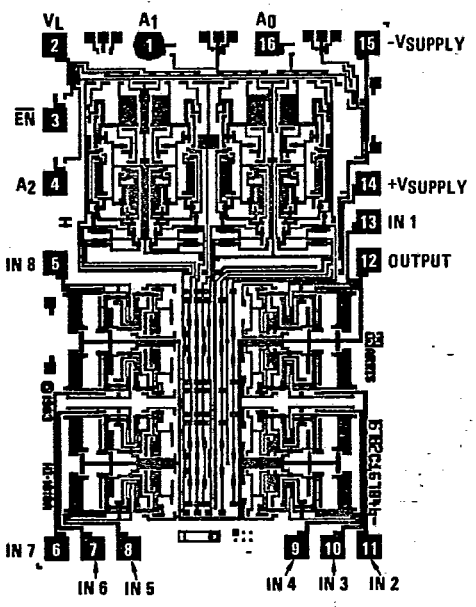
Die Characteristics

DIE DIMENSIONS: 67.7 x 103.5 x 19 mil
METALLIZATION
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ
WORST CASE CURRENT DENSITY: 1.43 x 10^5 A/cm^2

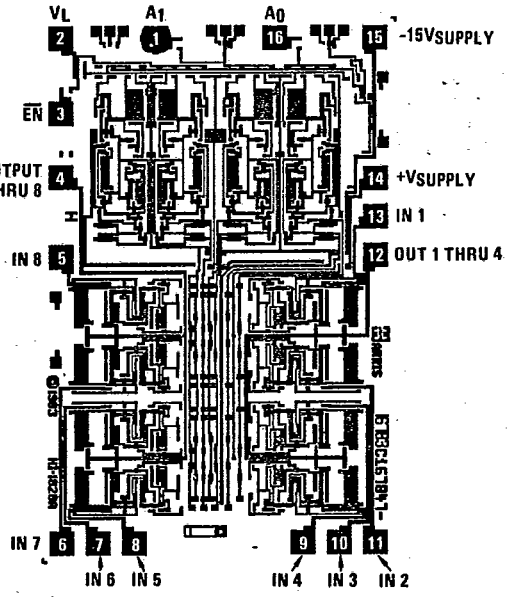
TRANSISTOR COUNT:
HI-1818A/883 210
HI-1828A/883 210
PROCESS: CMOS-DI
DIE ATTACH
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-1818A/883



HI-1828A/883



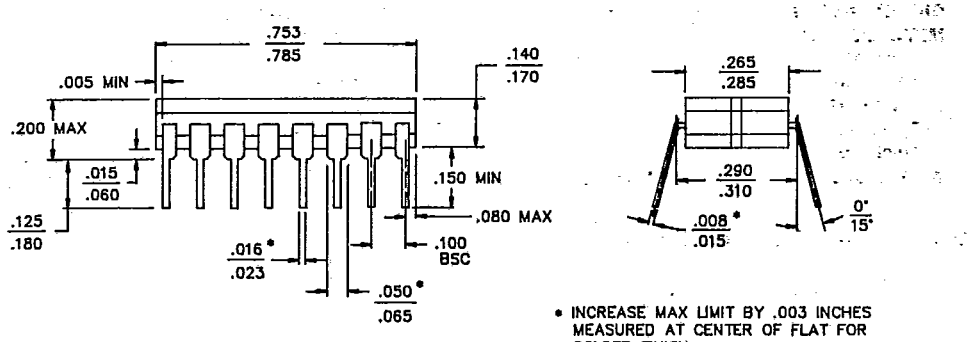
NOTE: Pad Numbers Correspond to DIP Pin Numbers Only

5 CMOS ANALOG MULTIPLEXERS

T-51-11

Packaging†

16 PIN CERAMIC DIP

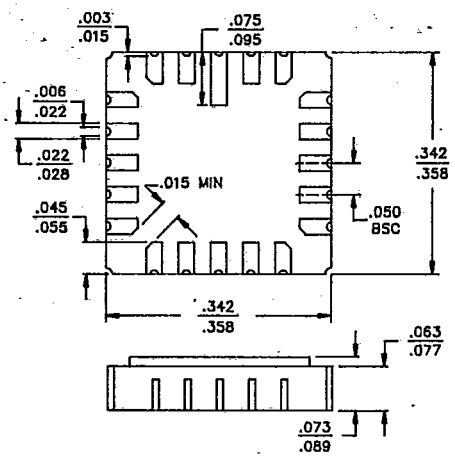


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

† MIL-M-38510 Compliant Materials, Finishes & Dimensions.

HI-1818A
HI-1828A

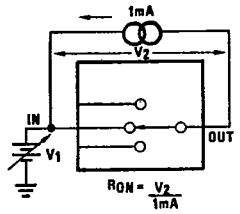
DESIGN INFORMATION

Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers

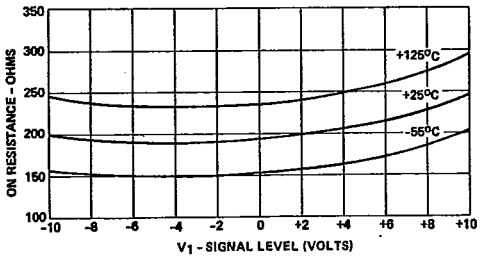
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics

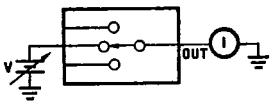
ON RESISTANCE vs. ANALOG SIGNAL LEVEL



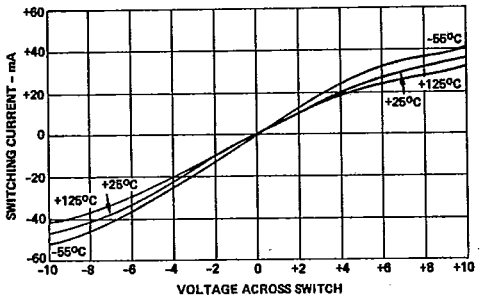
Test Circuit



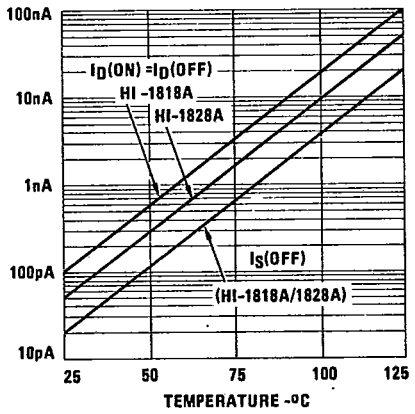
ON CHANNEL CURRENT vs. VOLTAGE



Test Circuit



LEAKAGE CURRENT vs. TEMPERATURE



5 CMOS ANALOG MULTIPLEXERS