SOJ, TSOP
Commercial Temp
Industrial Temp

128K x 8
1Mb Asynchronous SRAM

8, 9ns
3.3V V_{DD}
Center V_{DD} & V_{SS}

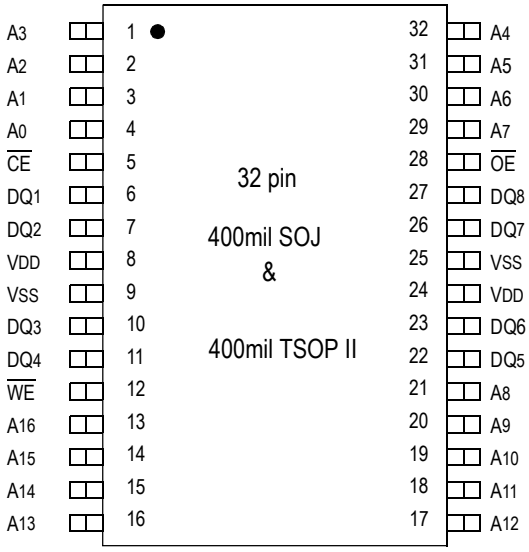
Features

- Fast access time: 8, 9ns
- CMOS low power operation: 150/150 mA at min. cycle time.
- Single 3.3V ± 0.3V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Industrial Temperature Option: -40° to 85°C
- Package line up
  - J: 400mil, 32 pin SOJ package
  - TP: 400mil, 32 pin TSOP Type II package

Description

The GS71208 is a high speed CMOS static RAM organized as 131,072-words by 8-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3V power supply and all inputs and outputs are TTL compatible. The GS71208 is available in 400 mil SOJ and 400 mil TSOP Type-II packages.

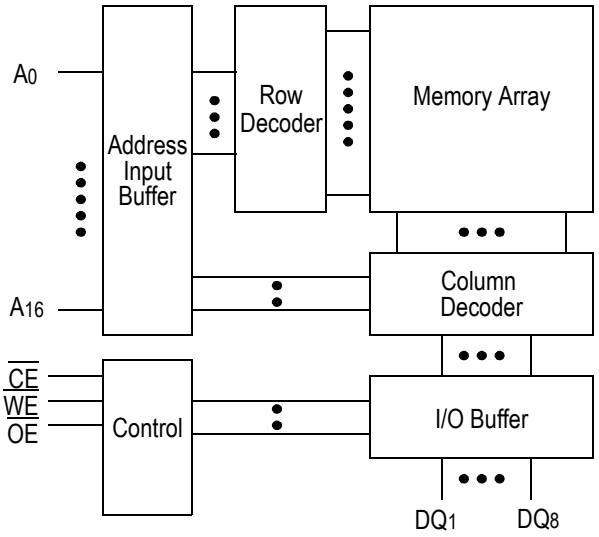
SOJ & TSOP-II 128K x 8 Pin Configuration



Pin Descriptions

Symbol	Description
A_0 to A_{16}	Address input
DQ_1 to DQ_8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{DD}	+3.3V power supply
V_{SS}	Ground
NC	No connect

Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ1 to DQ8	VDD Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	IDD
L	X	L	Write	
L	H	H	High Z	

Note: X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.5 to +4.6	V
Input Voltage	VIN	-0.5 to VDD+0.5 (≤ 4.6V max.)	V
Output Voltage	VOUT	-0.5 to VDD+0.5 (≤ 4.6V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	TSTG	-55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -9	V_{DD}	3.0	3.3	3.6	V
Supply Voltage for -8	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	-	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	-	70	°C
Ambient Temperature, Industrial Range	T_{AI}	-40	-	85	°C

Note:
1. Input overshoot voltage should be less than V_{DD}+2V and not exceed 20ns.
2. Input undershoot voltage should be greater than -2V and not exceed 20ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	7	pF

Notes:
1. Tested at T_A=25°C, f=1MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	-1uA	1uA
Output Leakage Current	I_{LO}	Output High Z V_{OUT} = 0 to V_{DD}	-1uA	1uA
Output High Voltage	V_{OH}	I_{OH} = - 4mA	2.4	
Output Low Voltage	V_{OL}	I_{LO} = + 4mA		0.4V

Power Supply Currents

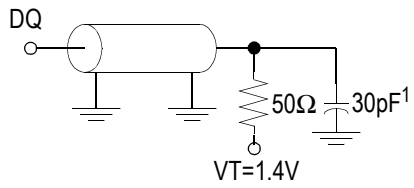
Parameter	Symbol	Test Conditions	0 to 70°C		-40 to 85°C	
			8ns	9ns	8ns	9ns
Operating Supply Current	I_{DD}	$\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time I_{OUT} = 0 mA	150mA	150mA	160mA	160mA
Standby Current	I_{SB1}	$\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	55mA	55mA	65mA	65mA
Standby Current	I_{SB2}	$CE \geq V_{DD}$ - 0.2V All other inputs $\geq V_{DD}$ - 0.2V or $\leq$ 0.2V	15mA		25mA	

AC Test Conditions

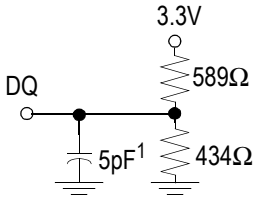
Parameter	Conditions
Input high level	V_{IH}=2.4V
Input low level	V_{IL}=0.4V
Input rise time	tr=1V/ns
Input fall time	tf=1V/ns
Input reference level	1.4V
Output reference level	1.4V
Output load	Fig. 1& 2

Note:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.

Output Load 1



Output Load 2



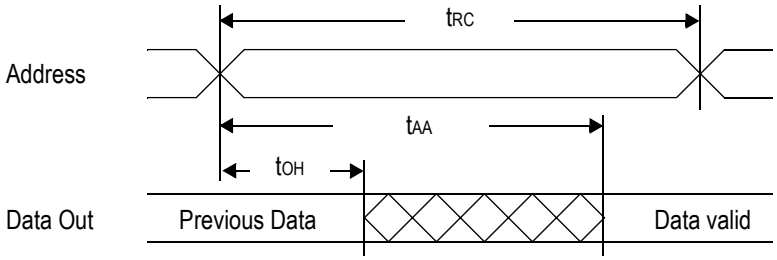
AC Characteristics

Read Cycle

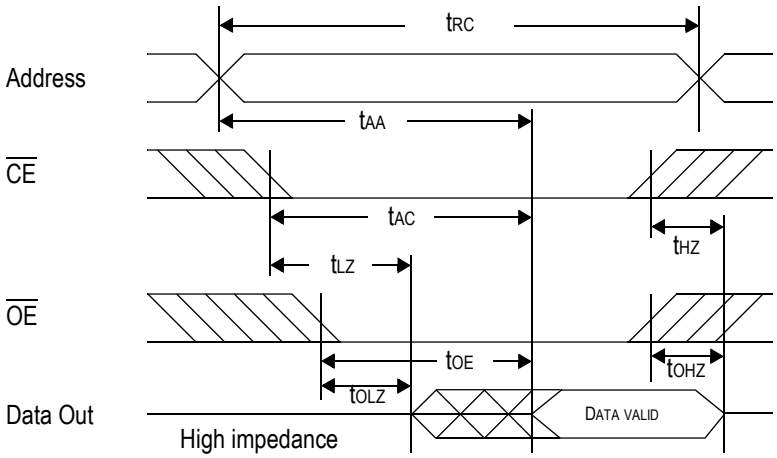
Parameter	Symbol	-8		-9		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	8	---	9	---	ns
Address access time	t_{AA}	---	8	---	9	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	---	8	---	9	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	---	3.5	---	3.5	ns
Output hold from address change	t_{OH}	3	---	3	---	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	---	3	---	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	---	0	---	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	---	4	---	4	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	---	3.5	---	3.5	ns

* These parameters are sampled and are not 100% tested

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



Read Cycle 2: $\overline{WE}$ = V_{IH}

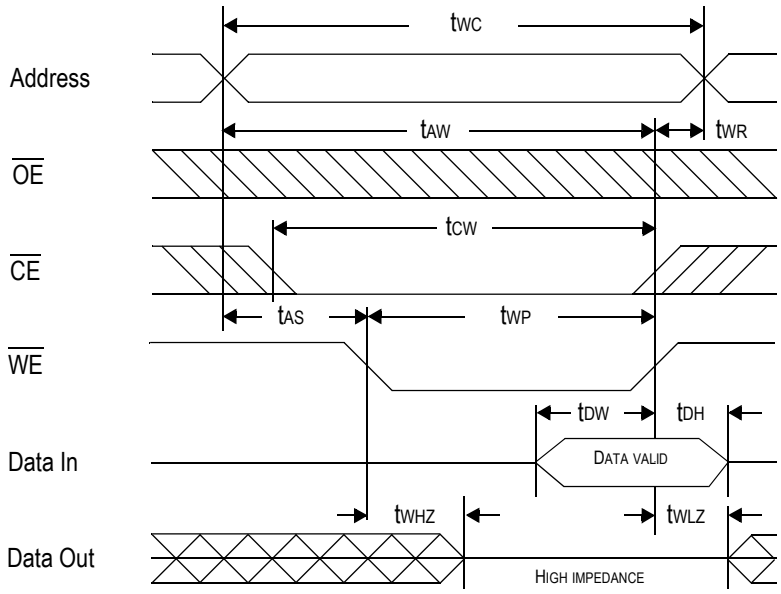


Write Cycle

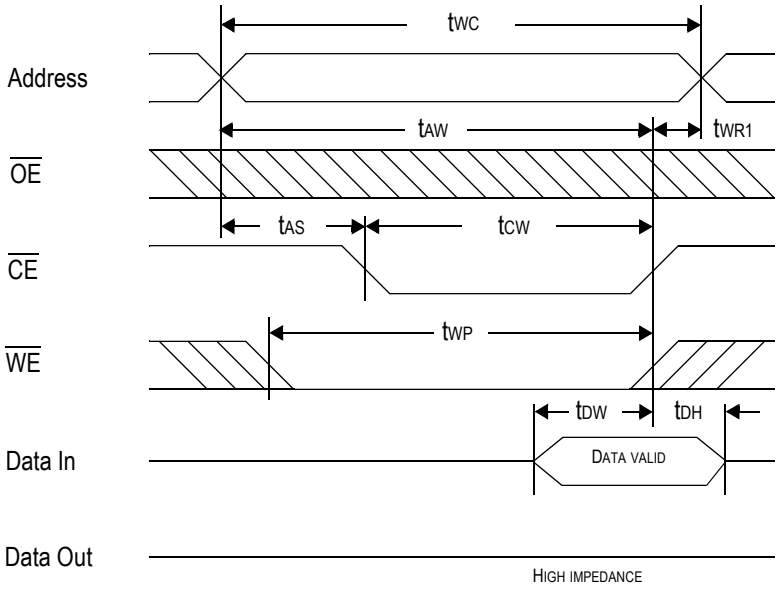
Parameter	Symbol	-8		-9		Unit
		Min	Max	Min	Max	
Write cycle time	tWC	8	---	9	---	ns
Address valid to end of write	tAW	5.5	---	5.5	---	ns
Chip enable to end of write	tCW	5.5	---	5.5	---	ns
Data set up time	tDW	4	---	4	---	ns
Data hold time	tDH	0	---	0	---	ns
Write pulse width	tWP	5.5	---	5.5	---	ns
Address set up time	tAS	0	---	0	---	ns
Write recovery time ($\overline{WE}$)	tWR	0	---	0	---	ns
Write recovery time ($\overline{CE}$)	tWR1	0	---	0	---	ns
Output Low Z from end of write	tWLZ*	3	---	3	---	ns
Write to output in High Z	tWHZ*	---	3.5	---	3.5	ns

* These parameters are sampled and are not 100% tested

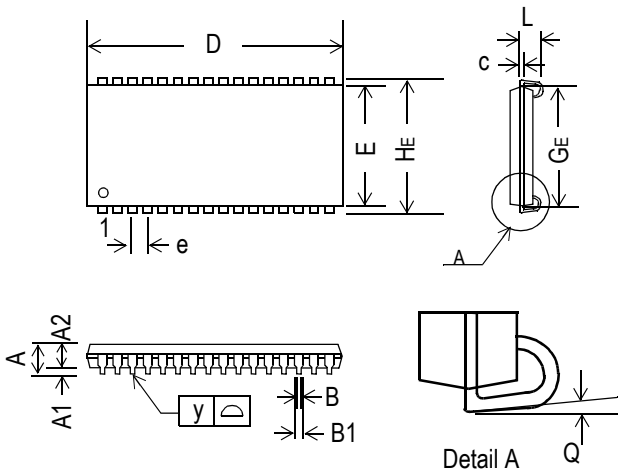
Write Cycle 1: $\overline{WE}$ control



Write Cycle 2: $\overline{CE}$ control



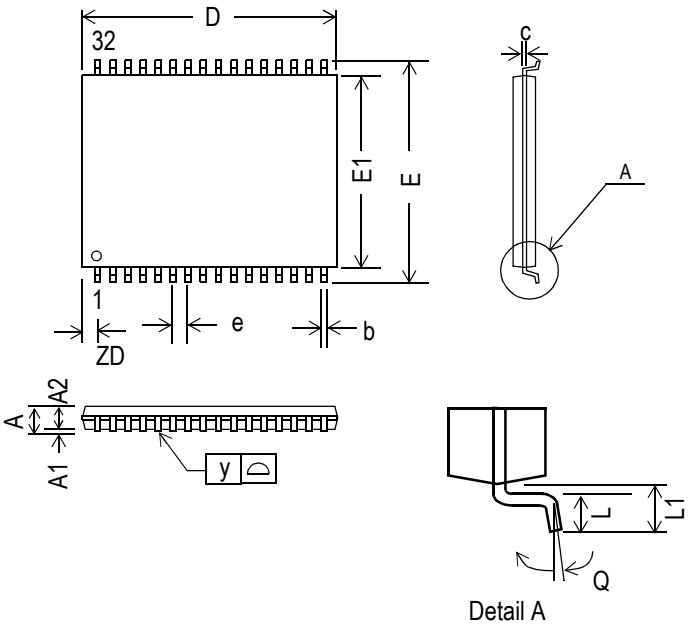
32 Pin SOJ, 400 mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.146	-	-	3.70
A1	0.026	-	-	0.66	-	-
A2	0.105	0.110	0.115	2.67	2.80	2.92
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.824	0.829	20.83	20.93	21.06
E	0.395	0.400	0.405	10.04	10.16	10.28
e	-	0.05	-	-	1.27	-
HE	0.430	0.435	0.440	10.93	11.05	11.17
GE	0.354	0.366	0.378	9.00	9.30	9.60
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Q	0^o	-	10^o	0^o	-	10^o

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

32 Pin TSOP-II, 400mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.039	-	0.05	-	-	1.27
A1	0.002	-	0.006	0.01	-	0.15
A2	0.037	0.040	0.045	0.90	1.02	1.14
b	0.012	0.016	0.018	0.30	0.40	0.45
c	0.0047	0.0051	0.0062	0.12	0.13	0.16
D	0.820	0.825	0.830	20.82	20.95	21.08
ZD	-	0.037	-	-	0.95	-
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.395	0.400	0.405	10.03	10.16	10.29
e	-	0.05	-	-	1.27	-
L	0.017	0.020	0.023	0.40	0.50	0.60
L1	0.024	0.031	0.039	0.60	0.80	1.00
y	0.00	-	0.003	0.00	-	0.76
Q	0^o	-	5^o	0^o	-	5^o

Note:
1.Dimension D includes mold flash, protrusions or gate burrs.
2. Dimension E does not include interlead flash
3. Controlling dimension: mm

Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS71208J-8	400 mil SOJ	8 ns	Commercial	
GS71208J-9	400 mil SOJ	9 ns	Commercial	
GS71208J-8I	400 mil SOJ	8 ns	Industrial	
GS71208J-9I	400 mil SOJ	9 ns	Industrial	
GS71208TP-8	400 mil TSOP-II	8 ns	Commercial	
GS71208TP-9	400 mil TSOP-II	9 ns	Commercial	
GS71208TP-8I	400 mil TSOP-II	8 ns	Industrial	
GS71208TP-9I	400 mil TSOP-II	9 ns	Industrial	

* Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. For example: GS71208TP-8T

Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
1.00 12/1999/1.01 12/1999	Content	1. Added TP package to 71208
GS71208Rev1.01 12/1999KRev 1.01 2/2000L	Format/Content	1. GSI Logo 2. Added Dimension D to 32 pin 400 ml TSOP II Package.

