# 2 Micron CMOS Process Family

## Features

- Double Poly / Double Metal
- 4 µm Poly and Metal 1 Pitch
- 320 ps Delay per stage (Ring Osc.)
- 5.5 Volts Maximum Operating Voltage
- 2.7~3.6 Volts Low Voltage Option
- Shrinkable to Mitel 1.5µm Process
- ProToDuction™ Option for low cost prototypes
- 150mm Wafers

## Description

The 2µm P-Well process provides flexibility, speed and packing density needed in mixed signal designs. The aggressive design rules make it comparable to most 1.5µm processes. Also, the MOSFET transistors are designed with very shallow source-drain junctions and a thin gate oxide to improve speed. A low voltage option is available for 3 volts applications. It offers low and matched threshold voltages for improved dynamic range needed in mixed analog/digital applications.

## Process parameters

| Process Parameters | 2µm (5 volts & 3volts) | Units |
|---|---|---|
| Metal I pitch (width / space) | 2 / 2 | µm |
| Metal II pitch (width / space) | 2.6 / 2.4 | µm |
| Poly pitch (width / space) | 2 / 2 | µm |
| Contact | 2 x 2 | µm |
| Via | 2.4 x 2.4 | µm |
| Gate geometry | 2 | µm |
| P-well junction depth | 4 | µm |
| N+ junction depth | 0.20 | µm |
| P+ junction depth | 0.28 | µm |
| Gate oxide thickness | 325 | Å |
| Inter poly oxide thick. | 500 | Å |

## MOSFET Electrical parameters

| Electrical Parameters | 2 MICRON - 5 volts | | | | | | 2 MICRON - 3 volts | | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | N Channel | | | P Channel | | | N Channel | | | P Channel | | | | |
| | min. | typ. | max. | min. | typ. | max. | min. | typ. | max. | min. | typ. | max. | | |
| Vt (10x2µm) | 0.55 | 0.70 | 0.85 | 0.55 | 0.70 | 0.85 | 0.35 | 0.50 | 0.65 | 0.35 | 0.50 | 0.65 | V | saturation |
| Ids (10x2µm) | | 160 | | | 70 | | | 175 | | | 80 | | µA/µm | Vds=Vgs=5volts |
| Gain β (10x2µm) | | 325 | | | 120 | | | 325 | | | 120 | | $\mu A/V^2$ | |
| Body Factor (50x50µm) | | 0.40 | | | 0.40 | | | 0.35 | | | 0.35 | | $\bar{Dv}$ | |
| Bvdss | 10 | 12 | | 10 | 13 | | 10 | 12 | | 10 | 13 | | V | Ids=100nA |
| Subthreshold Slope | | 100 | | | 100 | | | | | | | | mV/dec. | Vds=0.1v |
| Substrate Current | | 0.25 | 0.34 | | | | | 0.25 | 0.34 | | | | µA/µm | Vds=5.5v; Vgs=2.7v |
| Field Threshold | 10 | 18 | | 10 | 17 | | 10 | 18 | | 10 | 17 | | V | Ids = 14µA |
| L Effective | | 1.8 | | | 1.7 | | | 1.8 | | | 1.7 | | µm | L drawn = 2µm |


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# 2 Micron CMOS Process Family (cont'd)

## Resistances (¾ /sq.)

| | 2 µm 5 volts & 3 volts | | | |
|---|---|---|---|---|
| | min. | typ. | max. | Temp. coef. (Ω/sq/$^0$C) |
| Pwell | | 13000 | | 140 |
| Pfield in Pwell | 3000 | 3600 | 4200 | 32 |
| N+ | 35 | 45 | 55 | .06 |
| P+ | 80 | 100 | 120 | .15 |
| Poly gate | 15 | 20 | 25 | .02 |
| Poly capacitor | 75 | 100 | 125 | .06 |
| Metal I | | 0.038 | | |
| Metal II | | 0.038 | | |

## Capacitances (fF/µm$^2$)

| | 2 µm 5 volts & 3 volts | | |
|---|---|---|---|
| | min. | typ. | max. |
| Inter-poly | .62 | .73 | .84 |
| Gate oxide | 0.99 | 1.06 | 1.15 |
| N+ Junction | | .195 | |
| P+ Junction | | .138 | |

## Bipolar gain[1]

| | 2 µm 5 volts | | |
|---|---|---|---|
| | min. | typ. | max. |
| NPN vertical | | 300 | |

[1]Test condition : Vce = 5 volts

**FIG 1: I-V Characteristics for a 50x2µm N-MOSFET (2µm 5 volts process)**

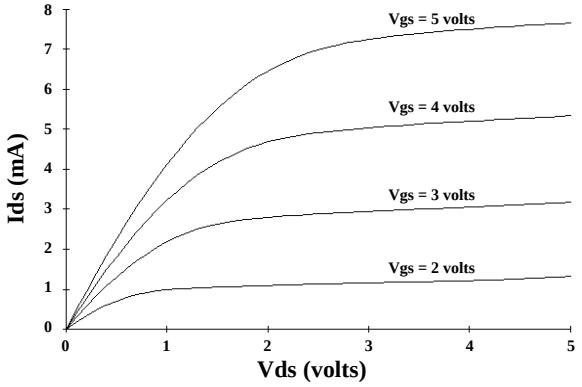



**FIG 2: I-V Characteristics for a 50x2µm P-MOSFET (2µm 5 volts process)**

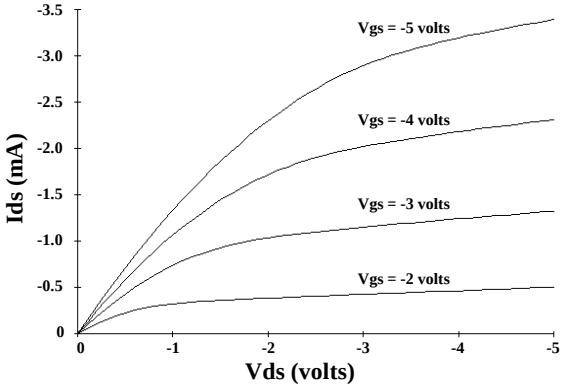



**FIG 3: Subthreshold Characteristics at Vds=0.1 volts for a 50x2µm N-MOSFET (2µm 5 volts Process)**

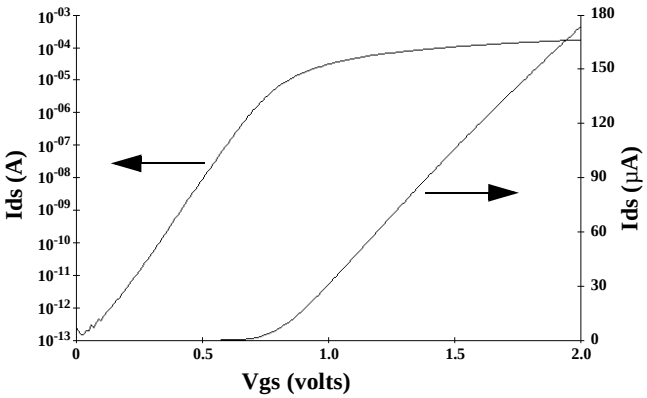
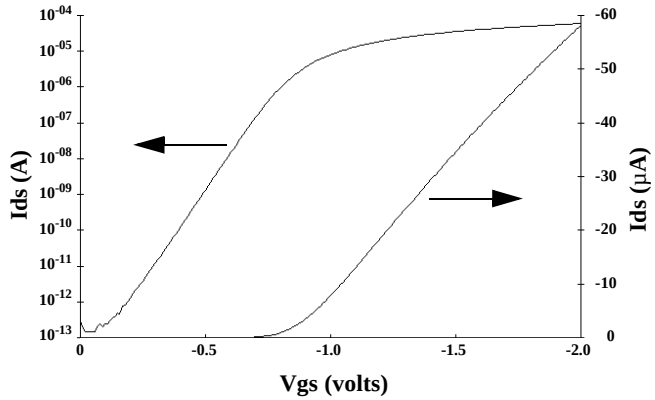



**FIG 4: Subthreshold Characteristics at Vds=-0.1 volts for a 50x2µm P-MOSFET (2µm 5 volts Process)**




Note: These values are for guidance only. Many of them can be adjusted to suit customer requirements.
For full process specifications contact a Dalsa Semiconductor sales office or representative.