Silicon diffused power transistors — BUT11; BUT11A

High-voltage, high-speed, glass-passivated npn power transistors in a TO-220 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

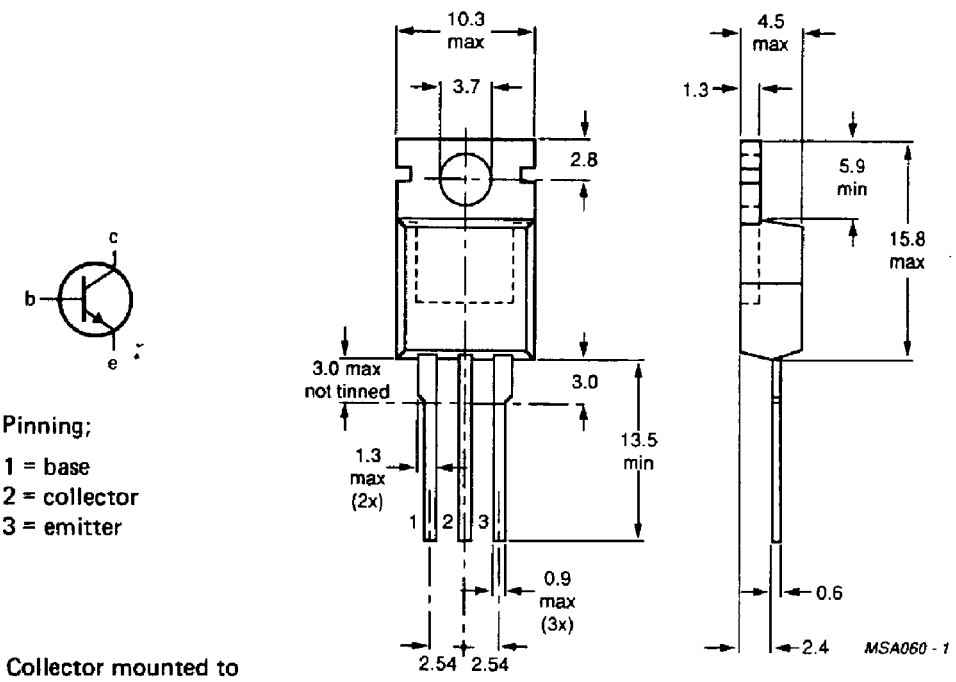
QUICK REFERENCE DATA

			BUT11	BUT11A	
Collector-emitter voltage (peak value; V_{BE} = 0)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector-emitter saturation voltage	V_{CEsat}	max.	1,5		V
Collector current (DC)	I_C	max.	5		A
Collector current (peak value)	I_{CM}	max.	10		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	100		W
Fall time	t_f	max.	0,8		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.



Pinning;

1 = base
2 = collector
3 = emitter

Collector mounted to mounting base.

Silicon diffused power transistors — BUT11; BUT11A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

			BUT11	BUT11A	
Collector-emitter voltage (peak value, V_{BE} = 0)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (DC)	I_C	max.	5		A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	10		A
Base current (DC)	I_B	max.	2		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	4		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	100		W
Storage temperature range	T_{stg}		−65 to + 150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,25	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current *					
$V_{CE} = V_{CESMmax}$; V_{BE} = 0	I_{CES}	max.	1		mA
$V_{CE} = V_{CESMmax}$; V_{BE} = 0; T_j = 125 °C	I_{CES}	max.	2		mA
Emitter cut-off current					
I_C = 0; V_{EB} = 9 V	I_{EBO}	max.	10		mA
Saturation voltages					
I_C = 3 A; I_B = 0,6 A	V_{CEsat}	max.	1,5	−	V
	V_{BEsat}	max.	1,3	−	V
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	max.	−	1,5	V
	V_{BEsat}	max.	−	1,3	V
Collector-emitter sustaining voltage					
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	min.	400	450	V
DC current gain					
I_C = 5 mA; V_{CE} = 5 V	h_{FE}	min.	10		
	h_{FE}	typ.	18		
	h_{FE}	max.	35		
I_C = 500 mA; V_{CE} = 5 V	h_{FE}	min.	10		
	h_{FE}	typ.	20		
	h_{FE}	max.	35		

* Measured with a half-sinewave voltage (curve tracer).

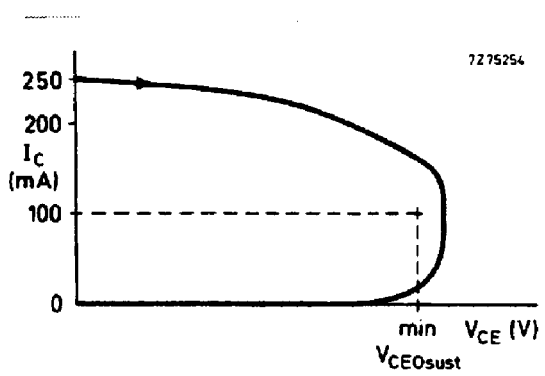


Fig. 2 Oscilloscope display for sustaining voltage.

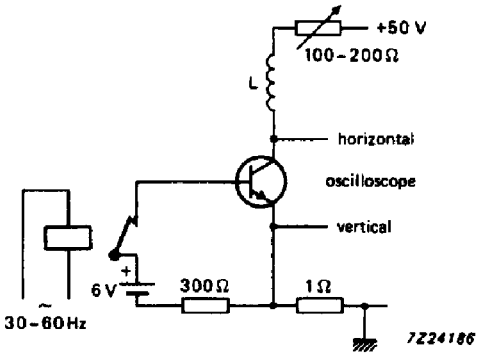
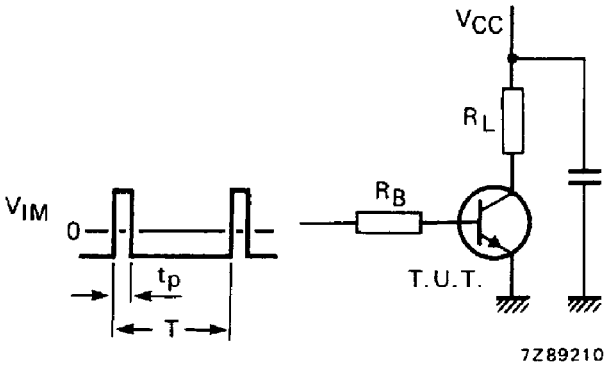


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUT11	BUT11A
Switching times resistive load (Figs 4 and 5)				
I_{Con} = 3 A; I_{Bon} = $-I_{Boff}$ = 0,6 A				
Turn-on time	t_{on}	max.	1	– µs
Turn-off: Storage time	t_s	max.	4	– µs
Fall time	t_f	max.	0,8	– µs
I_{Con} = 2,5 A; I_{Bon} = $-I_{Boff}$ = 0,5 A				
Turn-on time	t_{on}	max.	–	1 µs
Turn-off: Storage time	t_s	max.	–	4 µs
Fall time	t_f	max.	–	0,8 µs
Switching times inductive load (Figs 6 and 7)				
I_{Con} = 3 A; I_B = 0,6 A				
Turn-off: Storage time	t_s	typ.	1,1	– µs
		max.	1,4	– µs
Fall time	t_f	typ.	80	– ns
		max.	150	– ns
I_{Con} = 3 A; I_B = 0,6 A; T_j = 100 °C				
Turn-off: Storage time	t_s	typ.	1,2	– µs
		max.	1,5	– µs
Fall time	t_f	typ.	140	– ns
		max.	300	– ns
Switching times inductive load (Figs 6 and 7)				
I_{Con} = 2,5 A; I_B = 0,5 A				
Turn-off: Storage time	t_s	typ.	–	1,1 µs
		max.	–	1,4 µs
Fall time	t_f	typ.	–	80 ns
		max.	–	150 ns
I_{Con} = 2,5 A; I_B = 0,5 A; T_j = 100 °C				
Turn-off: Storage time	t_s	typ.	–	1,2 µs
		max.	–	1,5 µs
Fall time	t_f	typ.	–	140 ns
		max.	–	300 ns



V_{CC} = 250 V
V_{IM} = −6 to +8 V
$\frac{t_p}{T}$ = 0,01
t_p = 20 μs

The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

Fig. 4 Test circuit resistive load.

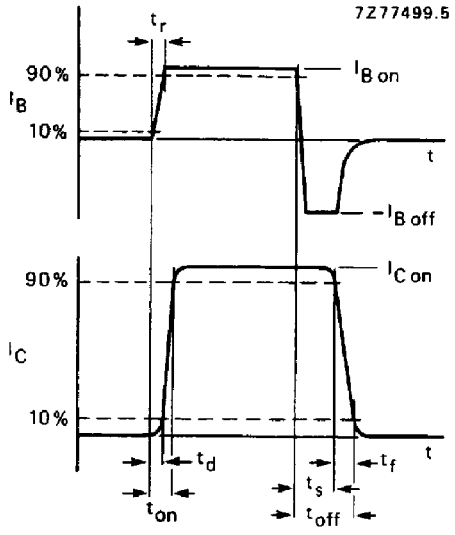


Fig. 5 Switching times waveforms with resistive load.

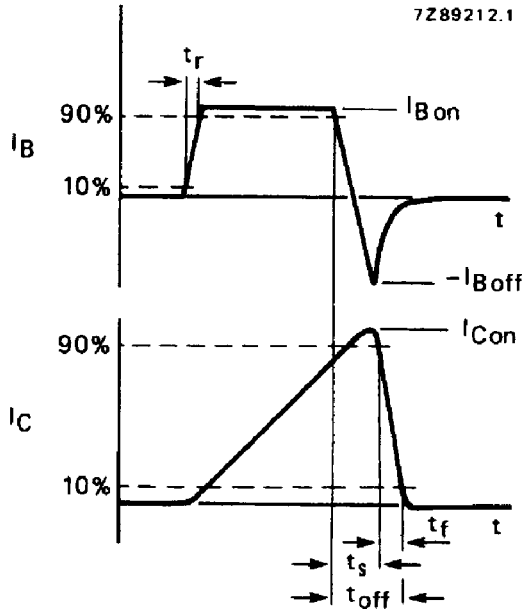
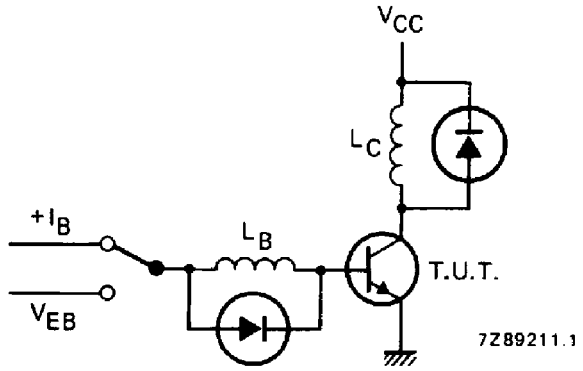
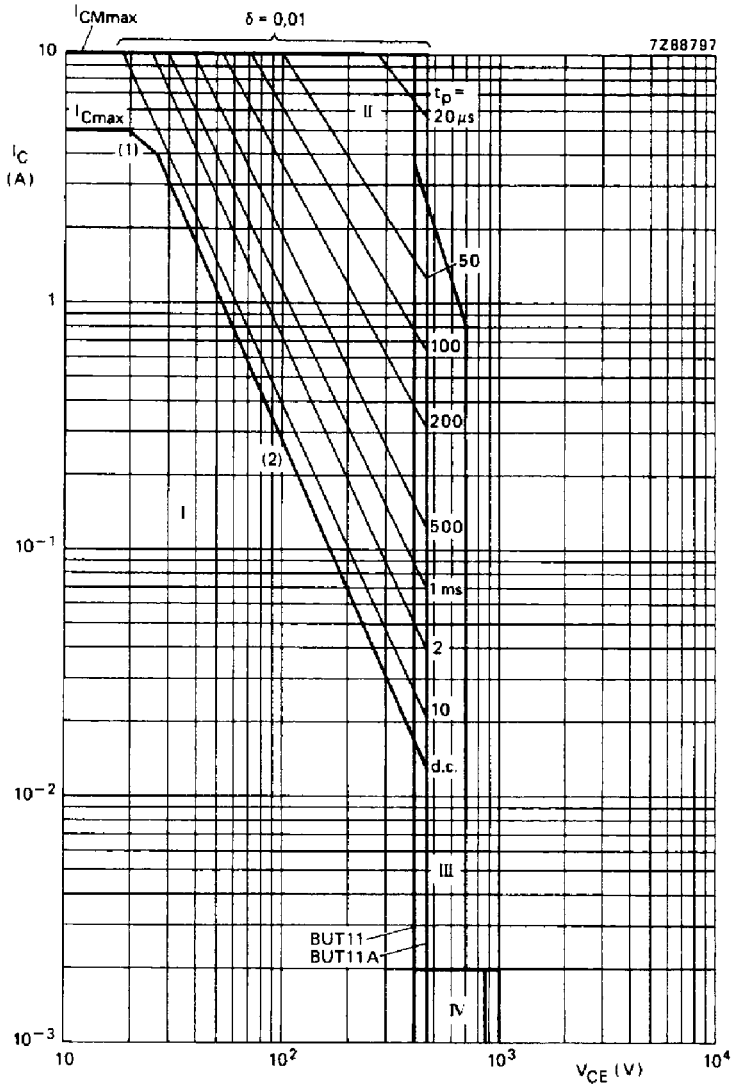


Fig. 6 Switching times waveforms with inductive load.



V_{CC} = 300 V
V_{EB} = 5 V
L_B = 1 μH

Fig. 7 Test circuit inductive load.



(1) $P_{tot\,max}$ and $P_{tot\,peak}$ max. lines.
(2) Second-breakdown limits

I Region of permissible DC operation
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0{,}6\ \mu s$.
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leqslant 0$ and $t_p \leqslant 5$ ms.

Fig. 8 Safe operating area at $T_{mb} \leqslant 25\ ^oC$.

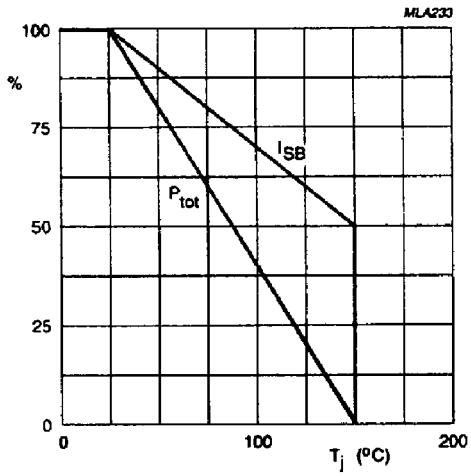


Fig. 9 Total power dissipation and second-breakdown current derating curve.

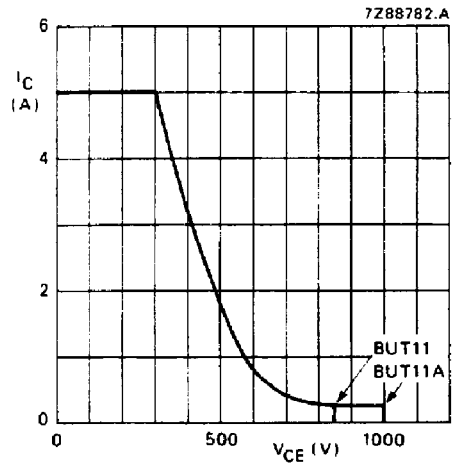


Fig. 10 Reverse bias SOAR.

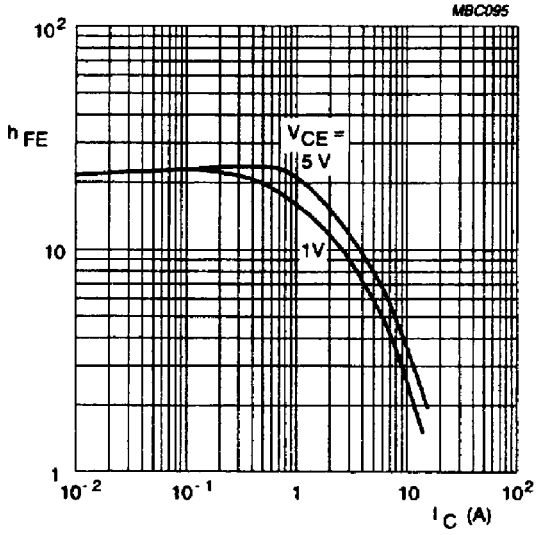


Fig.11 Typical DC current gain.

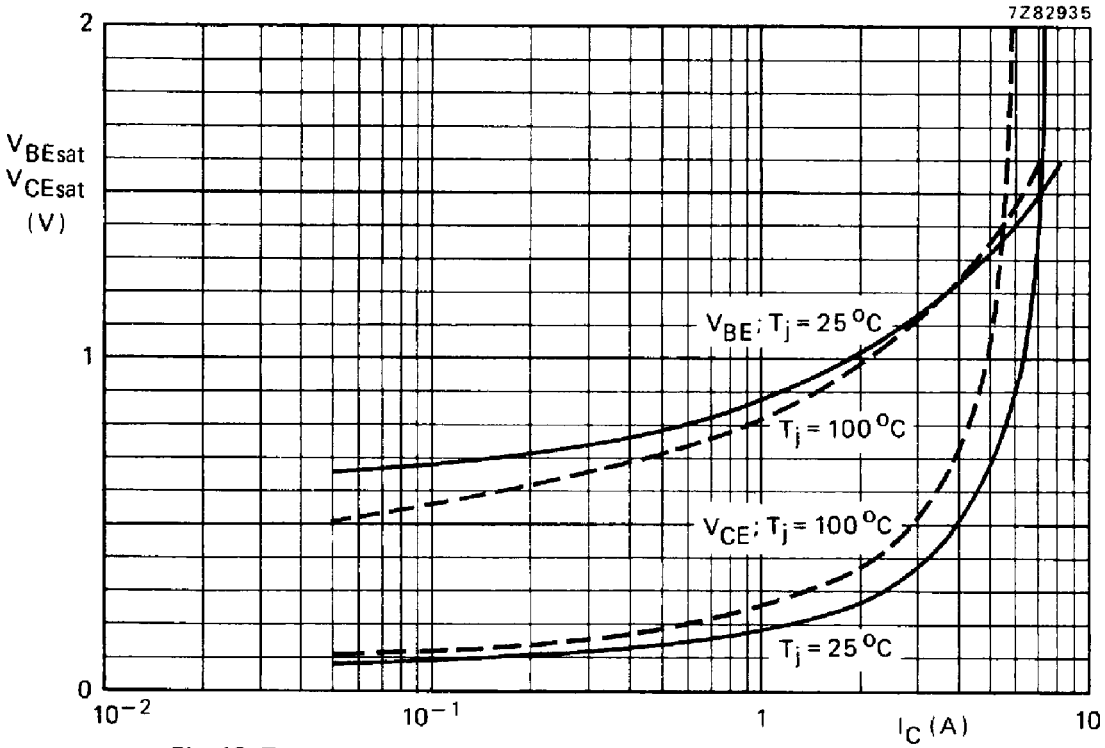


Fig. 12 Typical values base-emitter and collector-emitter voltage, $I_C/I_B = 5$.

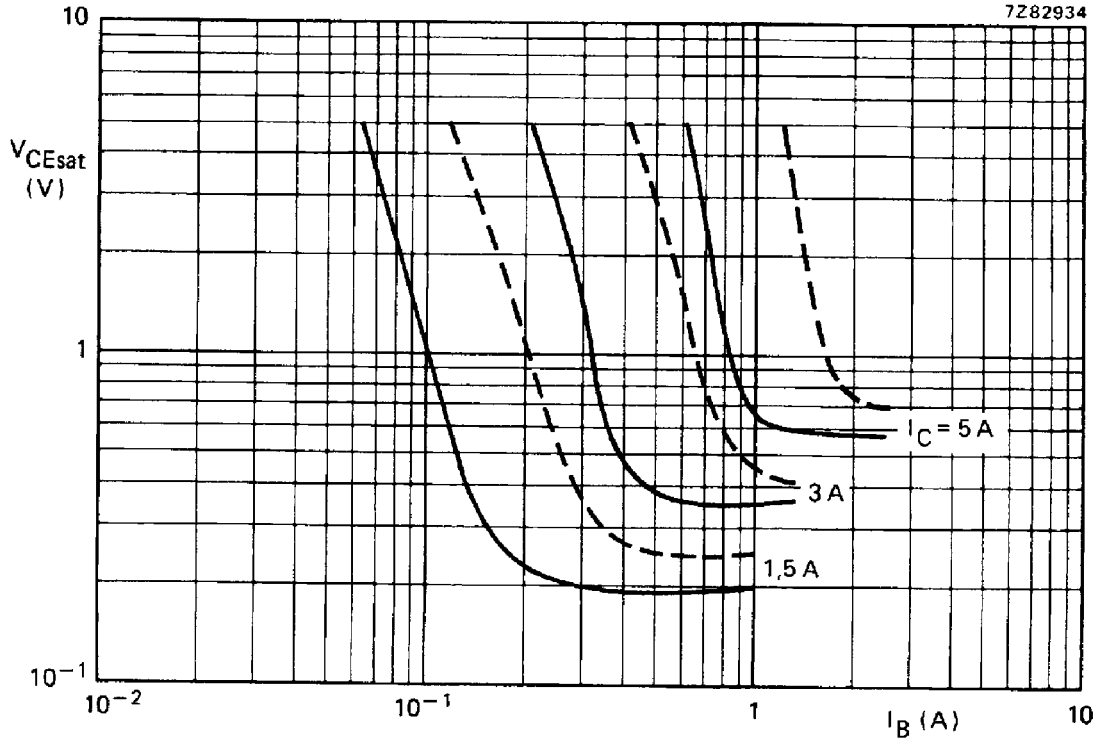


Fig. 13 Typ. (——) and max. (– – –) values collector-emitter saturation voltage at T_j = 25 °C.

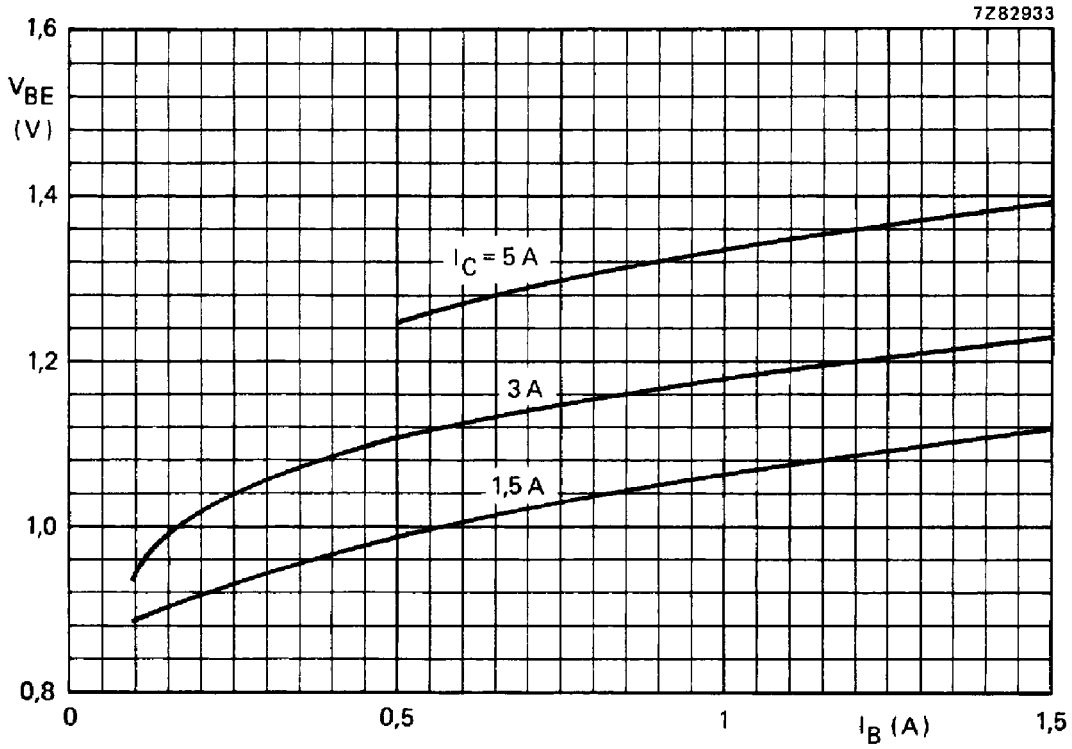


Fig. 14 Typical values at T_j = 25 °C.