NEC ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD6456

12 LINES×24 COLUMNS ON-SCREEN CHARACTER DISPLAY CMOS LSI FOR VCR CAMERA

DESCRIPTION

The μPD6456 is on-screen character display CMOS LSI which is combined with microcomputers and used for VCR CAMERA to display informations, date, tape counter, etc. on view finder.

Each character is in a 12 x 18 dots, and by combining two or more characters, Chinese characters (kanji) and graphics may be displayed.

μPD6456 can select out of two character signal output form. (mask code option)

In addition, thanks to its Power on reset function and Video RAM all reset command, the μPD6456 helps lighten a burden on the microcomputer.

NEC offers two types of devices μPD6456GS-101, μPD6456GS-102 and μPD6456GS-103 as standard products. These three products have the same character specifications and same package (16 pins SOP 300 mil), but the form of character signal output is as follows.

You can select Character output form from 3 types, and Display address from 2 types (Mask code option).

PART NUMBER	VC1, VBLK1 OUTPUT	VC2, VBLK2 OUTPUT	DISPLAY ADDRESS
μPD6456GS-101	Specified lines	Specified lines (except VC1, VBLK1 OUTPUT)	DISPLAY ADDRESS1
μPD6456GS-102	All lines	Specified lines	DISPLAY ADDRESS1
μPD6456GS-103	Specified columns	Specified columns	DISPLAY ADDRESS1

FEATURES

- Number of displayed character : 12 lines 24 columns
- Kinds of character : 128 (ROM)
- Character size : 1 dot/1H, 2H (Field)
- Character color : White
- Background : No background, black fringe, black squire background, or black solid background
- Dot matrix : 12 x 18 dots — with no clearance between neighboring characters
- Blinking ratio : 1:1, 3:1, or 1:3
- Character signal output : 2 form of character output
- Video RAM All release : It is possible to clear Video RAM by Power on reset function and Format specification command
- Interface with microcomputer : 8 bits serial input format
- Power supply : +5 V single power supply (Oscillation Frequency 4.0 to 6.0 MHz : +3 V)
- Structure : Low-power-consumption CMOS

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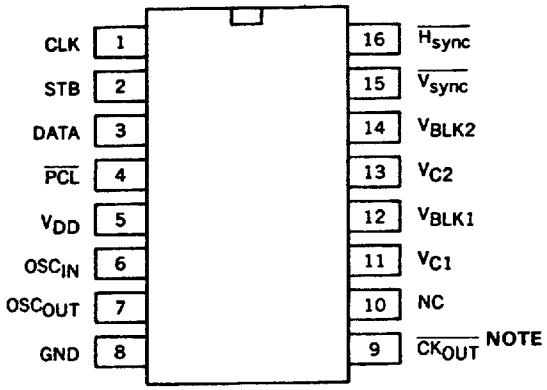
ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μPD6456GS-101	16-pin plastic SOP (300 mil)	Standard
μPD6456GS-102	16-pin plastic SOP (300 mil)	Standard
μPD6456GS-103	16-pin plastic SOP (300 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONNECTION DIAGRAM (Top View)



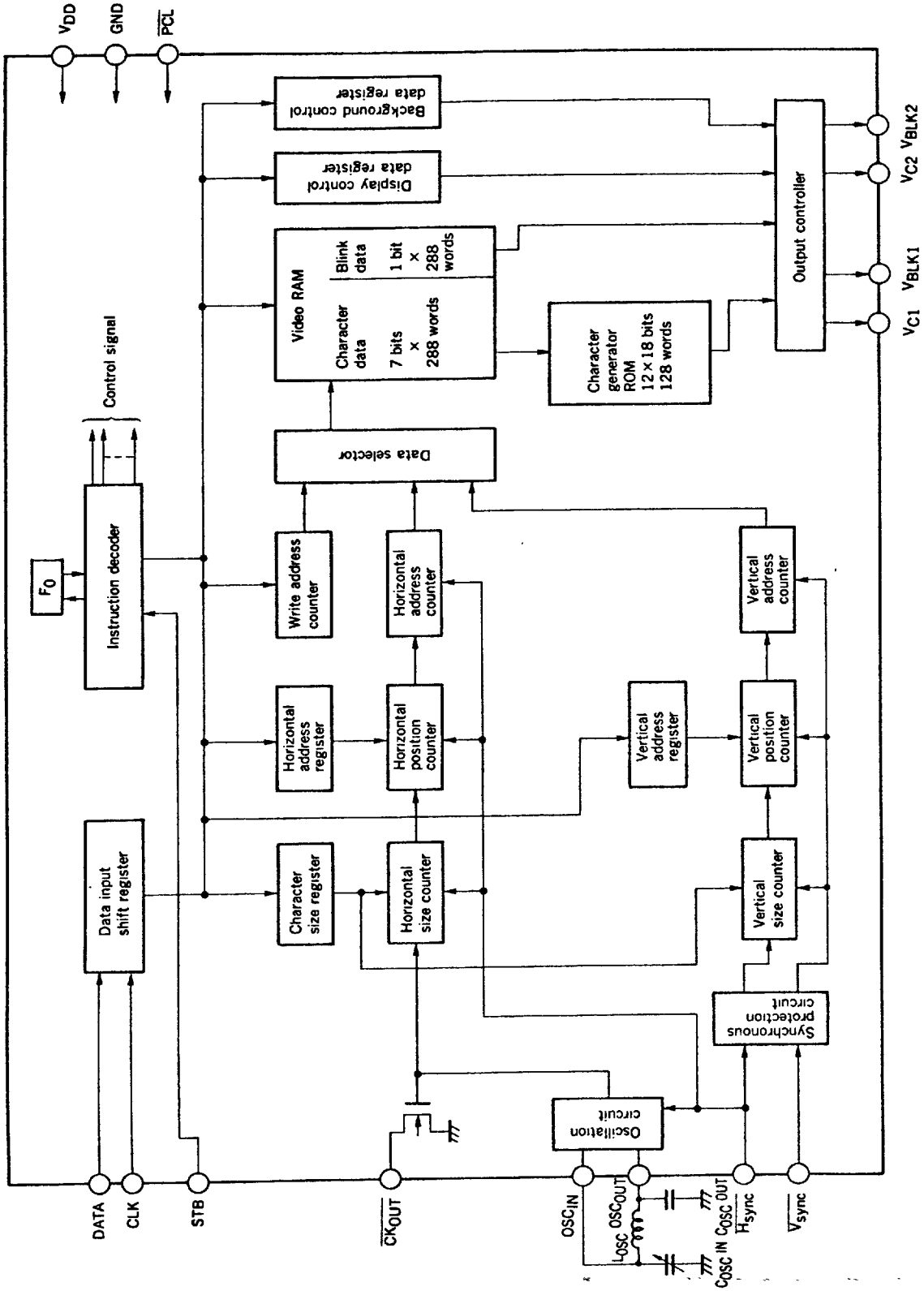
NOTE:

$\overline{CK_{OUT}}$: N-channel open drain output

PIN DESCRIPTION

No.	SYMBOL	PIN NAME	FUNCTION
1	CLK	Clock input terminal	This terminal is inputed the clock for reading data. At the rise of this clock, the data is inputed to the DATA terminal is read.
2	STB	Strobe input terminal	This terminal is inputed the strobe pulse after inputed of serial data. The 8 bits data is read at the rise of the strobe pulse inputed to the STB terminal. If the 8 bits data is a character, the data address is incremented by 1 at the fall of the strobe pulse.
3	DATA	Serial data input terminal	This terminal inputed the control data. It reads data synchronizing with the clock inputed to CLK terminal.
4	$\overline{PCL}$	Power on reset terminal	The state will be initialize by this terminal Low to High when power is ON.
5	V_{DD}	Power supply terminal	This terminal supplies +5 V power.
6 7	OSC_{IN} OSC_{OUT}	Oscillation terminal	These terminals are connected to the oscillation capacitor and coil.
8	GND	Grounding terminal	This terminals is connected to the system GND.
9	$\overline{CK_{OUT}}$	Clock output terminal	This terminal is used to frequency oscillation check. (N-channel open drain output)
10	NC	No connect	
11	V_{C1}	Character signal output terminal 1	This terminal outputs character signal. (active High)
12	V_{BLK1}	Blanking signal output terminal 1	This terminal outputs blanking signal correspond to the character signal (V_{C1}).
13	V_{C2}	Character signal output terminal 2	This terminal outputs character signal. (active High)
14	V_{BLK2}	Blanking signal output terminal 2	This terminal outputs blanking signal correspond to the character signal (V_{C2}).
15	$\overline{V_{sync}}$	Vertical synchronization signal input terminal	This terminal is inputed the vertical synchronization signal. Be sure to input this signal when active Low.
16	$\overline{H_{sync}}$	Horizontal synchronization signal input terminal	This terminal is inputed the horizontal synchronization signal. When this signal is high, oscillator oscillates is synchronizing with the rise of this signal. Be sure to input this signal when active low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply voltage	V_{DD}-V_{SS}	7	V
Input voltage	V_{IN}	V_{DD}+0.3 > V_{IN} > −0.3	V
Output voltage	V_{OUT}	V_{DD}+0.3 > V_{OUT} > −0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C
Output current	I_O	±5	mA

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3.0	5.0	5.5	V
Oscillation Frequency	f_{OSC}	V_{DD} = 4.5 V to 5.5 V	4.0		8.0	MHz
Oscillation Frequency	f_{OSC}	V_{DD} = 3.0 V to 4.5 V	4.0		6.0	MHz
Operating Temperature	T_{opt}		−20	+25	+75	°C

ELECTRICAL CHARACTERISTICS (T_a = −20 to +75 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply voltage	V_{DD}–V_{SS}	3.0	5.0	5.5	V	
Current consumption	I_{DD}			5.0	mA	f_{OSC} = 8.0 MHz, V_{DD} = 5.0 V
Control input high level voltage	V_{CIH}	2.4			V	V_{DD} = 5 V
Control input low level voltage	V_{CIL}			0.8	V	V_{DD} = 5 V
Synchronous signal input high level voltage	V_{ISH}	2.4			V	V_{DD} = 5 V
Synchronous signal input low level voltage	V_{ISL}			0.8	V	V_{DD} = 5 V
Signal output high level voltage	V_{OSH}	4.5			V	V_{DD} = 5 V, I_{OSH} = −1 mA
Signal output low level voltage	V_{OSL}			0.5	V	V_{DD} = 5 V, I_{OSL} = 1 mA
Clock output low level voltage	V_{OST}			0.5	V	V_{DD} = 5 V, I_{OST} = −0.1 mA

Control input : DATA, CLK, STB, $\overline{PCL}$
Synchronous signal input : $\overline{H_{sync}}$, $\overline{V_{sync}}$
Signal output : V_{C1}, V_{C2}, B_{LK1}, B_{LK2}
Clock output : $\overline{CK_{OUT}}$

COMMAND FORMAT

All the control commands are in 8-bits serial input format (input from MSB)

Before starting a program, transmit the format reset command by setting "FR=1" with the format specification command to release the test mode.

Each command is executed when a strobe pulse is input after 8-bits data have been input.

μPD6456GS-XXX COMMAND LIST

		(MSB)							(LSB)
CONTENT	F0	D7	D6	D5	D4	D3	D2	D1	D0
Display character data	0	0	C6	C5	C4	C3	C2	C1	C0
Blink data	0	1	0	0	0	BLNK	0	0	0
Character display line address	0	1	0	0	1	AR3	AR2	AR1	AR0
Character display column address	0	1	0	1	AC4	AC3	AC2	AC1	AC0
Background specification	0	1	1	0	BS4	BS3	0	0	0
Display ON/OFF, Blink, Oscillation	0	1	1	1	0	D0	BL2	BL1	OSC
Format specification	X	1	1	1	1	1	1	F0	FR
Display position vertical address*	1	0	1	0	V4	V3	V2	V1	V0
Display position horizontal address*	1	1	1	0	H4	H3	H2	H1	H0
Character signal output terminal*, character size specification	1	1	0	VC	S	AR3	AR2	AR1	AR0
Test mode setting[note]	1	1	1	1	0	T3	T2	T1	T0

*: μPD6456 can select out of three types. (mask code option)

note: Please don't set.

FORMAT SELECTION COMMAND

The commands of μPD6456 consist of 9-bits, but the shift registers for serial interfacing with external units consist of 8-bits. Therefore, instructions are divided into two banks. One of these banks is selected by 1 bit (F0) of the Format specification command.

- Commands of Bank 0
  - Display character data
  - Blink data
  - Character display line address
  - Character display column address
  - Background specification
  - Display ON/OFF, Blink, Oscillation
- Commands of Bank 1
  - Display position vertical address
  - Display position horizontal address
  - Character signal output terminal, character size specification

  Format specification command will be executed irrespective of Bank (0 or 1).

POWER ON RESET

At the time of power on, the internal states of this IC are indefinite (unknown). For this reason, be sure to perform the Power on reset function to set the IC to the initialized states by turning the voltage level of the PCL pin from Low to High. The commands to be set by this Power on reset function are as follows.

- Test mode is released.
- All the character data of video RAM are released to "7FH" (display off data).
- The line and column address values of the video RAM are set to "0".
- The character size specification is set to "1H" (normal size) with respect to all lines.
- Display is OFF, oscillation ON.
- BLINK DATA COMMAND: OFF

The time required for Power on reset can be obtained from the following express in.

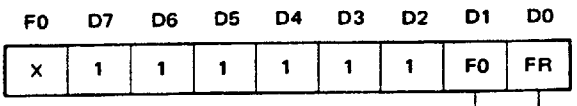
$t_1 = t_{PCLL}$* + The time required for video RAM all release
$= 10\ (\mu s) + 10\ (\mu s) + 12/f_{OSC}\ (MHz) \times 288$

* : Please refer to section of "Power ON reset" timing. (p. 23)

When without using Power ON reset function (PCL), the terminal PCL connects to V_{DD} and before starting the program, be sure to input the Format reset command ("FR = 1", set by the format specification command) to release the test mode. This command (Format reset) can set the same condition of Power ON reset.

During POWER ON RESET (t_1), please don't input commands for μPD6456.

FORMAT SPECIFICATION COMMAND



Format reset bit	
FR	Function
0	There is no change in the condition.
1	Format reset.

Bank selection bit	
F0	Function
0	Bank 0
1	Bank 1

FORMAT RESET

When the bit is set "FR = 1", the commands shown as follows are initialized. When the bit is set "FR = 0", there is no change in the condition.

The commands to be set by this Format reset bit (FR = 1) are as follows.

- Test mode is released.
- All the character data of video RAM are released to "7FH" (display off data).
- The line and column address values of the video RAM are set to "0".
- The character size specification is set to "1H" (normal size) with respect to all lines.
- Display is OFF, oscillation ON.
- BLINK DATA COMMAND: OFF

The time required for "video RAM all release" can be obtained from the following expression.

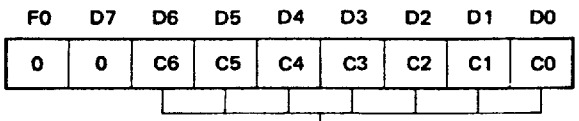
t_2 = The time required for video RAM all release
= 10 (μs) +12/f_{OSC} (MHz) x 288

During FORMAT RESET (t_2), please don't input commands for μPD6456.

- **Bank specification**

The commands of μPD6456 are devided two Banks. The Bank is specified by Bank selection bit.

DISPLAY CHARACTER DATA COMMAND



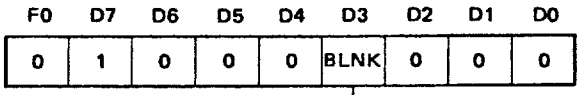
F0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	C6	C5	C4	C3	C2	C1	C0

Character specification bit							
C6	C5	C4	C3	C2	C1	C0	Function
0	0	0	0	0	0	0	Output the data for character code 00H.
⟆							⟆
1	1	1	1	1	1	1	Output the data for character code 7FH.

- **Character specification**

  The display character data (Character code) is written for video RAM.

BLINK DATA COMMAND



F0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	BLNK	0	0	0

Blink selection bit	
BLNK	Function
0	Blinking OFF
1	Blinking ON

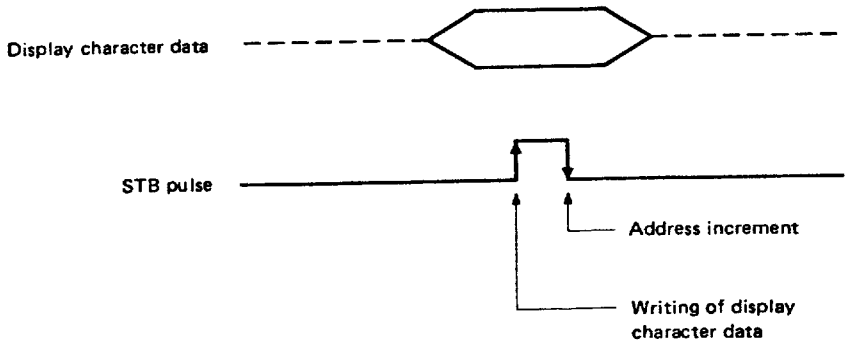
- **Blink selection for each character**

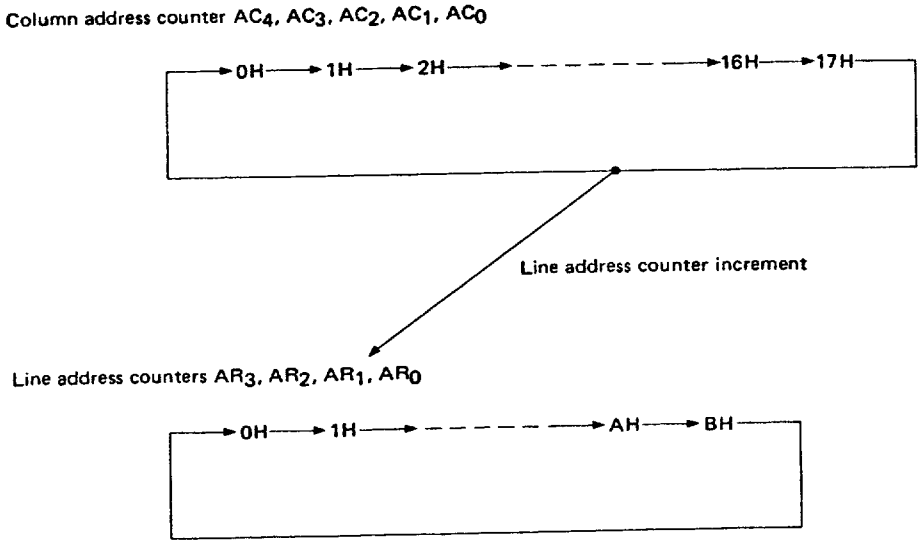
  It is possible to specificate the Blink data for each character. The Blink data is stored until the Blink data will be changed. This command is set to "Blinking OFF", by POWER ON RESET and FORMAT RESET.

WRITING OF DISPLAY CHARACTER DATA AND BLINK DATA FOR EACH CHARACTER

The write address for data can be directly set in the address counter by the character display line address command and the character display column address command.

After the write address is set, the Blink data for each character is input by the Blink data command. The Blink data for each character is saved in the internal register. Then, the display character data is input by the Display character data command. At the rise of the STB pulse (to be input at completion of the display character data command), the Blink data and Display character data, which are saved in the internal register, are written to the video RAM. The write address is incremented as shown below at the fall of the STB pulse when the Display character data is input. To write Display character data continuously without changing the Blink data for each character, just input the STB pulse.





CHARACTER DISPLAY LINE ADDRESS COMMAND

F0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	AR3	AR2	AR1	AR0

Line addressing bit				
AR3	AR2	AR1	AR0	Function
0	0	0	0	The 1st line is set.
0	0	0	1	The 2nd line is set.
⟆				⟆
1	0	1	1	The 12th line is set.

Do not set an address other than addresses 0H through BH.

- **Line addressing**

  Before the character data is written in the video RAM, this command specified the line address.

CHARACTER DISPLAY COLUMN ADDRESS COMMAND

F0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	AC4	AC3	AC2	AC1	AC0

Column addressing bit					
AC4	AC3	AC2	AC1	AC0	Function
0	0	0	0	0	The 1st column is set.
0	0	0	0	1	The 2nd column is set.
⟆					⟆
1	0	1	1	1	The 24th column is set.

Do not set an address other than addresses 0H through 17H.

- **Column addressing**

  Before the character data is written in the video RAM, this command specified the column address.

Character Display

The number of characters displayed is 12 lines x 24 columns; that is, 288 as shown below.

$AC_4.AC_3.AC_2.AC_1.AC_0$	00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011	01100	01101	01110	01111	10000	10001	10010	10011	10100	10101	10110	10111
$AR_3 AR_2 AR_1 AR_0$ 0000																								
0001																								
0010																								
0011																								
0100																								
0101																								
0110																								
0111																								
1000																								
1001																								
1010																								
1011																								

BACKGROUND SPECIFICATION COMMAND

F0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	BS4	BS3	0	0	0

Background specification bit		
BS4	BS3	Function
0	0	No background
0	1	Black fringe
1	0	Black square background
1	1	Black solid background

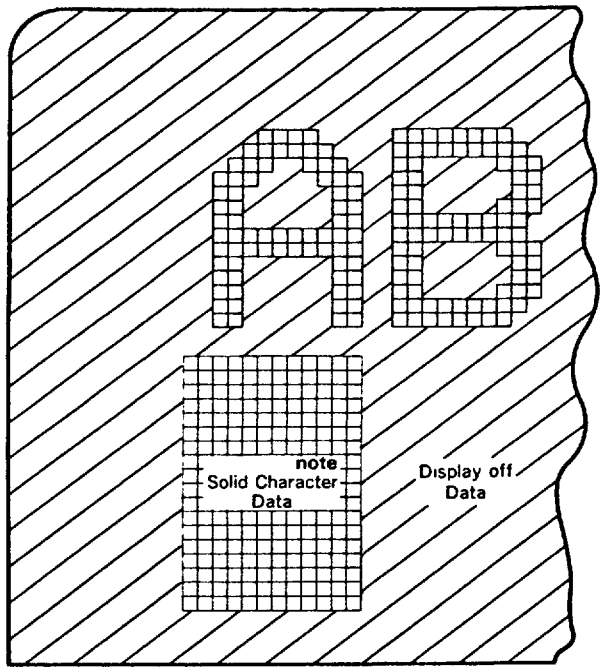
- **Background specification**

The background can be selected for each screen image from no-background, black fringe, black square background, and black solid background by Background specification command.

No-background : Only character data are outputed.
Black fringe : Character are trimmed with 1 dot-minimum character (1 H/1 dot).
Black square background : The 12 line x 24 column block display characters has black background.
Black solid background : The video signal is totally omitted and whole screen has black background.

Display format in Each Background Mode

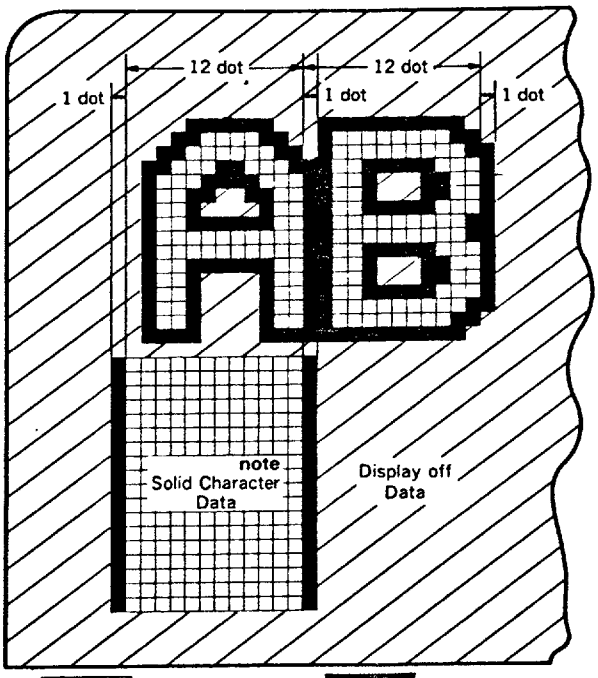
No background



Character color

Picture

Fringe

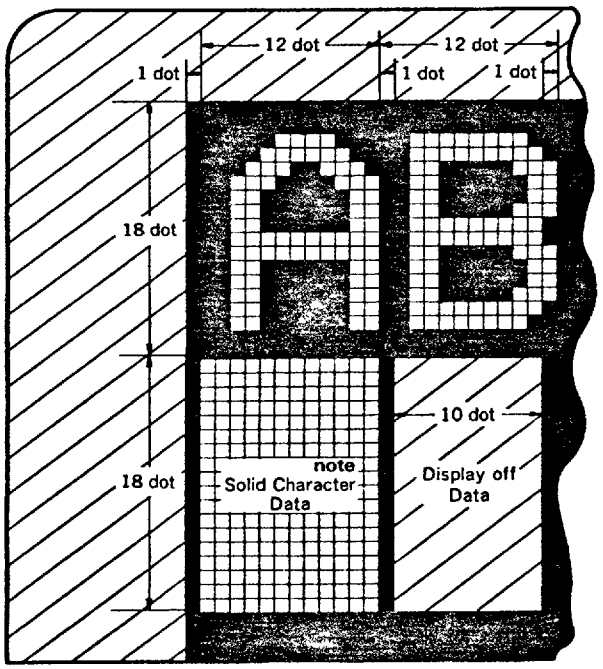


Character color

Fringe (Black)

Picture

Square background + Fringe

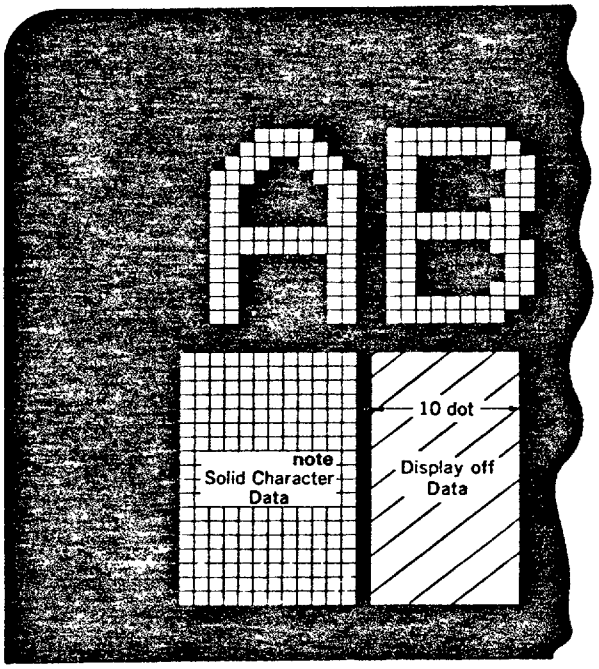


Character color

Background color (Black)

Picture

Solid background + Fringe



Character color

Background color (Black)

Picture

Note: The solid character data means the data of character code 1 E_H (Standard type of NEC).

1. No background

Only characters are displayed.

2. Black fringe

Characters with black fringe are displayed. Black fringe of a character which is used the edge of dot-matrix (right and left) is displayed in neighbor character area for 1 dot.

The fringe is the dot of the smallest character size and irrespective of character size.

3. Black square background

The black square background is displayed in character display area.

In this case, the background is displayed in outside of character display area (right and left) for 1 dot.

In case of using "Display OFF data", the background is displayed in the inside edge of "Display OFF data" for 1 dot.

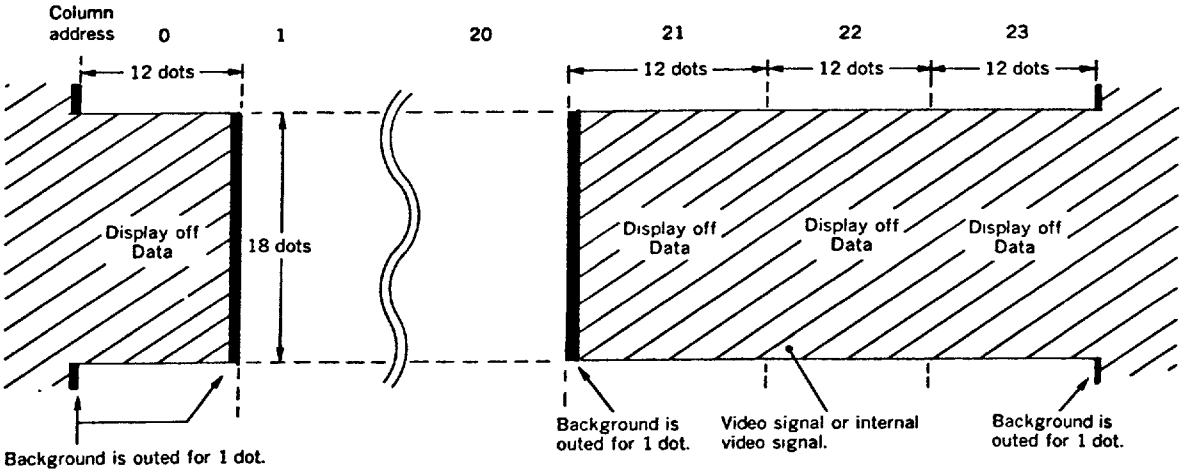
4. Black solid background

The black solid background is displayed in the all area of screen.

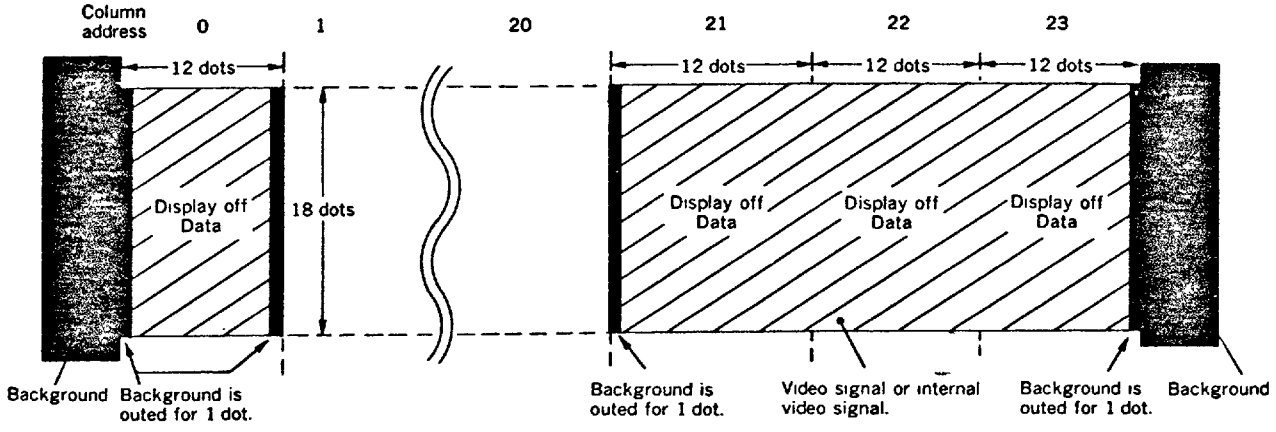
In case of using "Display OFF data", the background is displayed in the inside edge of "Display OFF data" for 1 dot.

In case of using "Display OFF data".

○ Black square background



○ Black solid background



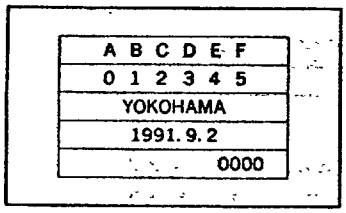
Note: The "1 dot" is the dot of the smallest character size and irrespective of character size.

BACKGROUND OUTPUT

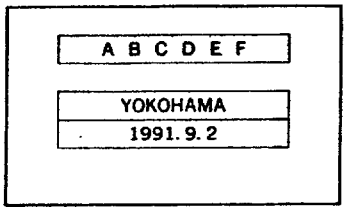
The background is outputed as follows. Please don't set solid background at mask option "C".

- **An image of background output at mask option "A".**
  - ○ Balack square background

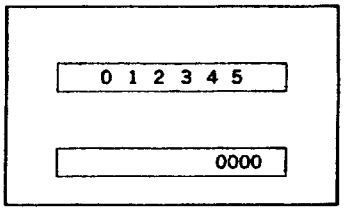
View-finder



V_{C1} output (Character signal)
V_{C2} output (Blanking signal)

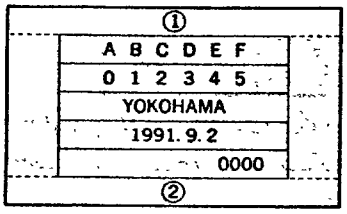


V_{C1} output (Character signal)
V_{C2} output (Blanking signal)

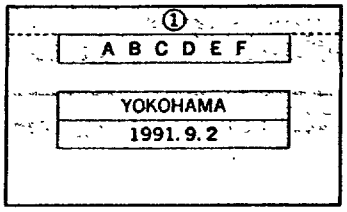


  - ○ Black solid background

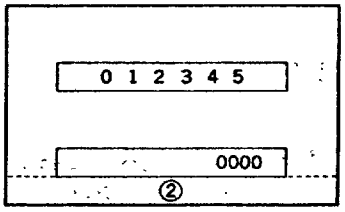
View-finder



V_{C1} output (Character signal)
V_{C2} output (Blanking signal)



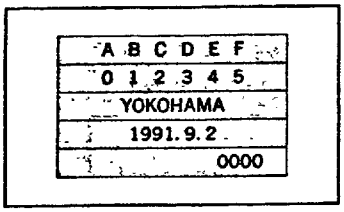
V_{C1} output (Character signal)
V_{C2} output (Blanking signal)



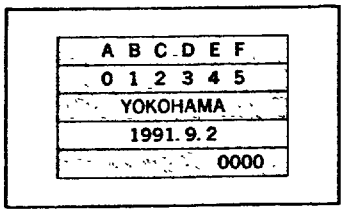
The part of ① (The upper part of display area) is outputed at V_{C1} when the Line 1 is specified output terminal V_{C1} (When the Line 1 is specified output terminal V_{C2}, The part of ① is outputed at V_{C2}.) and the part of ② (The lower part of display area) is outputed at V_{C2} when the Line 12 is specified output terminal V_{C2}. (When the Line 12 is specified output terminal V_{C1}, The part of ② is outputed at V_{C1}.)

- **An image of background output at mask option "B".**
  - ○ Balack square background

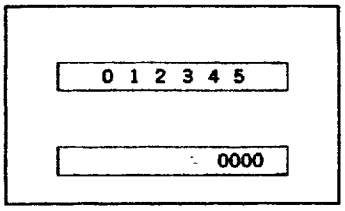
View-finder



V_{C1} output (Character signal)
V_{C2} output (Blanking signal)

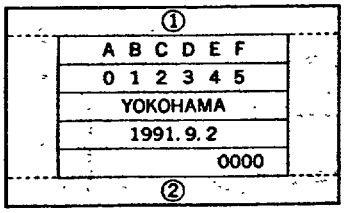


V_{C1} output (Character signal)
V_{C2} output (Blanking signal)

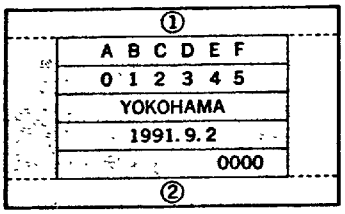


  - ○ Black solid background

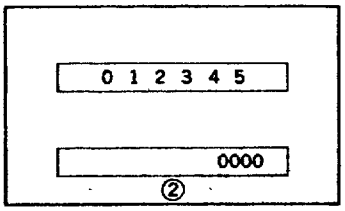
View-finder



V_{C1} output (Character signal)
V_{C2} output (Blanking signal)



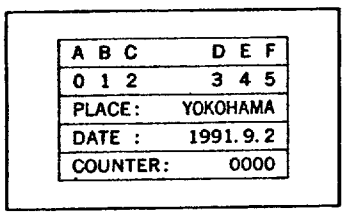
V_{C1} output (Character signal)
V_{C2} output (Blanking signal)



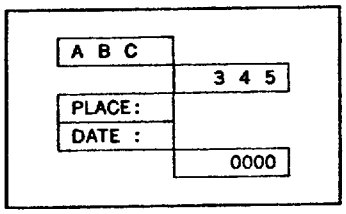
The part of ① (The upper part of display area) is outputed at V_{C2} when the Line 1 is specified to output at V_{C2} and the part of ② (The lower part of display area) is outputed at V_{C2} when the Line 12 is specified to output at V_{C2}. (V_{C1} outputs all character and all background.)

- **An image of background output at mask option "B".**
  - ○ Balack square background

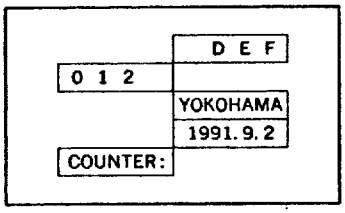
View-finder



V_{C1} output (Character signal)
V_{C2} output (Blanking signal)



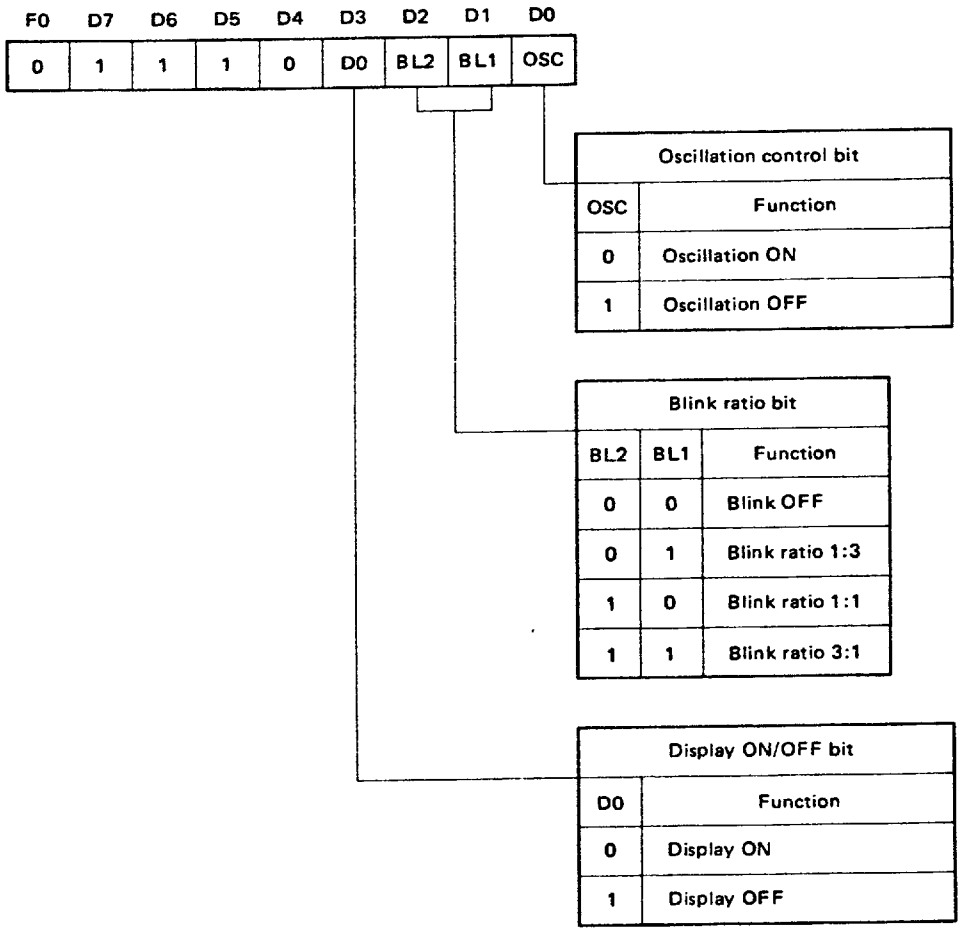
V_{C1} output (Character signal)
V_{C2} output (Blanking signal)



  - ○ Black solid background: Please don't set.

Note: These displays are images, so display area isn't 12 lines x 24 columns.

DISPLAY ON/OFF, BLINK, OSCILLATION COMMAND



F0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	D0	BL2	BL1	OSC

Oscillation control bit	
OSC	Function
0	Oscillation ON
1	Oscillation OFF

Blink ratio bit		
BL2	BL1	Function
0	0	Blink OFF
0	1	Blink ratio 1:3
1	0	Blink ratio 1:1
1	1	Blink ratio 3:1

Display ON/OFF bit	
D0	Function
0	Display ON
1	Display OFF

- **Oscillation control**

Since the μPD6456 enables control of LC oscillation with Display ON/OFF, Blink, Oscillation command, oscillation can be suspended while characters are not displayed, so that power can be saved. Since character output is not reliable after suspension of oscillation, set the Display ON/OFF bit (D0) to "0" (display OFF).

Note: When display is ON, the oscillation synchronizes $\overline{H_{sync}}$, so the oscillation is stopping at the low level term of $\overline{H_{sync}}$.
When display is OFF, the oscillation keeps on irrespective of $\overline{H_{sync}}$.

- **Blink ratio control**

The μPD6456 enables blinking for each character with Display ON/OFF, Blink, Oscillation command. Blinking characters are determined with the Blink data command. The blinking period is about 1 second (64 times longer than 1 vertical cycle), and three blinking ratios (1:3, 1:1, 3:1) are available.

- **Display ON/OFF**

The display can be partially turned off with blank data or display off data. The total display turned off with Display ON/OFF, Blink, Oscillation command. When display OFF is set with this command, characters and backgrounds are not outputed. Display ON and OFF synchronize with $\overline{H_{sync}}$.

It is possible to select the DISPLAY ADDRESS from 2 types (DISPLAY ADDRESS 1 or DISPLAY ADDRESS 2). (MASK CODE OPTION)

- **DISPLAY POSITION 1**

DISPLAY POSITION VERTICAL ADDRESS COMMAND

F0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	V_4	V_3	V_2	V_1	V_0

Vertical address bit					
V_4	V_3	V_2	V_1	V_0	Function
0	0	0	0	0	From the rising edge of $\overline{V_{sync}}$. 1 H + 1 H x 0
0	0	0	0	1	From the rising edge of $\overline{V_{sync}}$. 1 H + 1 H x 1
⟆					⟆
1	1	1	1	1	From the rising edge of $\overline{V_{sync}}$. 1 H + 1 H x 31

- **Vertical address**

  It is possible to set the display position vertical address 32 steps (1 H/step).

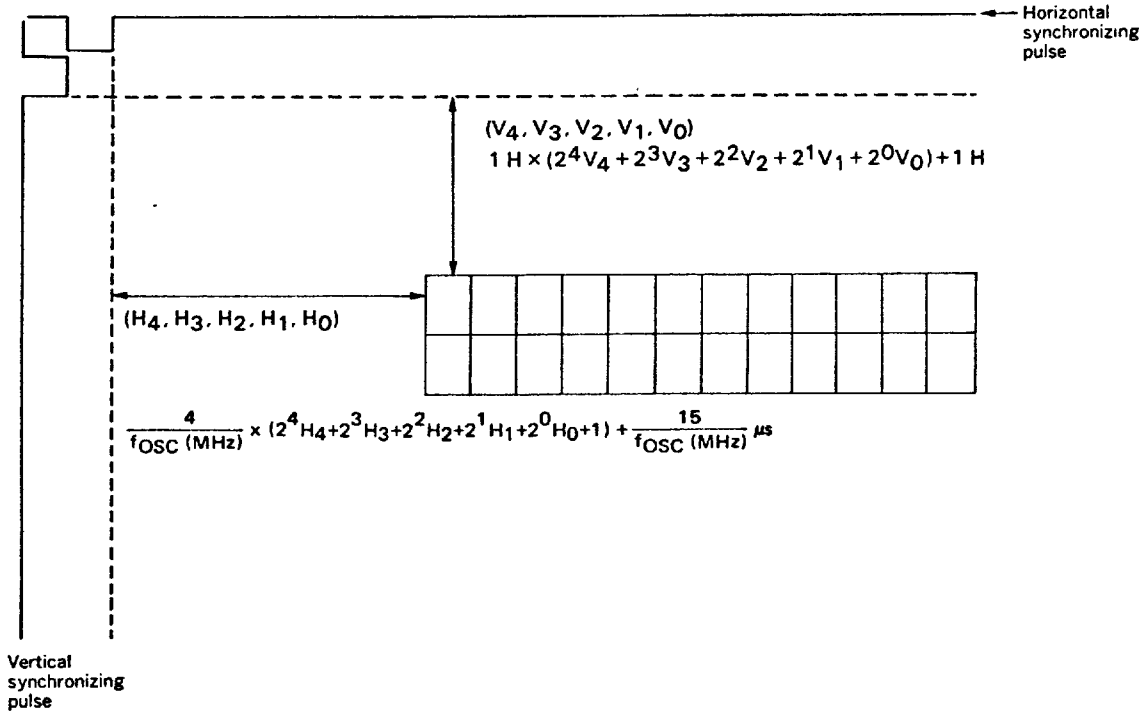
DISPLAY POSITION HORIZONTAL ADDRESS COMMAND

F0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	H_4	H_3	H_2	H_1	H_0

Horizontal address bit					
H_4	H_3	H_2	H_1	H_0	Function
0	0	0	0	0	From the rising edge of $\overline{H_{sync.}}$ $4/f_{OSC}$ (MHz) x 1 + $\frac{15}{f_{OSC}\ (MHz)}$ (μs)
0	0	0	0	1	From the rising edge of $\overline{H_{sync.}}$ $4/f_{OSC}$ (MHz) x 2 + $\frac{15}{f_{OSC}\ (MHz)}$ (μs)
⟆					⟆
1	1	1	1	1	From the rising edge of $\overline{H_{sync.}}$ $4/f_{OSC}$ (MHz) x 32 + $\frac{15}{f_{OSC}\ (MHz)}$ (μs)

- **Horizontal address**

  It is possible to set the display position vertical address 32 steps (4 dots/step).



- **DISPLAY POSITION 2**

DISPLAY POSITION VERTICAL ADDRESS COMMAND

F0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	V_4	V_3	V_2	V_1	V_0

Vertical address bit					
V_4	V_3	V_2	V_1	V_0	Function
0	0	0	0	0	From the rising edge of $\overline{V_{sync}}$, 1 H + 9 H × 0
0	0	0	0	1	From the rising edge of $\overline{V_{sync}}$, 1 H + 9 H × 1
			⌇		⌇
1	1	1	1	1	From the rising edge of $\overline{V_{sync}}$, 1 H + 9 H × 31

- **Vertical address**

  It is possible to set the display position vertical address 32 steps (9 H/step).

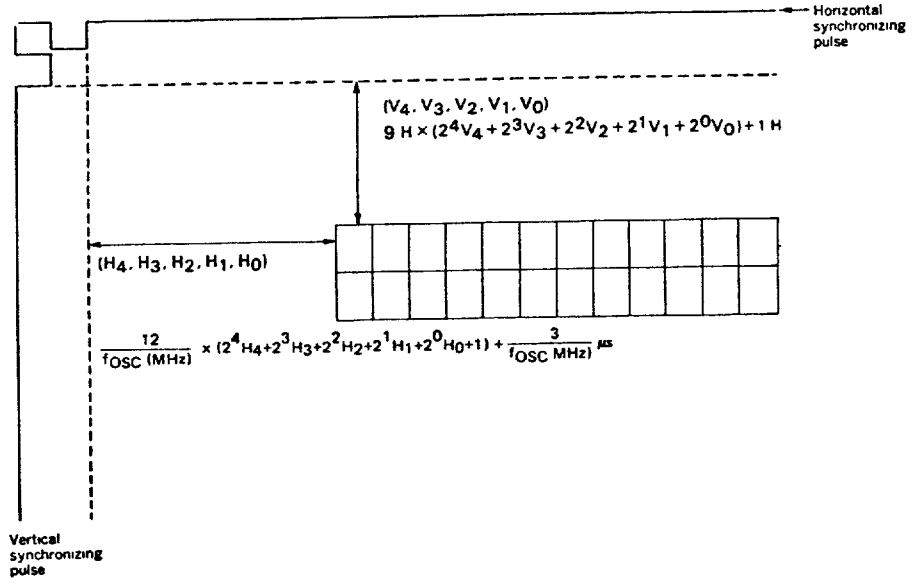
DISPLAY POSITION HORIZONTAL ADDRESS COMMAND

F0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	H_4	H_3	H_2	H_1	H_0

Horizontal address bit					
H_4	H_3	H_2	H_1	H_0	Function
0	0	0	0	0	From the rising edge of H_{sync}, $12/f_{OSC\ (MHz)} \times 1 + \frac{3}{f_{OSC\ (MHz)}}$ (μs)
0	0	0	0	1	From the rising edge of H_{sync}, $12/f_{OSC\ (MHz)} \times 2 + \frac{3}{f_{OSC\ (MHz)}}$ (μs)
			⌇		⌇
1	1	1	1	1	From the rising edge of H_{sync}, $12/f_{OSC\ (MHz)} \times 32 + \frac{3}{f_{OSC\ (MHz)}}$ (μs)

- **Horizontal address**

  It is possible to set the display position vertical address 32 steps (12 dots/step).



CHARACTER SIGNAL OUTPUT TERMINAL, CHARACTER SIZE SPECIFICATION COMMAND

F0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	V_C	S	AR_3	AR_2	AR_1	AR_0

Line address bit				
AR_3	AR_2	AR_1	AR_0	Function
0	0	0	0	The 1st line is set.
0	0	0	1	The 2nd line is set.
}				}
1	0	1	1	The 12th line is set.

Do not set an address other than addresses 0_H throuth B_H.

Character size bit	
S	Function
0	V: 1 H/DOT, H: 1 t dot
1	V: 2 H/DOT, H: 2 t dot

$$t\ dot = \frac{1}{f_{OSC}\ (MHz)}\ \mu s$$

***Mask option A**

Output terminal selection bit	
V_C	Function
0	V_{C1}: All lines, V_{C2}: Low
1	V_{C1}: Low, V_{C2}: Specified lines

***Mask option B**

Output terminal selection bit	
V_C	Function
0	V_{C1}: All lines, V_{C2}: Low
1	V_{C1}: All lines, V_{C2}: Specified line

F0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	V_{C1}	V_{C2}	AR_3	AR_2	AR_1	AR_0

Line address bit

***Mask option C (All character sizes are fixed smallest size.)**

Output terminal selection bit		
V_{C1}	V_{C2}	Function
0	0	V_{C1}: 1~12 Columns, V_{C2}: Low
0	1	V_{C1}: 1~12 Columns, V_{C2}: 13~24 Columns
1	0	V_{C1}: 13~24 Columns, V_{C2}: 1~12 Columns
1	1	V_{C1}: Low, V_{C2}: 1~24 Columns

*The μPD6456 can select out of three character signal output form. (Mask code option)—

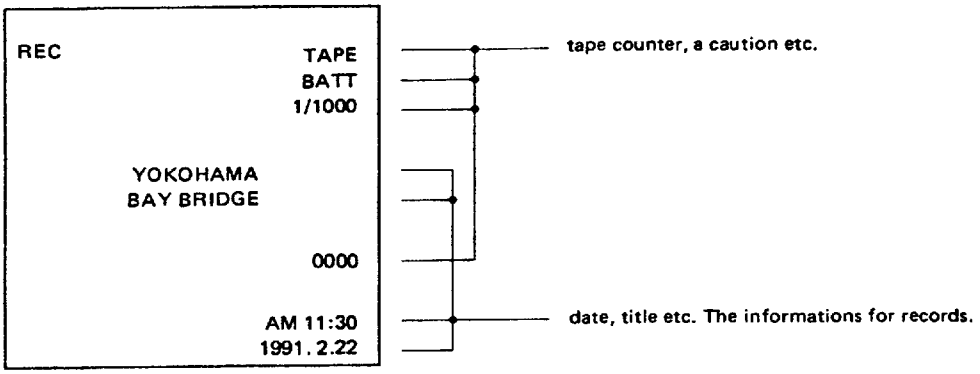
MASK CODE OPTION

When used in a VCR camera, the on-screen ICs provide two types of information; information to be recorded on VCR tape, such as the date and title, and information to be displayed only inside the viewfinder, such as the battery, focus, sensitivity, and mode.

So μPD6456 enable to select of three character signal output form by mask code options. (as follows)

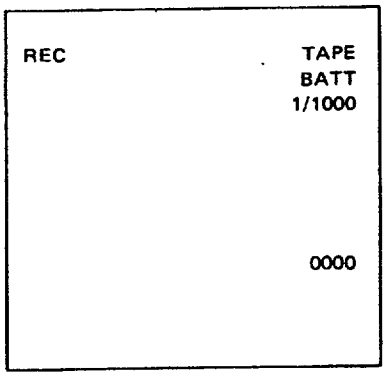
○ **Mask code option A**

An display example of the view finder.

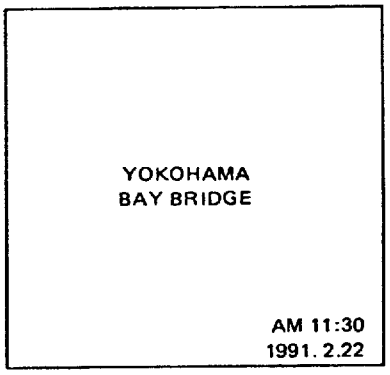


An example of Mask code option A

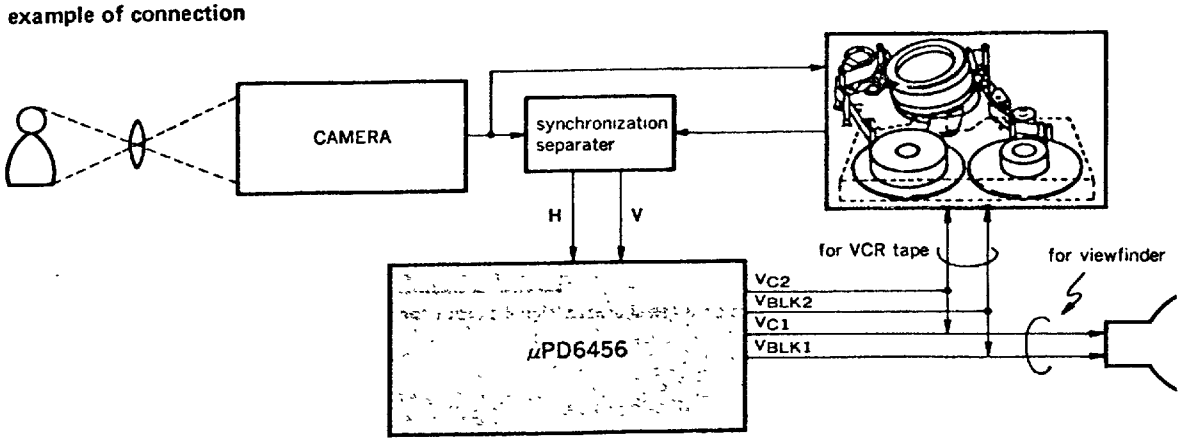
Output of V_{C1} (the lines of V_C = 0)



Output of V_{C2} (the lines of V_C = 1)

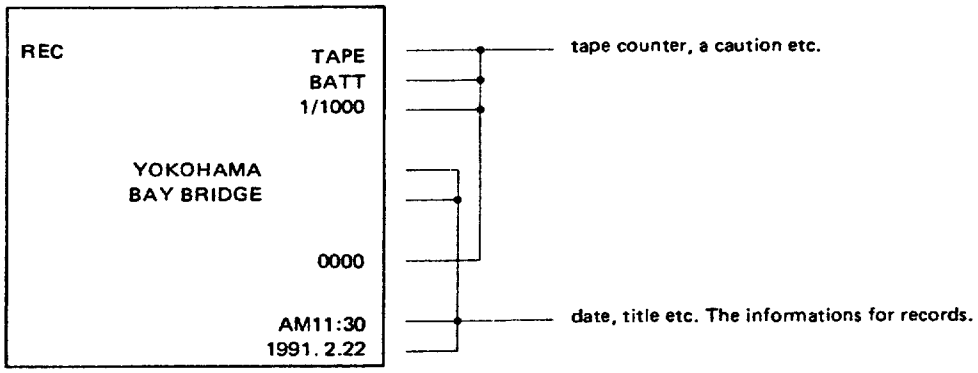


○ **An example of connection**



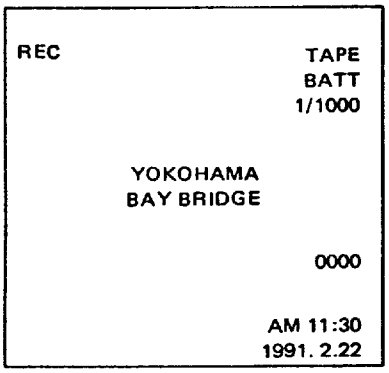
○ **Mask code option B**

An display example of the view finder.

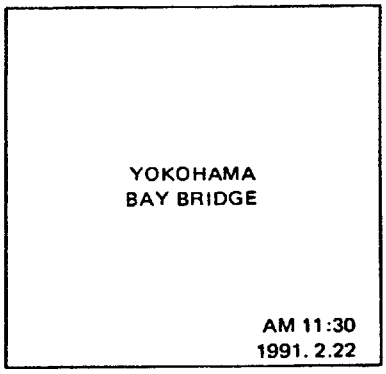


An example of Mask code option B

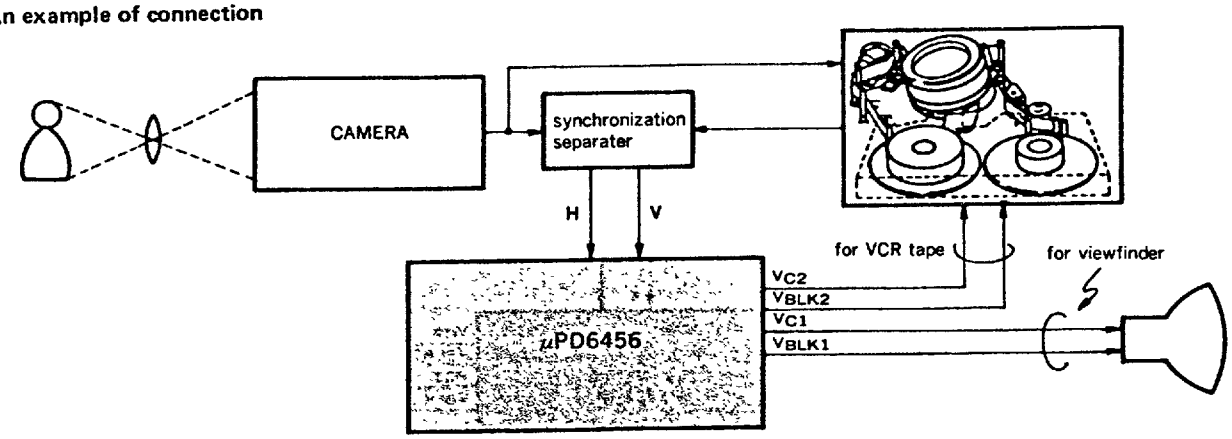
Output of V_{C1} (all lines)



Output of V_{C2} (the lines of V_C = 1)



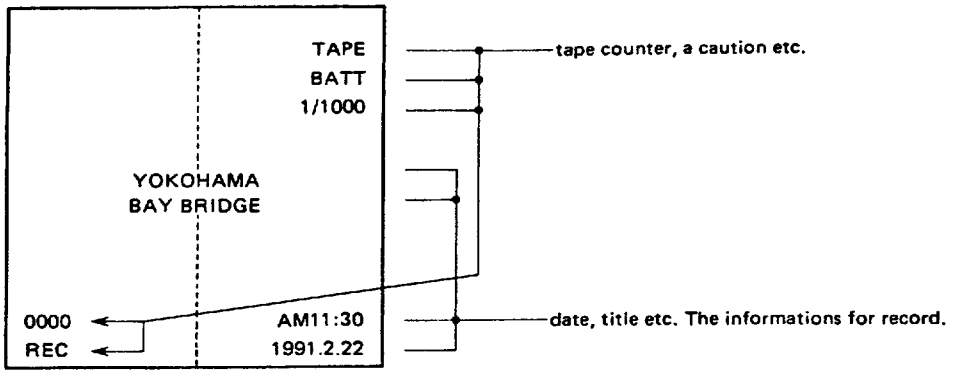
○ **An example of connection**



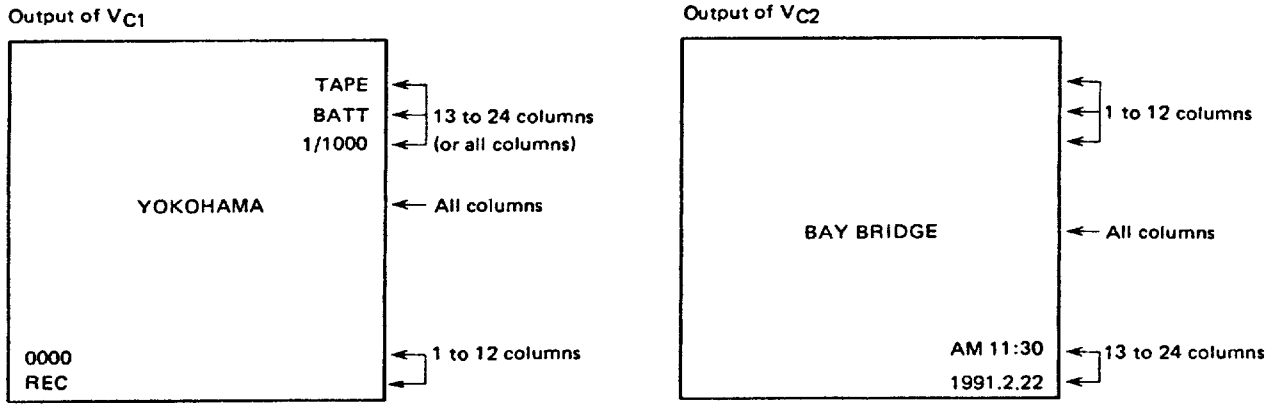
○ **Mask code option C**

μPD6456 can output character signal, a line devide into 1 to 12 columns and 12 to 24 columns.

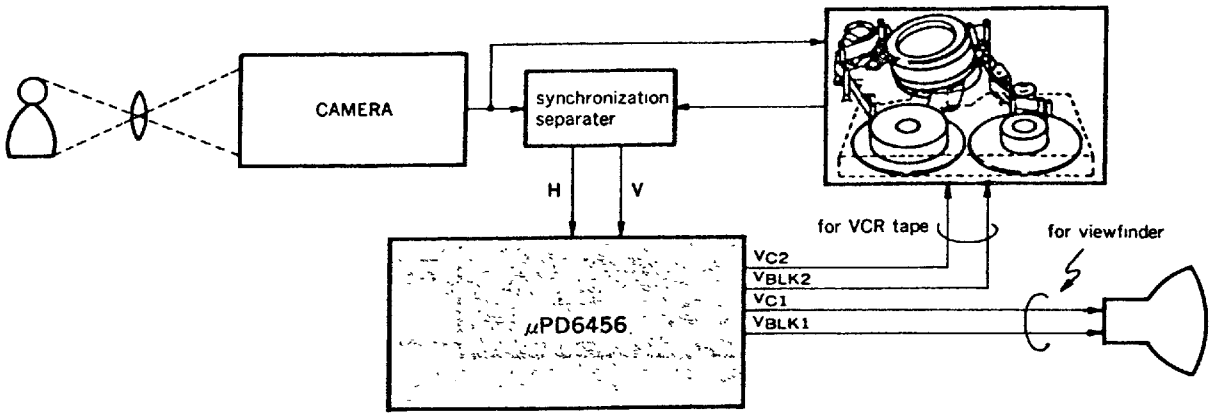
An display example of the view finder.



An example of Mask code option C



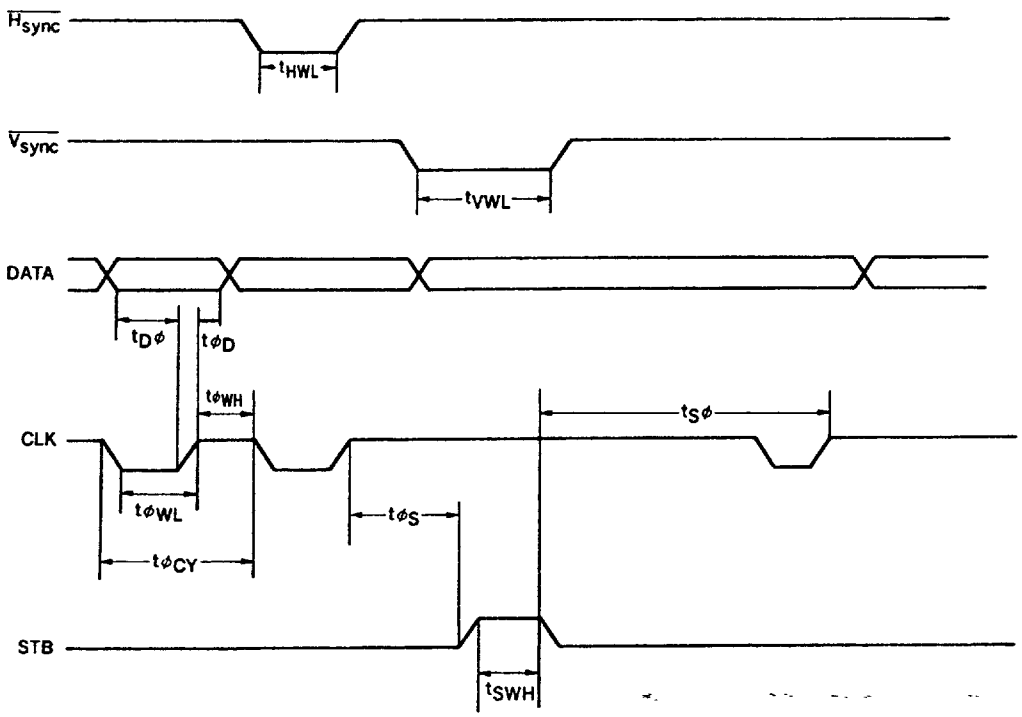
○ **An example of connection**



RECOMMENDED CONDITIONS FOR OPERATION TIMING (T_a = −20 to +75 °C, V_{DD} = 4.5 to 5.5 V)

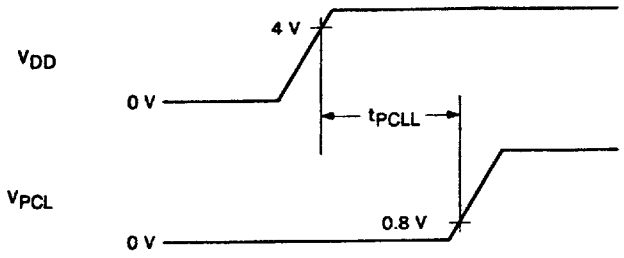
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Minimum setup time	$t_{D\phi}$	200			ns	
Minimum hold time	$t_{\phi D}$	200			ns	
Minimum clock width at low level	$t_{\phi WL}$	700			ns	
Minimum clock width at high level	$t_{\phi WH}$	700			ns	
Minimum clock to strobe time	$t_{\phi S}$	400			ns	
Minimum strobe width at high level	t_{SWH}	1			μs	
Minimum strobe to clock time	$t_{S\phi}$	$t_{HWL} + \frac{25}{f_{OSC}} \times S$			μs	Display ON, VRAM write command
		1				another
		$\frac{12}{f_{OSC}} \times S$				Display OFF
Minimum strobe to strobe time*	t_S	$t_{HWL} + \frac{25}{f_{OSC}} \times S$			μs	Display ON, VRAM write command
		1				another
		$\frac{12}{f_{OSC}} \times S$				Display OFF
Clock cycle	$t_{\phi CY}$	1.6			μs	
Minimum $\overline{H_{sync}}$ width at low level	t_{HWL}	4			μs	
Minimum $\overline{V_{sync}}$ width at low level	t_{VWL}	4			μs	

*: Minimum strobe to strobe time is applied when same character will be written continuously without changing blink data.
f_{OSC}: 4.0 to 8.0 MHz (V_{DD} = 4.5 V to 5.5 V), f_{OSC}: 4.0 to 6.0 MHz (V_{DD} = 3.0 V to 4.5 V)
S: Character size (1 or 2) (Mask option C: character size is fixed 1.)

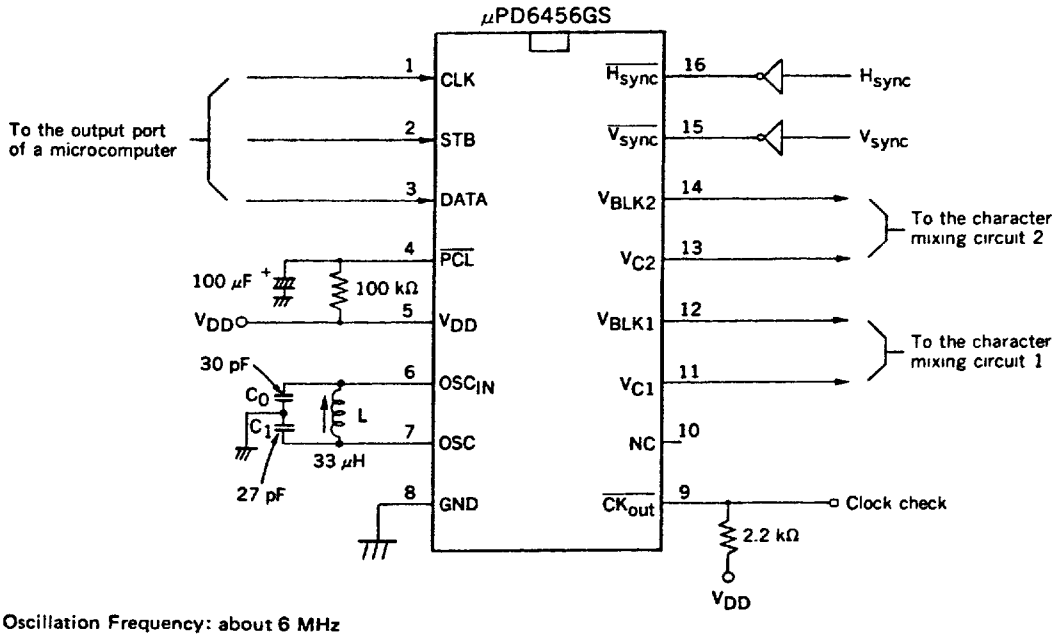


Power ON Reset

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
PCL terminal Minimum Low Hold Time	t_{PCLL}	10			μs	



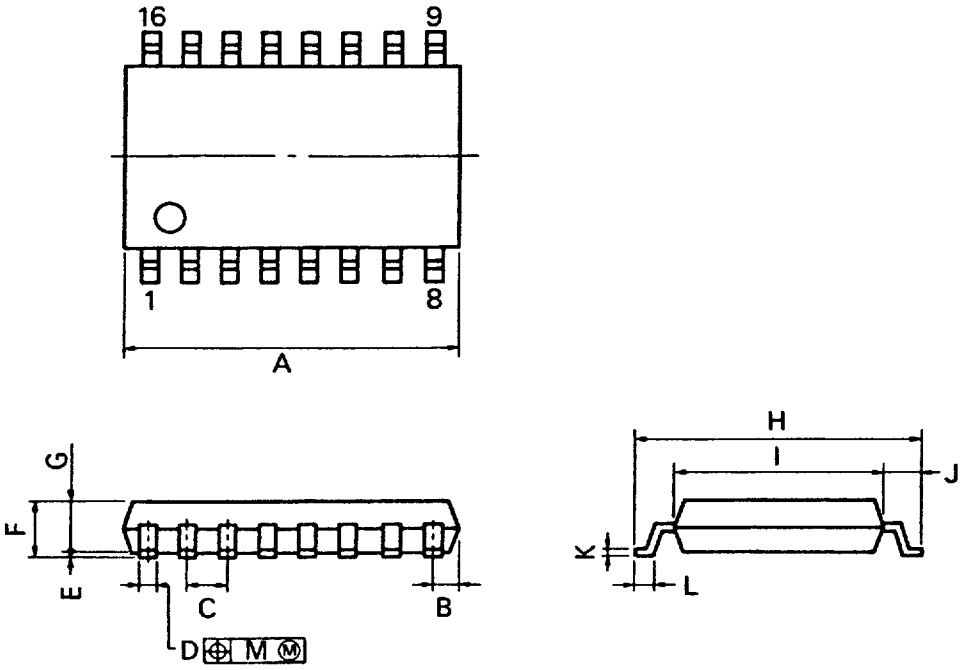
APPLICATION CIRCUIT



Oscillation Frequency: about 6 MHz

Note: The application circuit and values in this data sheet are simple examples, so they don't correspond to mass production.

16PIN PLASTIC SOP (300 mil)



P16GM-50-3008-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

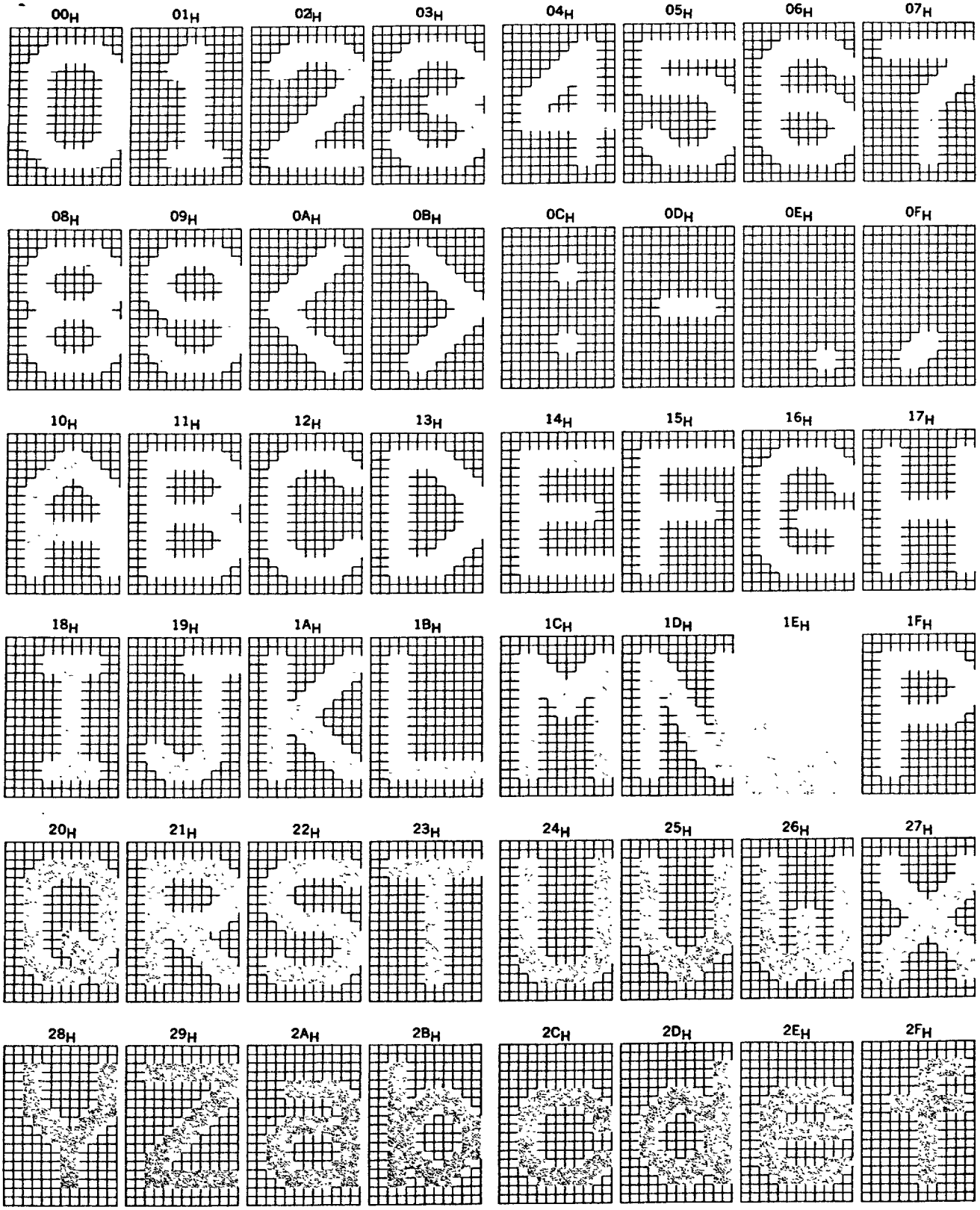
ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	$7.7^{+0.3}$	$0.303^{+0.012}$
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

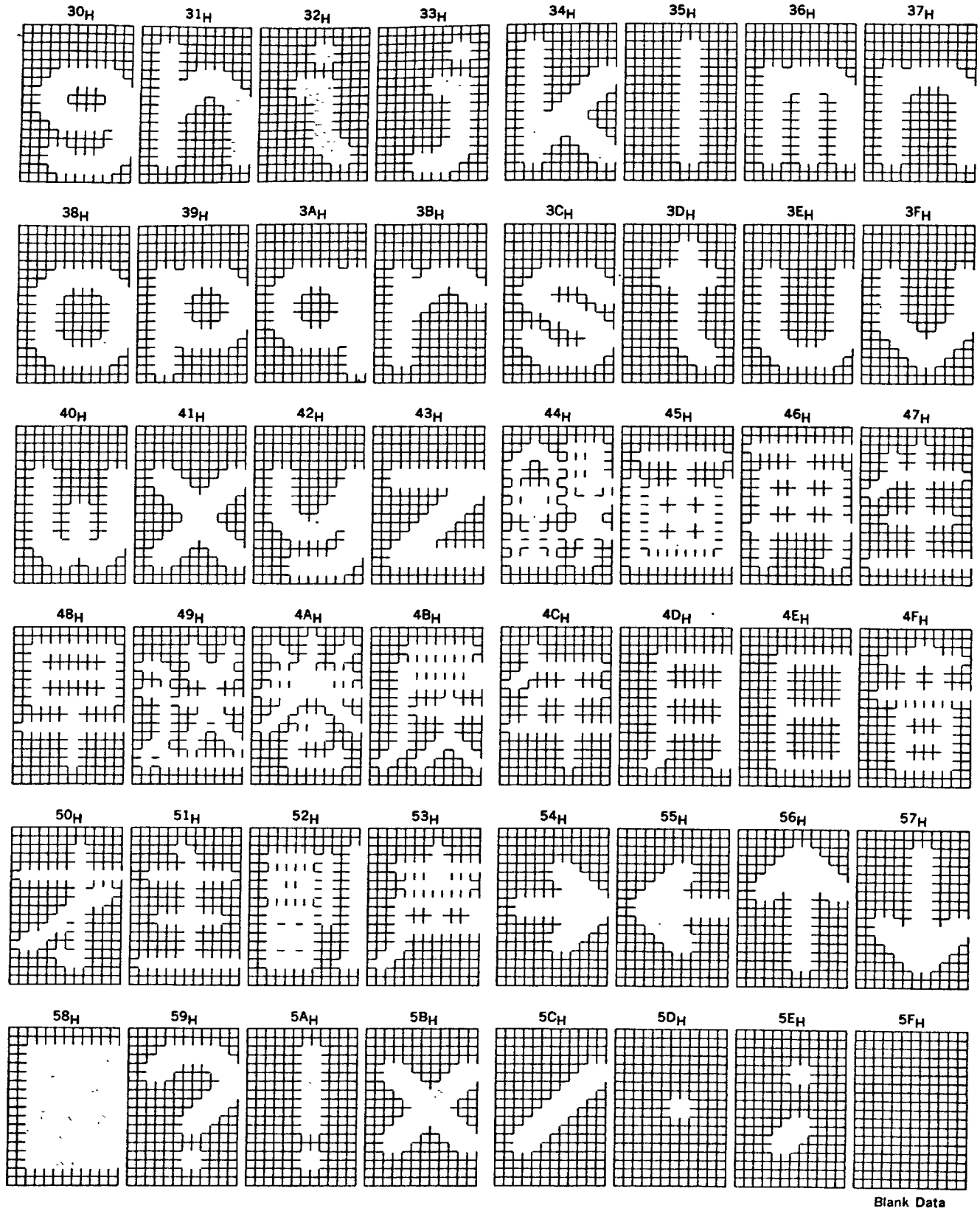
μPD6456GS-101/μPD6456GS-102/μPD6456GS-103 CHARACTER PATTERN

As shown in the following, μPD6456GS-101/μPD6456GS-102/μPD6456GS-103 enable display of 128 character generator ROM patterns. The 128 character generator ROM patterns can be changed by the mask code option. However, character code "7FH" is fixed to the Display OFF data so that no character pattern can be input to this code.

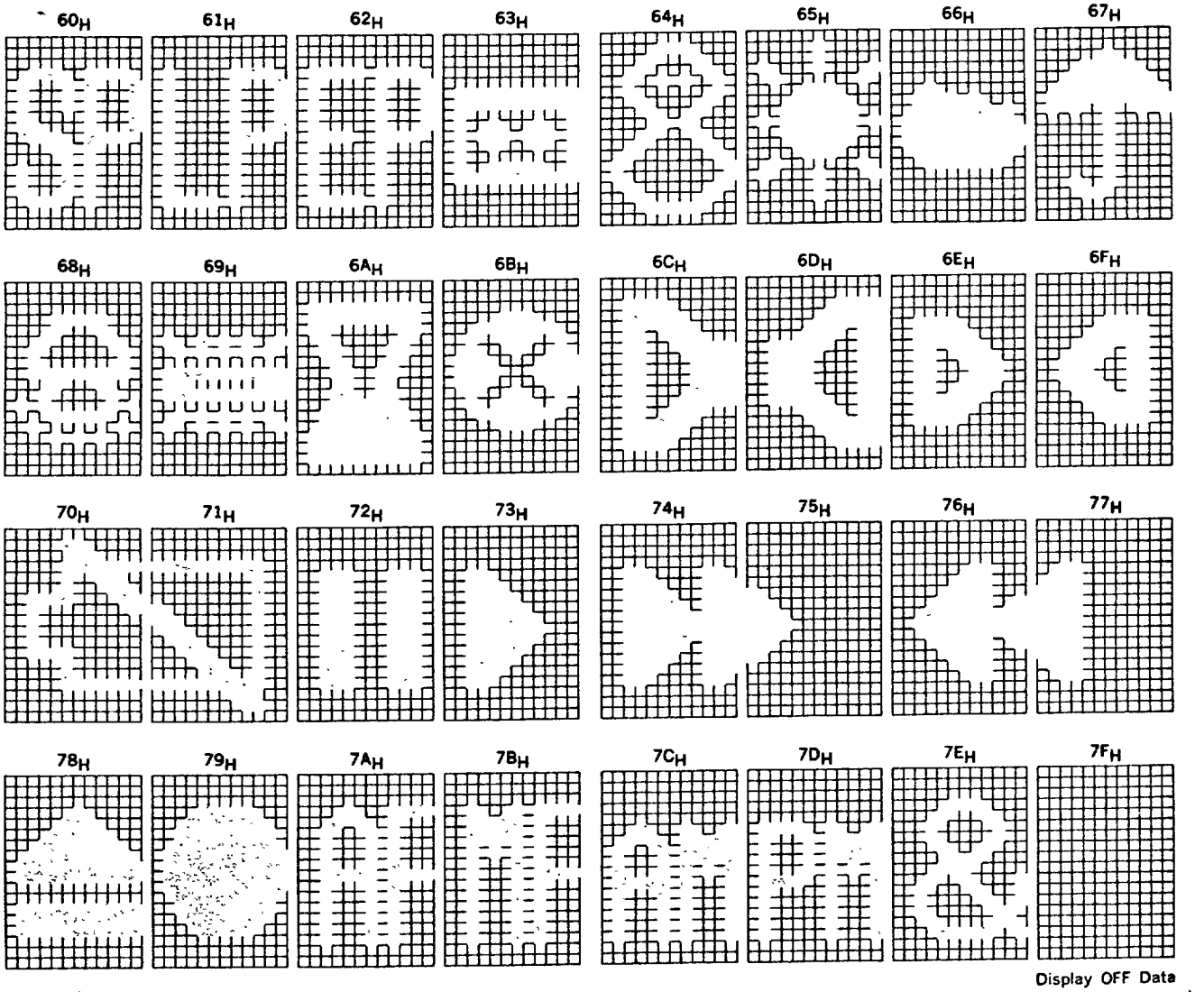
μPD6456GS-101, μPD6456GS-102 and μPD6456GS-103 have the same character patterns in the character generator ROM, and their packages are same, though their character signal output forms are different (μPD6456GS-101: mask code option A, μPD6456GS-102: mask code option B, μPD6456GS-103: mask code option C).

μPD6456GS-101, μPD6456GS-102, μPD6456GS-103 CHARACTER PATTERNS





Blank Data



Display OFF Data
(No character pattern can be set here.)