ABRIDGED VERSION

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SSI 33P3700

8-48 Mbit/s Magneto Optical Read Channel

February 1996

DESCRIPTION

The SSI 33P3700 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto optical (MO) drive systems. Functional blocks include sum and difference amplifier, input attenuator, pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 48 Mbit/s for (1,7) code, 6 to 36 Mbit/s for (2,7) code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3700 are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

FEATURES

- **Programmable MO/EMBOSS data rate of 8 to 48 Mbit/s for (1, 7RLL) code, 6 to 36 Mbit/s for (2, 7) code, internal DAC controlled**
- **Complete zoned recording application support**
- **Low-power operation (500 mW typical @ 5V)**
- **Bi-directional serial port register access**
- **Register programmable power management (sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-Lead TQFP package**

PULSE DETECTOR

- **Provides the head amplifiers difference for MO and sum for emboss signals**
- **Dual programmable attenuator (min-24 dB, 4-bit resolution) for MO and emboss data with Lo2w-Z switch and internal multiplexer**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Programmable LEVEL pin time constant with separate MO and emboss**
- **Separate MO and emboss AGC levels (4-bit DAC)**
- **Optimized pulse qualification circuitry for pit mark recording with input clip circuit**
- **Internal fast decay timing**
- **External $\overline{\text{LOW\_Z}}$ control pin**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 4 to 24 MHz**
- **Programmable boost/equalization of 0 to 12 dB**
- **Matched normal and differentiated outputs**
- **$\pm$ 20% fc accuracy (fc = 4 to 8 MHz)**
  $\pm$ 15% fc accuracy (fc = 8 to 24 MHz)
- **$\pm$ 4% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch is controlled by $\overline{\text{LOW\_Z}}$ pin**
- **No external filter components required**

TIME BASE GENERATOR

- **Better than 1% frequency resolution**
- **Up to 75 MHz frequency output**
- **Independent divide-by M and N registers**
- **VCO center frequency matched to data synchronizer VCO**
- **VCO (FOUT) output available except during power down mode**

DATA SYNCHRONIZER

- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data synchronizer**
  -No external delay lines, active devices, or active PLL components
- **Programmable decode window symmetry control via serial port**
  - Window shift control $\pm$ 30% (4-bit)
  - Includes delayed read MO/emboss data and VCO clock monitor points
- **Separate Qualifier output (RDO) and data separator input (RDI)**

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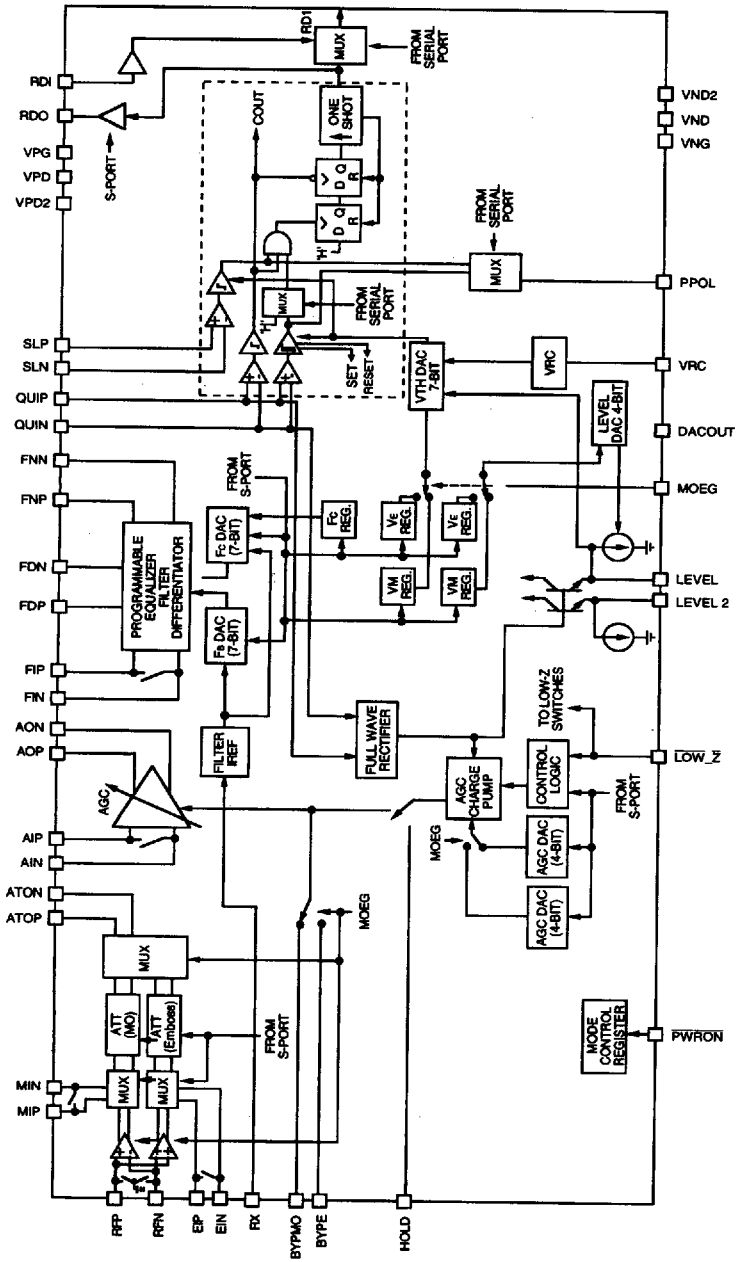

FIGURE 1A : Block Diagram - Front End

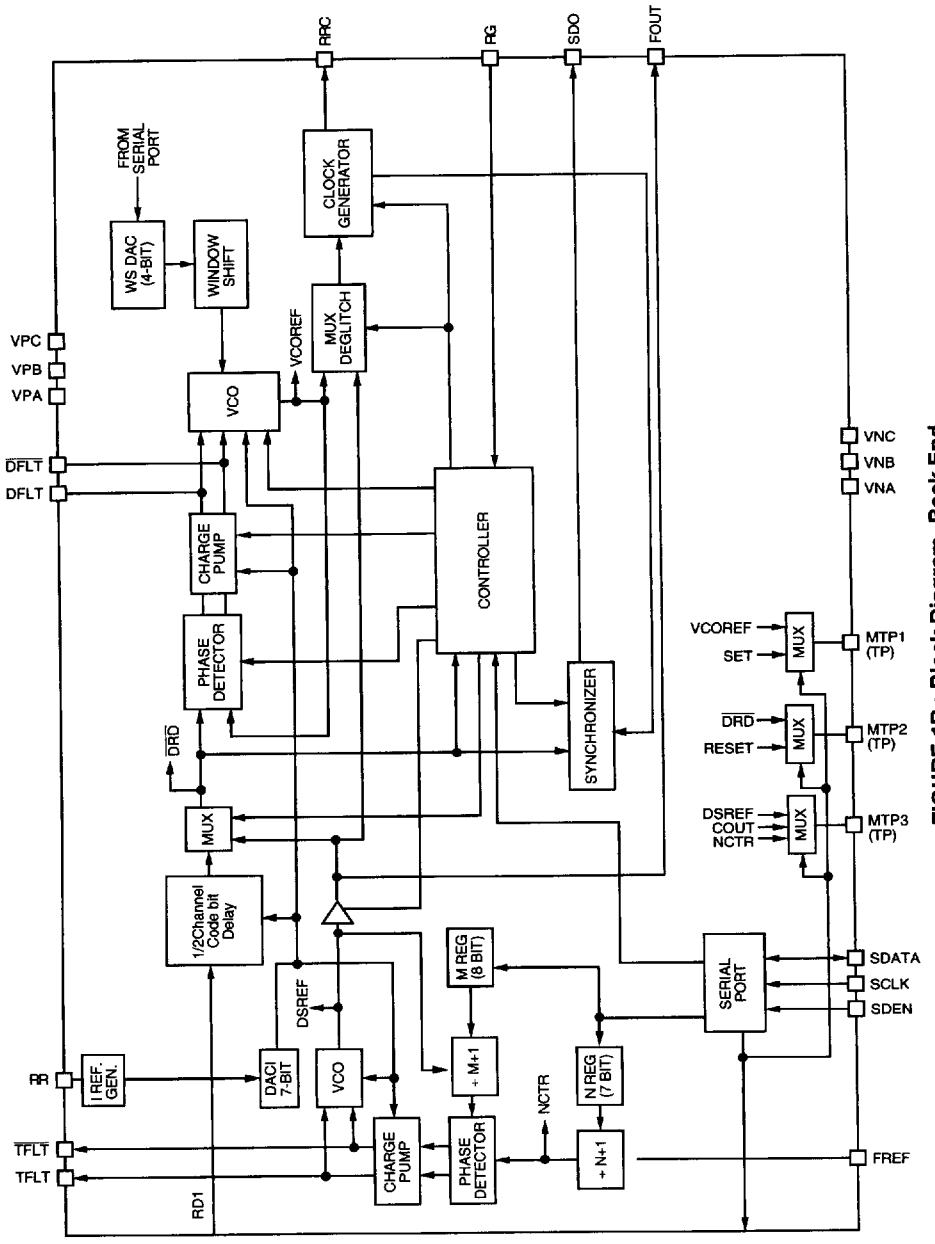

FIGURE 1B : Block Diagram -Back End

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FUNCTIONAL DESCRIPTION

The SSI 33P3700 implements a high performance complete read channel, including head amplifiers, dual programmable attenuator, multiplexer, pulse detector, programmable active filter, time base generator, and data synchronizer, at data rates up to 48 Mbit/s for (1, 7) code, 36 Mbit/s for (2, 7) code. A circuit diagram is shown in Figure 1.

INPUT INTERFACE & PULSE DETECTOR CIRCUIT DESCRIPTION

This device provides 3 types interface to the pulse detector, which are selected by MOEG and PDCR bit 1 for the customer applications. One is the RF signal interface, which provides the AC coupled connection from the I-V converter outputs. The second is the programmable attenuator interface, which provides dual attenuator for MO and emboss signals. The third is the AGC interface. The pulse detector, in conjunction with the programmable filter, provides all the MO data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide bandwidth, full-wave rectifier, and a dual rate charge pump. The entire signal path is fully differential to minimize external noise pick up.

HEAD AMPLIFIER

Two types of head amplifiers are provided: the difference amplifier for MO signals and the summing amplifiers for emboss signals. The gain of the difference amplifier is 5x and the summing one is 0.5x. So, the input ranges of RFP/RFN are 40-220 mVp-pd in MO mode (MOEG=low), 100-1100 mVp-p in emboss mode (MOEG=high) when PDCR bit 1 is low. When PDCR bit 1 goes high, these head amplifiers will be disabled and MIP/MIN (MOEG=low) or EIP/EIN (MOEG=high) input will be active.

PROGRAMMABLE ATTENUATOR

Dual attenuators are provided for the input signal swing variations of MO and emboss signals dependent on the zone and media. The maximum input range is 550 mVp-p and programmable range is 1 to 1/16 by 1/16 step. This circuit includes the MO and emboss signal multiplexer for AGC stage.

ATT Gain (MO) = (16-ATTMO)/16 V/V

ATT Gain (emboss) = (16-ATTEM)/16 V/V

where, ATTMO is lower 4 bits of attenuator Gain Register (ATGR) and ATTEM is upper 4 bits.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYPX}) stored on the BYPx hold capacitor (C_{BYPX}). A dual rate charge pump drives C_{BYPX} with currents that depend on the instantaneous differential voltage at the QUIP/QUIN pins. A constant decay current of approximately 4 µA acts to increases the amplifier gain. When the signal at QUIP/QUIN is greater than 100% of the programmed AGC level, the nominal attack current of approximately 0.18 mA is used to reduce the amplifier gain. The large ratio (0.18 mA:4 µA) of the nominal attack and nominal decay currents allow the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used the reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high/low yet minimizes distortion when the proper AGC level has been acquired.

A fast decay current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of 21. Fast decay occurs automatically for 1 µs after Low-Z.

In read mode, the reference voltage for the AGC charge pump is a nominal 1V. If you need, the reference voltage for the AGC charge pump is set by a 4-bit DAC (DACAMO/DACAEM) controlled by AGC level register. The DAC output voltage is offset so that "1111" results in a 0.76V output, and "0000" results in a 1V output:

$$V_{AGC} = 1.00 - (DACA\ X \bullet 0.016)\ Vp\text{-}p$$

where DACAX is the decimal value of the AGC Level register (DACAMO/DACAEM).

When the chip is in power down mode, the AGC dual rate charge pump is disabled.

Upon power-up the $\overline{LOW\_Z}$ pin should be brought low then high to execute fast decay. The part will recover from any transients or drift which may have occurred on the BYPX hold capacitors.

BYPMO AND BYPE CONTROL VOLTAGE

The BYPX capacitor voltage will be held constant (subject to leakage currents) during sleep mode, Low_Z mode, or when the HOLD signal is high. Upon the transition of $\overline{PWRON}$ high to low, there is a 1 µs delay inserted before the AGC loop is allowed to drive the BYPX capacitor (see AGC Mode). MOEG selects which capicator will be used. When MOEG is low, the BYPE capacitor voltage will be held constant (subject to leakage currents). When MOEG is high, the BYPMO capacitor voltage will be held constant (subject to leakage currents).

AGC MODE CONTROL

When the $\overline{LOW\_Z}$ pin is driven low, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. And the input impedance at the Head Amplifier, the Attenuator, the AGC amplifier and the programmable filter are reduced to allow for quick recovery of AC coupling capacitors. When the $\overline{LOW\_Z}$ pin goes high, the fast decay mode is internally set at a nominal 1 µs. Fast decay mode is also triggered by a transition of the MO/emboss gate (MOEG) pin in either direction. When the pulse detector is powered-down, V_{BYPX} will be held constant subject to leakage currents only.

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, V_{BYPX} will be held constant subject to leakage currents only.

RDO OUTPUT PIN

A PSEUDO CMOS output, 6 ns wide (min), Raw Data Output (RDO) signal is provided. This pin is controlled by CBR bit 0 (RDO register bit). When CBR bit 0 goes high, RDO will be held High_Z. The rising edge of RDO indicates the presence of a valid MO or emboss data pulse.

RDI INPUT PIN

A TTL compatible pin read data input (RDI) is provided as a read data input to the synchronizer from an external qualification circuit. RDI is available when CBR bit 2 (RDI register bit) goes high.

FUNCTIONAL DESCRIPTION (continued)

PULSE QUALIFICATION

The SSI 33P3700 provides an optimized pulse qualification circuit for pit mark detection. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The programmable hysteresis threshold, VTH, is driven by a multiplying DAC which is driven by the LEVEL voltage and referenced to VRC. The hysteresis threshold may be set from 10 to 80% with a resolution of 1%. A slice comparator also allows normal signal qualification for noise rejection. The slice level is set to AC ground when CBR bit 7 is low. When CBR bit 7 goes high, the slice level is added as an offset referenced to AC ground. This offset is related to the hysteresis threshold by a specific equation (See Electrical Specifications: Slice comparator). The internal current sink LEVEL DAC (DACL) and external capacitor CT set the hysteresis threshold time constant. DACL is switched between two 4-bit registers by MO/emboss gate (MOEG) to determine the sink current magnitude in MO data mode and emboss mode. In MO data mode, the four LSBs of the Hysteresis Decay Register (HDCR) determine the value of the pull-down current. In emboss mode the four MSBs are selected. The LSB value of DACL is 3.125 μA. DACL is offset by 1 LSB such that "0000" corresponds to 3.125 μA, and "1111" results in 50 μA. The SSI 33P3700 also provides a LEVEL 2 pin. The internal sink current is fixed at 50 μA.

The differentiated signal is connected to both the hysteresis and zero cross comparators. A positive peak that clears the established threshold level will set the hysteresis comparator. A peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator. This output signal is gated by the slice comparator output when FCCR bit 7 is low. When FCCR bit 7 goes high, the gate output is independent of the hysteresis comparator output. A positive edge of this gate output sets the D-Flip-flop Q high. This in turn feeds in to the D-input of the second Flip-flop which is triggered by the negative edge of the zero cross comparator output. Timing for the pulse qualification is shown in Figure 2.

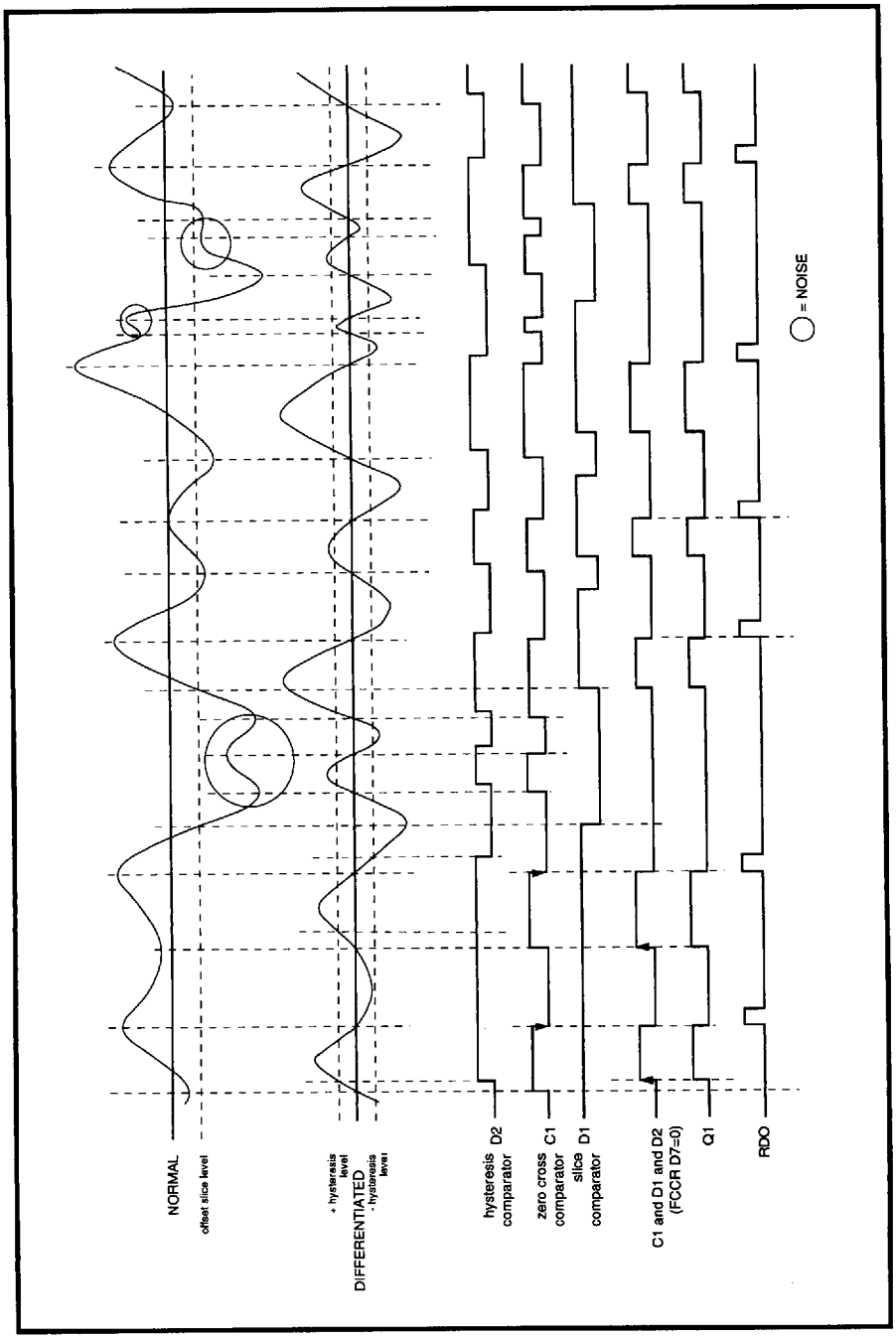

FIGURE 2 : Pulse Qualification Timing Diagram

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FUNCTIONAL DESCRIPTION (continued)

PPOL OUTPUT PIN

Pulse polarity signal output (a pseudo CMOS output) is provided for the sector mark detection. This signal is a comparator output and can be selected by MDTR bit 7 to be the output of the normal or differentiated signal. When the MDTR bit 7 goes low, the normal signal is selected. When the EMTR bit 7 goes high, PPOL will be held High_Z. The output is high when the pulse being qualified positive and it is low when the pulse being qualified is negative.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 33P3700 programmable filter consists of an electronically controlled low-pass filter with separate normal and differentiated low-pass outputs. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., Wc = 2 πfc = 1) are:

Vnorm/Vi = [(-Ks2 + 17.98016)/D(s)] • A_N

and

Vdiff/Vi = (Vnorm/Vi) • (s/0.86133) • A_D

Where D (s)=

$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203s + 2.95139)(S^2 + 1.14558s + 5.37034)(s + 0.86133)$,

A_N is adjusted for a gain of 2 at fs = (2/3) fc. A_D is adjusted for a gain of 2 at fs = fc

FILTER OPERATION

AC coupled differential signals from the AGC are applied to the FIP/FIN inputs of the filter. To improve settling time of the coupling capacitors, the FIP/FIN inputs are placed into a Low-Z state when the $\overline{LOW\_Z}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 12.1 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

fc = (0.194 • FCDAC) - 0.638 (MHz)

where FCDAC = FCCR register value.

In the read mode, the Filter Cutoff Control Register (FCCR) is used to determine the filter's 3 dB cutoff frequency. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost verses 3 dB frequency.

TABLE 1: 3 dB cutoff frequency versus boost magnitude.

BOOST (dB)	fc (3 dB)	BOOST (dB)	fc (3 dB)
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	-	-

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost = 20 log [(0.02559 • FBDAC) + (3.8 • 10^{-5} • FBDAC • FCDAC) + (-1.6 • 10^{-5} • $FBDAC^2$) +1](dB)

Where FBDAC = FBCR value

For example, with the DAC set for maximum output at fc = 4.0 MHz (FCCR = 18h or 24, FBCR = 79h or 121) there will be 12 dB of boost added at the 3 dB frequency. This will result in +9 dB of signal boost above the 0 dB baseline.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL.

In read, and idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In read mode the internal reference clock is disabled after the data synchronizer has achieved lock and switched over to read MO data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

Reference Frequency = ((M+1)/(N+1)) FREF

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the Data Recovery Control Register (DRCR). This DAC also sets the 1/2 channel code bit delay, VCO center frequency and phase detector gain for the data synchronizer circuitry. When changing frequencies, the M and N registers must be loaded first, followed by the DRCR register. A frequency change is initiated only when the DRCR register has been changed.

Fvco = [12.5/(RR + 0.4)]
• [(0.622 • DACI) + 4.27] MHz;

for Fvco < 24 MHz
Fvco = [12.5/(RR + 0.4)]
• [(0.7 • DACI) + 1.4] MHz

Where DACI is the value in the DRCR, and RR is the value (kΩ) of the external RR resistor, typically 12.1 kΩ.

DATA SYNCHRONIZER CIRCUIT DESCRIPTION

In the read mode, the data synchronizer performs sync field search and data synchronization. Data rate is established by the time base generator and the internal reference DACI controlled by the DRCR. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/2 channel code bit delay.

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the idle mode. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{DRD}$ pulse. In the idle mode the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL.

MODE CONTROL

The read gate (RG) input controls the device operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk.

FUNCTIONAL DESCRIPTION (continued)

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and a low level selects the reference clock. In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/2 code bit wide (TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock.

PREAMBLE SEARCH

When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read MO/emboss data, RD. Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to MO/emboss data.

VCO LOCK

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. If GS = "1", the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 16 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and dampening factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the MO data which follows. This (a total of 19 pulses from assertion of RG) asserts an internal VCO lock signal.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 2 VCO clock periods, however no short duration glitches will occur.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 16 transitions.

WINDOW SHIFT

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR). Further description of the WSCR is provided in the window shift control section.

NON-READ MODE

In the non-read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual MO data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

OPERATING MODES AND CONTROL

The SSI 33P3700 has several operating modes that support read (MO/emboss), and power management functions. Mode selection is accomplished by controlling the read gate (RG), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A register (CAR), and the Control B register (CBR) via the serial port.

EXTERNAL MODE CONTROL

All operating modes of the device are controlled by driving the read gate (RG), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins with TTL compatible signals. For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the SSI 33P3700 is controlled by the read gate (RG), and MO/emboss gate (MOEG) pins. When RG is high the device is in read mode. If the RG is low the device will be in idle mode. During the read mode, the MOEG pin can be activated to enable the emboss read mode of operation.

POWER DOWN CONTROL

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought high ("1") the device is placed into sleep mode (<5 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{\text{PWRON}}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3. To improve recovery time from the sleep mode, the $\overline{\text{LOW\_Z}}$ pin should be asserted following power down to initiate the AGC recovery sequence.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bidirectional port for reading and writing programming data from/to the internal registers of the SSI 33P3700. The serial port data transfer format is shown in Figure 3. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 3 provides register mapping information. The second byte contains the programming data. In serial port read mode (R/W=1) the SSI 33P3700 will output the register contents of the selected address. In serial port write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 4.

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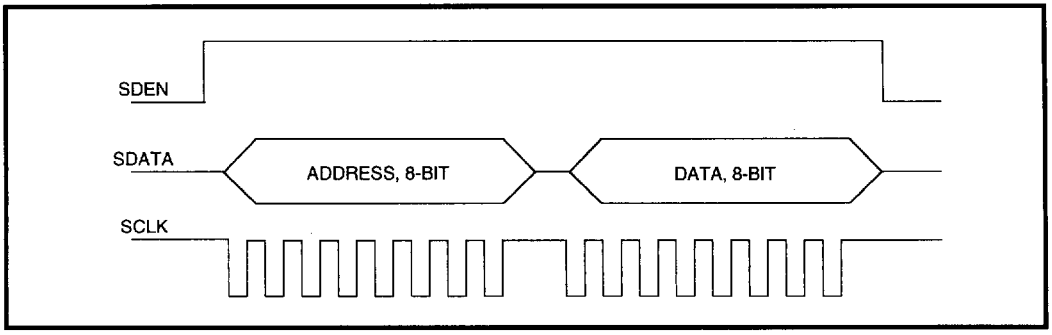

FIGURE 3: Serial Port Data Transfer Format

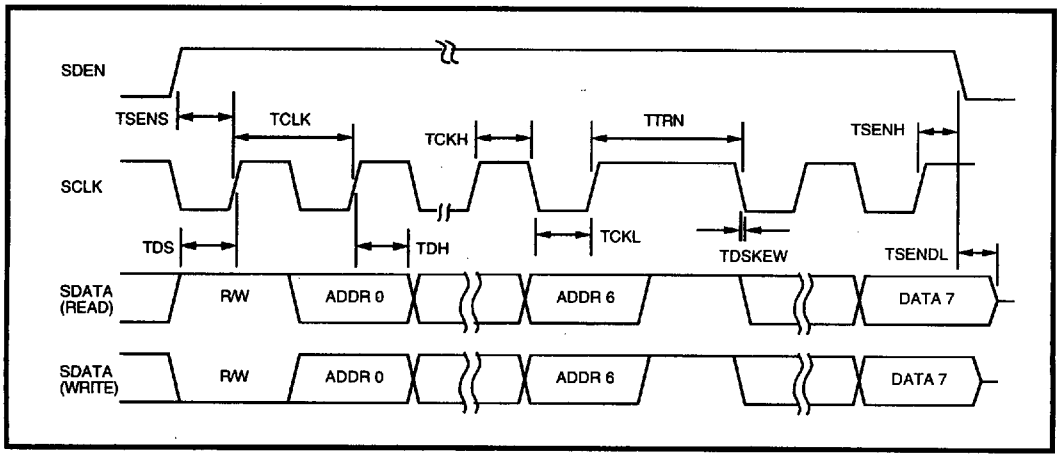

FIGURE 4 : Serial Port Timing Information

TABLE 2 : Mode Control

CONTROL LINE				DEVICE MODE	DAC CONTROL			
$\overline{PWRON}$	RG	MOEG	$\overline{LOW\_Z}$		VTH	AGC	ATT gain	HYSTERESIS
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	1	0	1	**MO READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence.	MR	MR	MR	MR
0	1	1	1	**EMBOSS READ MODE:** The pulse detector is active and the emboss control registers are selected for the V_{TH}, AGC Level, Hysteresis decay, and Attenuator gain. The data synchronize begins the preamble lock sequence.	ER	ER	ER	ER
0 (0	0 0	0 1	X X)	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the MO data (Emboss) control registers are used for V_{TH} and FC.	MR (ER	MR ER	MR ER	MR ER)
-	-	-	-	All other states are illegal. If an illegal state is programmed, the chip function will be in an indeterminable state, but no damage will occur.	MR	MR	MR	MR

DAC Control Key: MR = MO data register, ER = Emboss register, off = disabled

TABLE 3 : Serial Port Register Mapping

REGISTER NAME		A6						A0	R/W	D7			DATA BIT MAP				D0
POWER DOWN CONTROL	(PDCR)	0	0	0	0	0	1	0	0	--	--	--	TBG 1=DISABLE 0=ENABLE	DATA SEP 1=DISABLE 0=ENABLE	FILTER 1=DISABLE 0=ENABLE	RF AMP 1=DISABLE 0=ENABLE	PD 1=DISABLE 0=ENABLE
FILTER CUTOFF	(FCCR)	0	0	0	0	0	1	1	0	VTH COMP. OUTPUT 1=UNUSED 0=NORMAL	Fc DAC BIT 6	Fc DAC BIT 5	Fc DAC BIT 4	Fc DAC BIT 3	Fc DAC BIT 2	Fc DAC BIT 1	Fc DAC BIT 0
FILTER BOOST	(FBCR)	0	0	0	1	0	1	1	0	--	Fs DAC BIT 6	Fs DAC BIT 5	Fs DAC BIT 4	Fs DAC BIT 3	Fs DAC BIT 2	Fs DAC BIT 1	Fs DAC BIT 0
MO DATA THRESHOLD	(MDTR)	0	0	0	1	0	1	0	0	PPOL SEL 1=DIFF 0=NORMAL	VTH DAC BIT 6 MO	VTH DAC BIT 5 MO	VTH DAC BIT 4 MO	VTH DAC BIT 3 MO	VTH DAC BIT 2 MO	VTH DAC BIT 1 MO	VTH DAC BIT 0 MO
EMBOSS THRESHOLD	(EMTR)	0	0	1	0	0	1	0	0	PPOL OUTPUT 1=HI-Z 0=ENABLE	VTH DAC BIT 6 EMBOSS	VTH DAC BIT 5 EMBOSS	VTH DAC BIT 4 EMBOSS	VTH DAC BIT 3 EMBOSS	VTH DAC BIT 2 EMBOSS	VTH DAC BIT 1 EMBOSS	VTH DAC BIT 0 EMBOSS
CONTROL A	(CAR)	0	0	1	1	0	1	0	0	Fast Decay test mode 0=ENABLE	TMS1	TMS0	TBG 1=BYPASS 0=NORMAL	MTP3 TEST POINT 1=ENABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE
CONTROL B	(CBR)	0	0	0	1	1	0	0	0	SLICE LEVEL OFFSET 1=ENABLE 0=DISABLE	MTPE 1=ENABLE 0=DISABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE	RDI 1 = INPUT 0 = DISABLE	GAIN SHFT 1 = ON 0 = OFF	RDO 1=RDO HI-Z 0=ENABLE
N COUNTER	(NCR)	0	0	0	0	1	1	0	0	TBG KD 1=3 x KD 0=1 x KD	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	(MCR)	0	0	0	1	1	1	0	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	(DRCR)	0	0	0	0	1	0	0	0	--	DAC I BIT 6	DAC I BIT 5	DAC I BIT 4	DAC I BIT 3	DAC I BIT 2	DAC I BIT 1	DAC I BIT 0
WINDOW SHIFT	(WSCR)	0	0	0	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
AGC LEVEL	(ALCR)	0	1	0	0	0	1	0	0	DACAEM BIT 3	DACAEM BIT 2	DACAEM BIT 1	DACAEM BIT 0	DACAMO BIT 3	DACAMO BIT 2	DACAMO BIT 1	DACAMO BIT 0
HYSTERESIS DECAY	(HDCR)	0	1	0	1	0	1	0	0	DACL BIT 3 EMBOSS	DACL BIT 2 EMBOSS	DACL BIT 1 EMBOSS	DACL BIT 0 EMBOSS	DACL BIT 3 MO	DACL BIT 2 MO	DACL BIT 1 MO	DACL BIT 0 MO
ATTENUATOR GAIN	(ATGR)	0	1	1	0	0	1	0	0	ATTEM BIT 3	ATTEM BIT 2	ATTEM BIT 1	ATTEM BIT 0	ATTMO BIT 3	ATTMO BIT 2	ATTMO BIT 1	ATTMO BIT 0

FUNCTIONAL DESCRIPTION (continued)

CONTROL REGISTERS

Control registers CAR and CBR allow the user to configure the SSI 33P3700 test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the pulse detector, filter, and time base generator. CBR controls test points and functions of the data separator. The bits of the CA and CB registers are defined as follows:

CONTROL REGISTER CA

BIT	NAME	FUNCTION
0	EPDT	Enable Phase Detector (Time Base Generator)
1	UT	Pump Up (TFLT sources current, $\overline{\text{TFLT}}$ sinks current)
2	DT	Pump Down (TFLT sinks current, $\overline{\text{TFLT}}$ sources current)
3	ET	Enable MTP3 Test Point Output
4	BYPT	Bypass Time Base Generator Circuit Function
5	TMS0	Control bit for selecting test point source (see Table 4)
6	TMS1	Control bit for selecting test point source (see Table 4)
7	FDTM	Constant fast decay current test mode

CONTROL REGISTER CB

BIT	NAME	FUNCTION
0	RDO	RDO pin control
1	GS	Enable Phase Detector Gain Switching
2	RDI	RDI Pin input control
3	EPDD	Enable Phase Detector (Data Separator)
4	UD	Pump Up (DFLT sources current, $\overline{\text{DFLT}}$ sinks Current)
5	DD	Pump Down (DFLT sinks current, $\overline{\text{DFLT}}$ sources Current)
6	MTPE	Enable Test Points MTP1, 2, 3, (see Table 4)
7	SLICE LEVEL OFFSET	Enable slice level offset of SLP/SLN comparator

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data synchronizer PLL analog power supply pin
VPB	-	Time base generator PLL analog power supply pin
VPC	-	Internal ECL, CMOS logic power supply pin
VPD, VPD2	-	CMOS and Pseud CMOS buffer I/O digital power supply pin
VPG	-	RF amp, attenuator, pulse detector, filter, analog power supply pin
VNA	-	Data Synchronizer PLL analog ground pin
VNB	-	Time base generator PLL analog ground pin
VNC	-	Internal ECL, CMOS logic ground pin
VND, VND2	-	CMOS and pseud CMOS buffer I/O digital ground pin
VNG	-	RF amp, attenuator, pulse detector, filter, analog ground pin

INPUT PIN

RFP, RFN	I	RF AMPLIFIER INPUTS: Sum and differential amplifier input pins.
MIP, MIN	I	MO SIGNAL INPUTS: Differential MO signal attenuator input pins.
EIP, EIN	I	EMBOSS SIGNAL INPUTS: Differentia emboss signal attenuator input pins.
AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
SLP, SLN	I	ANALOG INPUTS FOR QUALIFIER: Differential analog inputs to the comparator.
QUIP, QUIN	I	ANALOG INPUTS FOR QUALIFIER: Differential analog inputs to the hysteresis and zero cross comparator and full wave rectifier.
FIP, FIN	I	FILTER SIGNAL INPUTS: The AGC output must be AC coupled into these pins.
$\overline{\text{LOW\_Z}}$	I	LOW IMPEDANCE ENABLE: TTL compatible input pin that activates the Low-Z switches. A low level activates the switches, and the falling edge of the internal LOW_Z triggers the fast decay circuit.
$\overline{\text{PWRON}}$	I	POWER ENABLE: CMOS compatible power control input. A low level TTL input enables power to circuitry according to the contents of the PDCR. A high level CMOS input shuts down all circuitry.
HOLD	I	HOLD CONTROL: TTL compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. FREF pin has an internal pull-down resistor.
RDI	I	READ DATA INPUT: TTL compatible input. RDI is provided as read data input to the data synchronizer from an external qualification circuit. RDI is available when CBR bit 2 goes high.
RG	I	READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input and enables the read mode and activates SDO output.
MOEG	I	MO/emboss GATE: TTL compatible MO/emboss gate inputs. A high level TTL input activates the emboss mode by selecting emboss control registers, and the BYPE capacitor.

OUTPUT PINS

MTP1-3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO	O	SYNCHRONIZED READ DATA: Pseudo CMOS output pin. Read MO/emboss data output when RG is high.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals.
RDO	O	RAW DATA OUTPUT: Pseudo CMOS output pin. The rising edge of RDO indicates the presence of a valid MO/emboss data pulse. When CBR bit 0 goes high, RDO will be held High_Z.
RRC	O	READ REFERENCE CLOCK: Read clock pseudo CMOS output. During mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to the reference clock. When the Sync Bits (internal) are detected, RRC is synchronized to the read data. When RG goes low, RRC is synchronized back to the reference clock.
ATOP, ATON	O	ATTENUATOR OUTPUT: Differential attenuator output pins. These are AC coupled into the AGC amplifier inputs (AIP, AIN).
AOP, AON	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN).
FOUT	O	TIME BASE GENERATOR VCO OUTPUT: Pseudo CMOS output pin. This clock signal is the data synchronizer PLL reference.
PPOL	O	PULSE POLARITY: Pulse polarity pseudo CMOS output pin. The output is high when the input signal is over the threshold level. This output signal can select either input signal normal or differentiated by MDTR bit 7. When the MDTR bit 7 = low, the normal signal is selected. When the EMTR bit 7 goes high, PPOL will be held High_Z.

ANALOG PINS

NAME	TYPE	DESCRIPTION
BYPMO	-	The AGC read mode integration capacitor CBYPMO, is connected between BYPMO and VPG.
BYPE	-	The AGC emboss read mode integration capacitor CBYPE, is connected between BYPE and VPG.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the output of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register (see Table 5).
TFLT, $\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DFLT, $\overline{\text{DFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the data synchronizer loop filter.
LEVEL, LEVEL 2	-	An NPN emitter output that provides a full wave rectified signal from QUIP/ QUIN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with the internal current DAC, (DACL). The internal sink current of LEVEL 2 is fixed.
VRC	-	REFERENCE VOLTAGE OUTPUT: This pin provides the internal DC bias reference voltage.
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data synchronizer and time base generator.
RX	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	I	SERIAL DATA ENABLE: Serial enable CMOS compatible CMOS input. A high level input enables the serial port.
SDATA	I/O	SERIAL DATA: Serial data bidirectional CMOS compatible CMOS pin. NRZ programming data for the internal registers is applied to this input when the first bit is 0. When the first bit is 1, the address register data will be clocked out on the rising edge of SCLK.
SCLK	I	SERIAL CLOCK: Serial clock CMOS compatible CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA.

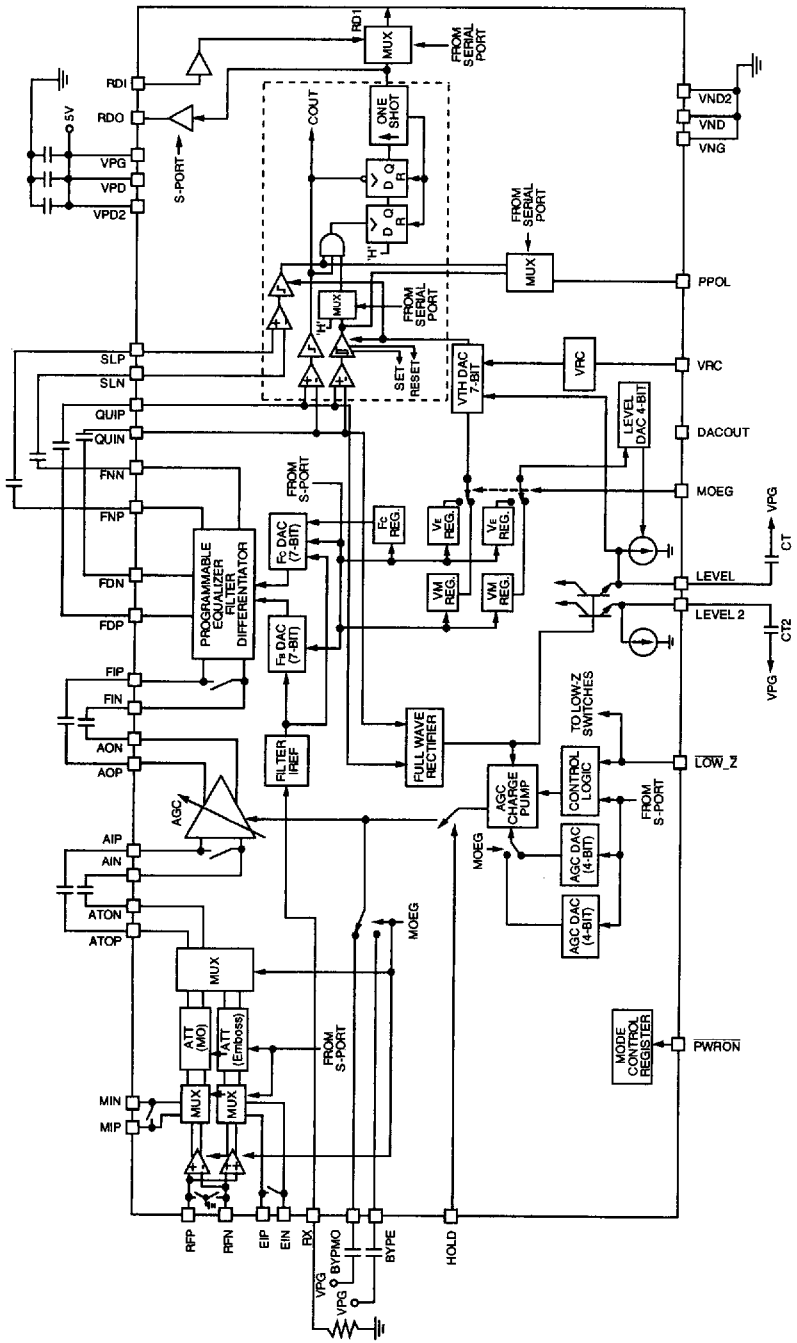

FIGURE 7A : Application Diagram - Front End

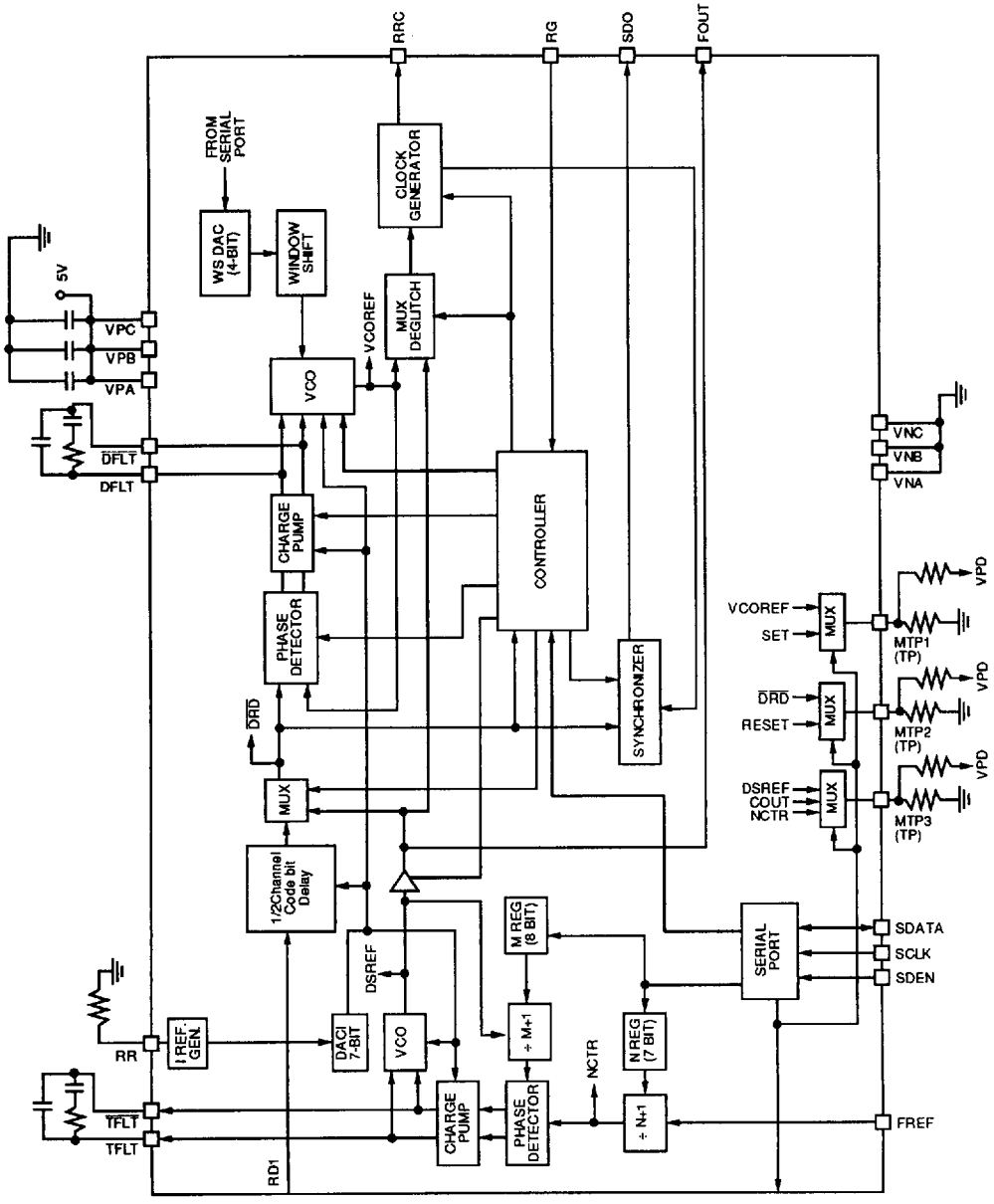

FIGURE 7B : Application Diagram -Back End

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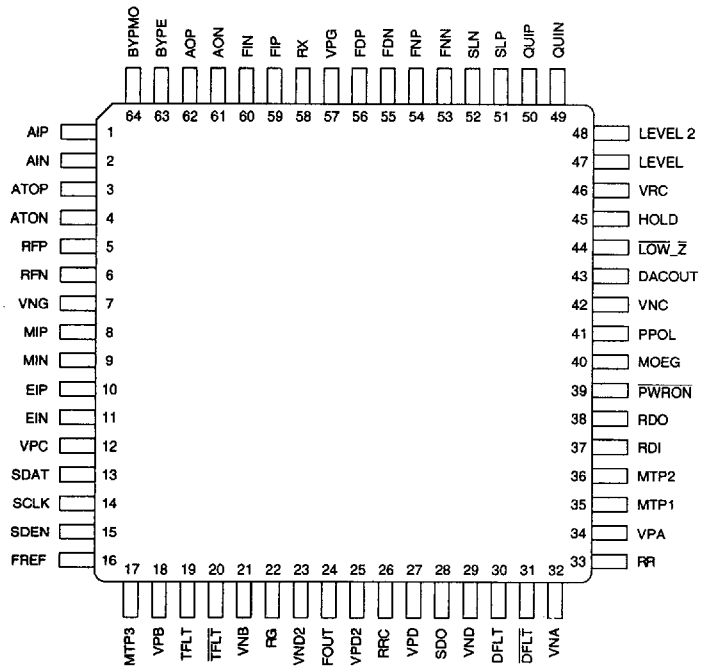
SSI 33P3700
8-48 Mbit/s Magneto Optical Read Channel

PACKAGE PIN DESIGNATIONS
(Top view)

THERMAL CHARACTERISTICS: θjA

64-lead TQFP	75° C/W



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 33P3700	64-Lead TQFP	33P3700-CGT	33P3700-CGT

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914