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Mosaic Semiconductor Inc.



# PUMA 2U2000-12/15/17/20

Issue 1.2 : February 1990

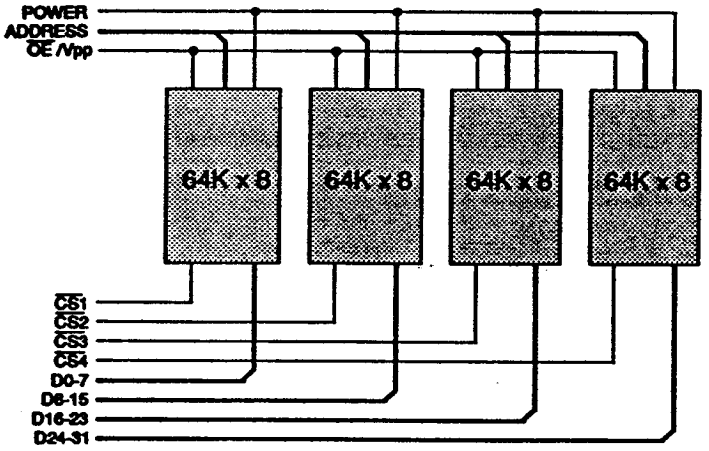
## ADVANCE PRODUCT INFORMATION

1,048,576 bit CMOS High Speed UV EPROM

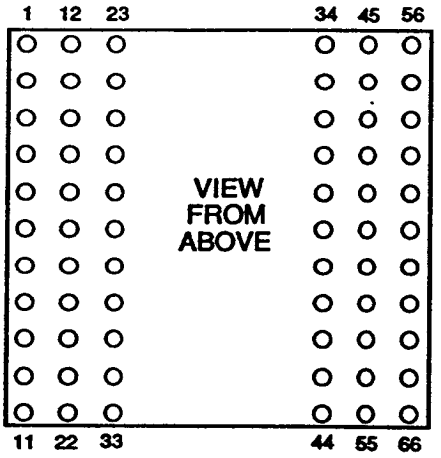
### Features

- User Configurable as 8,16 or 32 bit wide.
- Very Fast access times of 120/150/170/200 ns.
- Operating Power 1000mW (typ), 32 bit mode.
  530mW (typ), 16 bit mode.
  295mW (typ), 8 bit mode.
- Low Power Standby 4mW (typ).
- $V_{PP}$ Program Voltage of 12.5V.
- Pin grid array gives 2:1 improvement over DIL.
- Package Suitable for Thermal Ladder Applications.
- On board decoupling capacitors.
- May be screened as BS9400 & MIL-STD-883C.

### Block Diagram




### Pin Definition

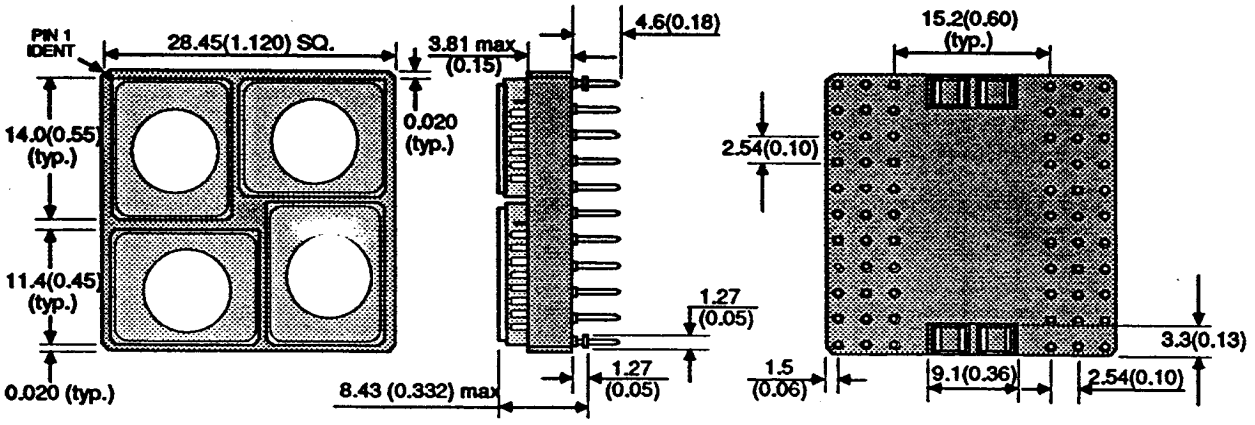



For pinout see page 7

### Pin Functions

| | |
|---|---|
| A0-15 | Address Inputs |
| D0-D32 | Data Inputs/Outputs |
| $\overline{CS1\text{-}4}$ | Chip Select |
| $\overline{OE}/V_{PP}$ | Output Enable/Programming Voltage |
| NC | No Connect |
| $V_{CC}$ | Power (+5V) |
| GND | Ground |

### Package Details Dimensions in mm (inches).



## Absolute Maximum Ratings (1)

| | | |
|---|---|---|
| Supply Voltage (2) | $V_{CC}$ | -0.6 to +6.25 V |
| Programming Voltage | $V_{PP}$ | -0.6 to +14 V |
| Input Voltage (2),(3) | $V_{IN}$ | -0.6 to +6.25 V |
| Operating Temperature | $T_{OPR}$ | -60 to +140 °C |
| Storage Temperature | $T_{STG}$ | -65 to +150 °C |

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) Pulse Width: -2.0V for less than 20ns.
(3) With Respect to GND.

## Recommended Operating Conditions

| | | *min* | *typ* | *max* | |
|---|---|---|---|---|---|
| DC Logic Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 6.3 | V |
| DC EPROM Program Voltage | $V_{PP}$ | 12.2 | - | 12.5 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | - | $V_{CC}$+1 | V |
| Input Low Voltage | $V_{IL}$ | 0.3 | - | 0.8 | V |
| Operating Temperature(1) | $T_A$ | 0 | - | 70 | °C |
| | $T_{AI}$ | -40 | - | 85 | °C (2000I) |
| | $T_{AM}$ | -55 | - | 125 | °C (2000M,MB) |

Note: (1) Programming would normally take place at 25°C
(2) When programming a 0.1µF high frequency by-pass capacitor is required across $V_{PP}$ and GND to suppress noise transients

## Operating Modes

The Table below show the logic inputs required to control the operating modes of each EPROM on the PUMA2U2000.

| *Mode* | $\overline{CS}$ | $\overline{OE}/V_{PP}$ | $V_{CC}$ | *Outputs* |
|---|---|---|---|---|
| Read | 0 | 0 | 5V | Data out |
| Output Disable | 0 | 1 | 5V | Floating |
| Standby | 1 | X | 5V | Floating |
| Program | 0 | 12.5V | 6V | Data in |
| Program Verify | 0 | 0 | 6V | Data out |
| Program Inhibit | 1 | 12.5V | 6V | Floating |

1 = $V_{IH}$
0 = $V_{IL}$
X = $V_{IH}$ or $V_{IL}$

## Device Identifier Mode

The Identifier Mode allows the reading out of binary codes, which identify manufacturer and type of device, from the outputs of each EPROM. By this mode, the device can be automatically matched to the correct programming algorithm using a suitable EPROM Programmer. The table below shows the outputs of a single EPROM with the PUMA 2U2000 in 8 bit Mode.

| PINS / IDENTIFIER | A9 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX DATA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | 12.0V | $V_{il}$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1F |
| Device Code | | $V_{ih}$ | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |

Notes (1) A1 - A8, A10 - A15, $\overline{CS1}$ and $\overline{OE}$ are all held at $V_{IL}$

## READ OPERATION

### DC Electrical Characteristics ($T_a$= -55°C to +125°C, $V_{CC}$=5V±5%)

| Parameter | Symbol | Test Condition | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IN1}$ | $V_{IN}$=5.25V, Address & $\overline{OE}/V_{PP}$ | - | - | 40 | µA |
| | $I_{IN2}$ | $\overline{CE1}$ - $\overline{CE4}$ | - | - | 10 | µA |
| Output Leakage Current | $I_{OUT}$ | $V_{OUT}$=5.25V/0.45V | - | - | 40 | µA |
| $V_{PP}$ Leakage Current | $I_{PP}$ | $V_{PP}$=5.5V | - | - | 40 | µA |
| Standby Power | $I_{SB1}$ | $\overline{CS}$ = $V_{IH}$ | - | - | 12 | mA |
| Supply Current | $I_{sb2}$ | $\overline{CS}$=$V_{CC}$ ±0.3V, $I_{OUT}$=0mA | - | - | 800 | µA |
| Operating Power Supply Current | $I_{CC}$ | f=5MHz, $I_{OUT}$=0mA (3) | 59 | 106 | 200 | mA |
| Input Low Voltage | $V_{IL}$ | Note (1) | -0.6 | - | 0.8 | V |
| Input High Voltage | $V_{IH}$ | Note (2) | 2.0 | - | $V_{CC}$+1 | V |
| Output LowVoltage | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.45 | V |
| Output HighVoltage | $V_{OH}$ | $I_{OH}$=-400µA | 2.4 | - | - | V |

Notes (1) -1.0V for pulse width ≤ 50 ns
(2) Vcc+1.5V for pulse width ≤20 ns. If $V_{IH}$ is over the specified max. value, READ operation cannot be guaranteed.
(3) For these currents min, typ and max values are given for 8, 16 and 32 bit mode operation respectively. Values are min.

### Capacitance ($T_A$=25°C, f=1MHz)

| Parameter | Symbol | Test Condition | typ | max | Unit |
|---|---|---|---|---|---|
| Input Capacitance: | $C_{IN}$ | $V_{IN}$=0V, 8 bit mode | 16 | 24 | pF |
| Output Capacitance: | $C_{OUT}$ | $V_{OUT}$=0V, 8 bit mode | 32 | 48 | pF |

Note: Capacitance calculated not measured.

### AC Characteristics

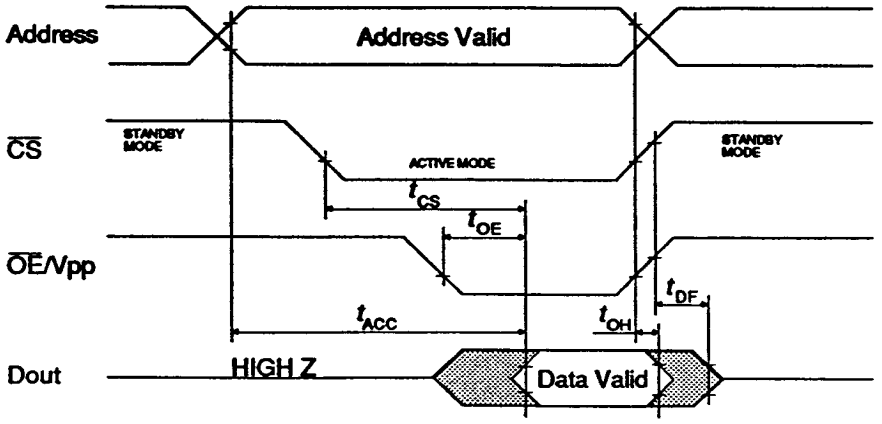
| | | -12 | | -15 | | -17 | | -20 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | min | max | min | max | min | max | min | max | Unit |
| Address to Output Delay | $t_{ACC}$ | - | 120 | - | 150 | - | 170 | - | 200 | ns |
| $\overline{CS}$ to Output Delay | $t_{CS}$ | - | 120 | - | 150 | - | 170 | - | 200 | ns |
| $\overline{OE}/V_{PP}$ to Output Delay | $t_{OE}$ | - | 65 | - | 70 | - | 70 | - | 75 | ns |
| $\overline{OE}/V_{PP}$ or $\overline{CS}$ High to Output Float | $t_{DF}$ | - | 50 | - | 50 | - | 50 | - | 55 | ns |
| O/P Hold from Address, $\overline{CS}$ or $\overline{OE}/V_{PP}$ | $t_{OH}$ | - | 0 | - | 0 | - | 0 | - | 0 | ns |

NOTE : $T_{DF}$ not measured but guaranteed by design.

### AC Test Conditions

* Input pulse levels: 0.45V to 2.4V
* Input rise and fall times: ≤ 20ns
* Input and Output timing reference levels: 0.8V and 2.0V
* Output load : 1 TTL gate plus 100pF.

### Read Cycle Timing Waveform



## PROGRAMMING OPERATION

### DC Electrical Characteristics ($T_A$ = 25°C ±5°C, $V_{CC}$ = 6V±0.25V, $V_{PP}$ = 12.5V ±0.5V)

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IN}$ | $V_{IH}$=5.25V | - | - | 40 | µA |
| Operating Power Supply Current | $I_{CC}$ | Note (7) | 46 | 84 | 160 | mA |
| $V_{PP}$ Supply Current | $I_{PP1}$ | Single Byte Programming (7) | 25 | 50 | 100 | mA |
| Input Low Voltage | $V_{IL}$ | Note (5) | -0.6 | - | 0.8 | V |
| Input High Voltage | $V_{IH}$ | Note (6) | 2.0 | - | $V_{CC}$ +1 | V |
| Output LowVoltage (Verify) | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.45 | V |
| Output HighVoltage (Verify) | $V_{OH}$ | $I_{OH}$=-400µA | 2.4 | - | - | V |

Notes (1) $V_{CC}$ must be applied before $V_{PP}$ and removed after $V_{PP}$.
(2) $V_{PP}$ must not exceed 13V including overshoot.
(3) Device reliability may be affected if device is installed or removed while $V_{PP}$= 12.5V
(4) The transitions Vil to 12.5V or 12.5V to $V_{il}$ are not allowed while CS = Low.
(5) -0.6V for pulse width ≤ 20 ns.
(6) If $V_{ih}$ is over the specified maximum value, programming operation cannot be guaranteed.
(7) For Vcc and Vpp Supply Currents, min, typ and max values are given for 8, 16 and 32 bit mode operation respectively. Each individual value shown is a maximum.
(8) When programming a 0.1µF high frequency by-pass capacitor is required across $V_{PP}$ and GND to suppress noise transients

### AC Characteristics ($T_A$=25±5°C, $V_{CC}$=6.0±0.25V, $\overline{OE}/V_{PP}$=12.5±0.5V)

| *Parameter* | *Symbol* | *min* | *max* | *Unit* | *Notes* |
|---|---|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 2 | - | µs | |
| $\overline{OE}/V_{PP}$ Setup Time | $t_{OES}$ | 2 | - | µs | 1 |
| $\overline{OE}/V_{PP}$ Hold Time | $t_{OEH}$ | 2 | - | µs | 1 |
| Data Setup Time | $t_{DS}$ | 2 | - | µs | |
| Address Hold Time | $t_{AH}$ | 0 | - | µs | |
| Data Hold Time | $t_{DH}$ | 2 | - | µs | |
| $\overline{CS}$ High to Output Float Delay | $t_{DFP}$ | 0 | 130 | ns | 2 |
| $V_{CC}$ Setup Time | $t_{VCS}$ | 2 | - | µs | 1 |
| $\overline{CS}$ Initial Program Pulse Width | $t_{PW}$ | 0.95 | 1.05 | ms | 3 |
| $\overline{CS}$ Overprogram Pulse Width | $t_{OPW}$ | 2.85 | 78.75 | ms | 4 |
| Data Valid from $\overline{CS}$ | $t_{DV}$ | - | 1 | µs | 2 |
| $\overline{OE}/V_{PP}$ Recovery Time | $t_{VR}$ | 2 | - | µs | 1 |
| $\overline{OE}/V_{PP}$ Pulse Rise time during Programming | $t_{PRT}$ | 50 | - | ns | |

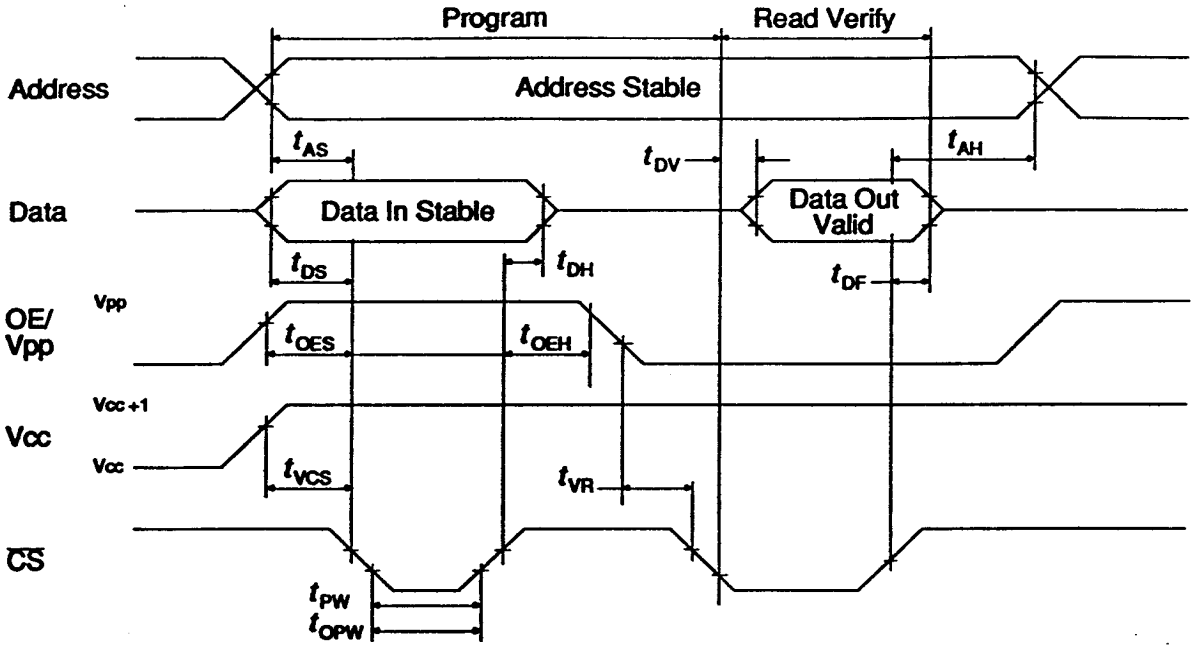
Notes (1) $V_{CC}$ must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$
(2) Defines the time at which the output achieves the open circuit condition and is no longer driven. This parameter is not measured but guaranteed by design.
(3) Initial program pulse width tolerance is 1 ms ± 5%.
(4) Length of this pulse may vary as a function of the iteration counter value n.

### AC Test Conditions

* Input pulse levels: 0.45V to 2.4V
* Input rise and fall times: ≤ 20ns
* Input and Output timing reference levels: 0.8V and 2.0V

## Programming Cycle Timing Waveform

### Single Byte Programming



## HIGH PERFORMANCE PROGRAMMING ALGORITHM

The PUMA2U2000 can be programmed using the alogorithm shown below. This allows faster programming times without stressing the device or causing deterioration in Data Retention Time.

Although the flow chart specifically refers to a single EPROM, all four devices on the PUMA tile can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode. Obviously 32 bit mode is potentially the fastest programming time, but this makes greater demands on the Vpp Supply Current.

### Programming Algorithm

Two $\overline{CS}$ pulse widths are used to program, initial and overprogram. The address inputs are set to address the desired byte. $V_{CC}$ is raised to 6.0V and $\overline{OE}$/Vpp is raised to 12.5v. The first $\overline{CS}$ pulse is 1ms. The programmed byte is then verified. If the byte is programmed successfully, then an overprogram $\overline{CS}$ pulse is applied for 3ms.

If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the address inputs are set to the next address repeating the algorithm until all required addresses are programmed. Then $V_{CC}$ and $\overline{OE}/V_{PP}$ are lowered to 5.0V All bytes subsequently are read to compare with the original data to determine if the device passes or fails.

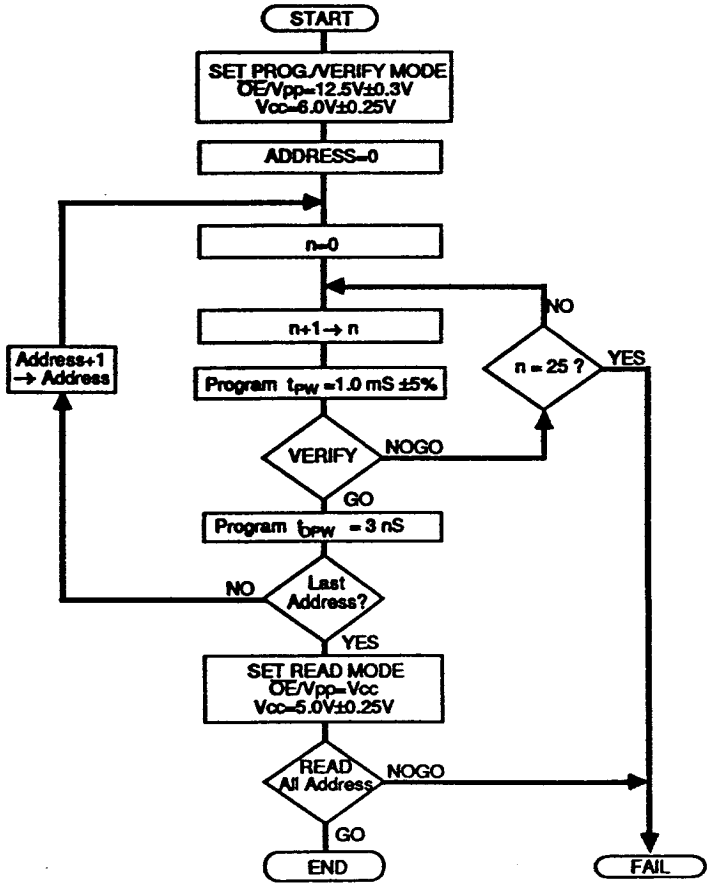
Notes:

1. $V_{CC}$ must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.

## ERASE

Erasure of the PUMA 2U2000 is performed by exposure to ultraviolet light of 2537 Å at a minimum intensity of 15WS/cm², for approximately 15 - 20 minutes.

Note that sunlight and flourescent light may contain sufficient ultraviolet light to erase the programmed information. For this reason, and anyway for any operation in the READ mode, the transparent lids on this device should be covered with an opaque label.



## Connection Table

| PGA Pin No. | Signal Name | PGA Pin No. | Signal Name | PGA Pin No. | Signal Name | PGA Pin No. | Signal Name | PGA Pin No. | Signal Name |
|---|---|---|---|---|---|---|---|---|---|
| 1 | D8 | 2 | D9 | 3 | D10 | 4 | A13 | 5 | A15 |
| 6 | NC | 7 | NC | 8 | NC | 9 | D0 | 10 | D1 |
| 11 | D2 | 12 | A14 | 13 | $\overline{CS2}$ | 14 | GND | 15 | D11 |
| 16 | A10 | 17 | A11 | 18 | A12 | 19 | Vcc | 20 | $\overline{CS1}$ |
| 21 | NC | 22 | D3 | 23 | D15 | 24 | D14 | 25 | D13 |
| 26 | D12 | 27 | $\overline{OE}$/Vpp | 28 | NC | 29 | A14 | 30 | D7 |
| 31 | D6 | 32 | D5 | 33 | D4 | 34 | D24 | 35 | D25 |
| 36 | D26 | 37 | A6 | 38 | A7 | 39 | NC | 40 | A8 |
| 41 | A9 | 42 | D16 | 43 | D17 | 44 | D18 | 45 | Vcc |
| 46 | $\overline{CS4}$ | 47 | A14 | 48 | D27 | 49 | A3 | 50 | A4 |
| 51 | A5 | 52 | A14 | 53 | $\overline{CS3}$ | 54 | GND | 55 | D19 |
| 56 | D31 | 57 | D30 | 58 | D29 | 59 | D28 | 60 | A0 |
| 61 | A1 | 62 | A2 | 63 | D23 | 64 | D22 | 65 | D21 |
| 66 | D20 | | | | | | | | |

**Note:**

**Pins 12, 29, 47 and 52 (A14) are not connected together on the PUMA substrate - they must be connected externally.**

## Military Screening Procedure

**Module Screening Flow** for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

| MB MODULE SCREENING FLOW | | |
|---|---|---|
| *SCREEN* | *TEST METHOD* | *LEVEL* |
| **Visual and Mechanical** | | |
| External visual | 2017 Condition B (or manufacturers equivalent) | 100% |
| Temperature cycle | 1010 Condition C (10 Cycles,-65°C to +150°C) | 100% |
| **Burn-In** | | |
| Pre Burn-in Electrical | Per Applicable device Specifications at $T_A$ = +25°C (optional) | 100% |
| Burn-In | Method 1015, Codition D, $T_A$ = +125°C | 100% |
| **Final Electrical Tests** | Per applicable Device Specification | |
| Static (dc) | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Functional | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Switching (ac) | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| **Percent Defective Allowable (PDA)** | Calculated at Post Burn-in at $T_A$=+25°C | 10% |
| **Quality Conformance** | Per applicable Device Specification | Sample |
| **External Visual** | 2009 Per HMP or customer specification | |

## Ordering Information

**PUMA 2U2000MB-20**

| | | |
|---|---|---|
| Speed | 12 | = 120 ns |
| | 15 | = 150 ns |
| | 17 | = 170 ns |
| | 20 | = 200 ns |
| Temp. range/screening | Blank | = Commercial Temp. |
| | I | = Industrial Temp. |
| | M | = Military Temp. |
| | MB | = Screened in accordance with MIL STD 883C |
| Memory Type | U | = UV EPROM |

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