

OKI Semiconductor

MSM514256B/BL

262,144-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM514256B/BL is a 262,144-word × 4-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM514256B/BL achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon single metal CMOS. The MSM514256B/BL is available in a 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP. The MSM514256BL (the low-power version) is specially designed for lower-power applications.

FEATURES

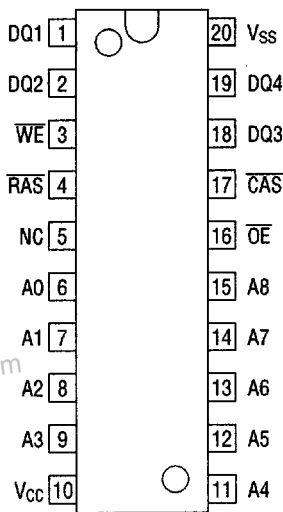
- 262,144-word × 4-bit configuration
 - Single 5 V power supply, ±10% tolerance
 - Input : TTL compatible, low input capacitance
 - Output : TTL compatible, 3-state
 - Refresh : 512 cycles/8 ms, 512 cycles/64 ms (L-version)
 - Fast page mode, read modify write capability
 - CAS before RAS refresh, hidden refresh, RAS-only refresh capability
 - Package options:

20-Pin 300 mil plastic DIP	(DIP20-P-300-W1)	(Product : MSM514256B/BL-xxRS)
26/20-Pin 300 mil plastic SOJ	(SOJ26/20-P-300)	(Product : MSM514256B/BL-xxJS)
20-Pin 400 mil plastic ZIP	(ZIP20-P-400)	(Product : MSM514256B/BL-xxZS)
- xx indicates speed rank.

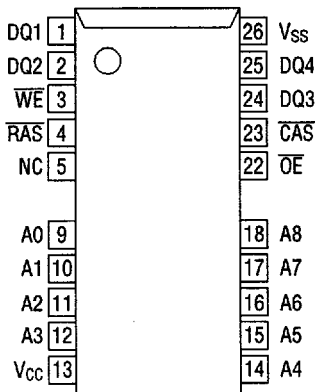
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM514256B/BL-60	60 ns	30 ns	15 ns	15 ns	120 ns	495 mW	5.5 mW/ 1.1 mW (L-version)
MSM514256B/BL-70	70 ns	35 ns	20 ns	20 ns	130 ns	440 mW	
MSM514256B/BL-80	80 ns	40 ns	20 ns	20 ns	150 ns	385 mW	
MSM514256B/BL-10	100 ns	50 ns	25 ns	25 ns	190 ns	330 mW	

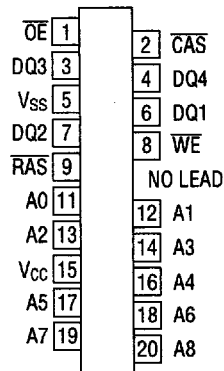
PIN CONFIGURATION (TOP VIEW)



20-Pin Plastic DIP



26/20-Pin Plastic SOJ

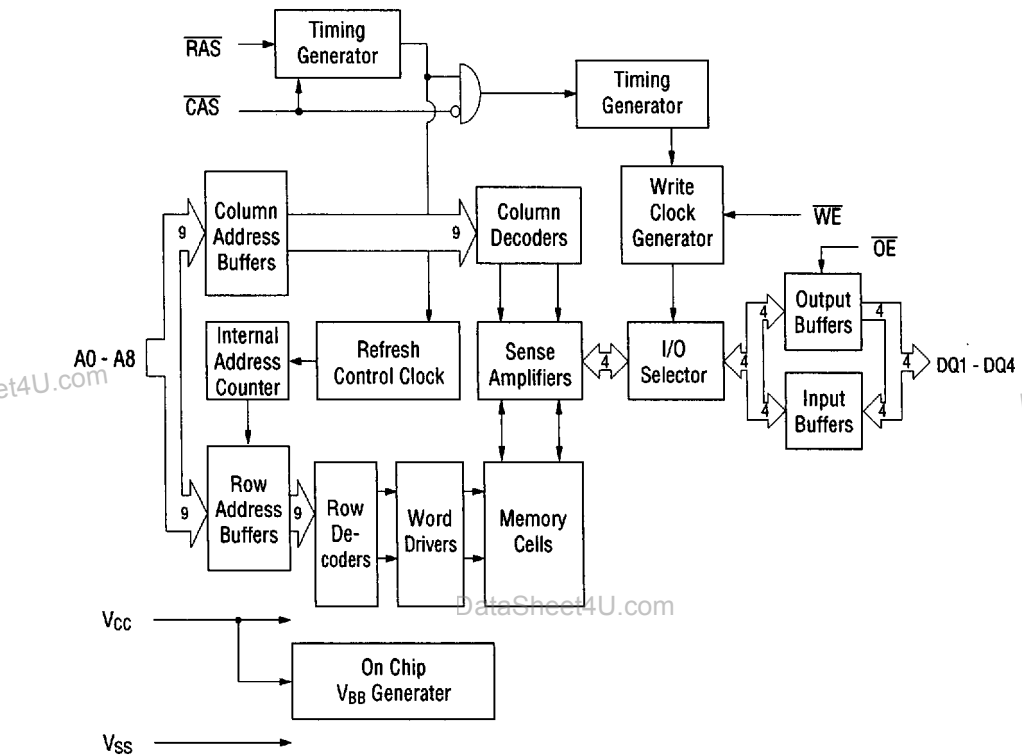


20-Pin Plastic ZIP

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Pin Name	Function
A0 - A8	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
DQ1 - DQ4	Data Input/Data Output
OE	Output Enable
WE	Write Enable
V _{CC}	Power Supply (5 V)
V _{SS}	Ground (0 V)
NC	No Connection

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-1.0 to 7.0	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	1	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	6.5	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

Capacitance

(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	C _{IN1}	—	6	pF
Input Capacitance (RAS, CAS, WE, OE)	C _{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ4)	C _{I/O}	—	7	pF

DC Characteristics

 $(V_{CC} = 5\text{ V} \pm 10\%, T_a = 0^\circ\text{C to } 70^\circ\text{C})$

Parameter	Symbol	Condition	MSM514256 B/BL-45		MSM514256 B/BL-50		MSM514256 B/BL-60		MSM514256 B/BL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	V_{OH}	$I_{OH} = -5.0\text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4		
Output Low Voltage	V_{OL}	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0\text{ V} \leq V_i \leq 6.5\text{ V};$ All other pins not under test = 0 V	-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQ disable $0\text{ V} \leq V_o \leq 5.5\text{ V}$	-10	10	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	90	—	80	—	70	—	60	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}, \overline{\text{CAS}}$ $\geq V_{CC} - 0.2\text{ V}$	—	1	—	1	—	1	—	1	μA	1, 5
		$\geq V_{CC} - 0.2\text{ V}$	—	200	—	200	—	200	—	200	μA	1, 5
Average Power Supply Current (RAS-only Refresh)	I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH},$ $t_{RC} = \text{Min.}$	—	90	—	80	—	70	—	60	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{\text{RAS}} = V_{IH},$ $\overline{\text{CAS}} = V_{IL},$ DQ = enable	—	5	—	5	—	5	—	5	mA	1
Average Power Supply Current (CAS before RAS Refresh)	I_{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	90	—	80	—	70	—	60	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{\text{RAS}} = V_{IL},$ $\overline{\text{CAS}}$ cycling, $t_{PC} = \text{Min.}$	—	80	—	70	—	60	—	55	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	$t_{RC} = 125\text{ }\mu\text{s},$ $\overline{\text{CAS}}$ before $\overline{\text{RAS}},$ $t_{RAS} \leq 1\text{ }\mu\text{s}$	—	300	—	300	—	300	—	300	μA	1, 2, 4, 5

- Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.
 4. $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}, -1.0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$.
 5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM514256 B/BL-60		MSM514256 B/BL-70		MSM514256 B/BL-80		MSM514256 B/BL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
		Random Read or Write Cycle Time	t _{RC}	120	—	130	—	150	—		
Read Modify Write Cycle Time	t _{RWC}	170	—	185	—	205	—	225	—	ns	
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	60	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	60	—	70	—	75	—	90	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	—	100	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	—	50	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	—	45	—	55	ns	4
Access Time from $\overline{\text{OE}}$	t _{OEa}	—	15	—	20	—	20	—	25	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{OFF}	0	15	0	20	0	20	0	25	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	15	0	20	0	20	0	25	ns	7
Transition Time	t _T	3	50	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	8	—	8	—	8	—	8	ms	
Refresh Period (L-version)	t _{REF}	—	64	—	64	—	64	—	64	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50	—	50	—	60	—	80	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	10	—	10	—	10	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{RHCP}	35	—	40	—	45	—	55	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	20	60	25	75	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	20	50	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	20	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	50	—	55	—	60	—	75	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	50	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ± 10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM514256 C/CL-60		MSM514256 C/CL-70		MSM514256 C/CL-80		MSM514256 C/CL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
		Read Command Set-up Time	t _{RCs}	0	—	0	—	0	—		
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t _{WCs}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t _{WCH}	10	—	15	—	15	—	20	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	50	—	55	—	60	—	75	—	ns	
Write Command Pulse Width	t _{WP}	10	—	15	—	15	—	20	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEh}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	20	—	ns	10
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	50	—	55	—	60	—	75	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t _{oED}	15	—	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	50	—	50	—	50	—	60	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	60	—	65	—	70	—	85	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	90	—	100	—	110	—	135	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	65	—	70	—	75	—	90	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	30	—	30	—	30	—	30	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t _{CPT}	40	—	40	—	40	—	50	—	ns	

- Notes:
1. A start-up delay of 100 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle, and to $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle or a read modify write cycle.