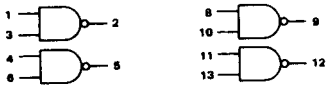
MC1048
MC1248

Four 2-input gates designed to provide four NAND functions. The output is low if and only if the two inputs are at a high logic level.

POSITIVE LOGIC



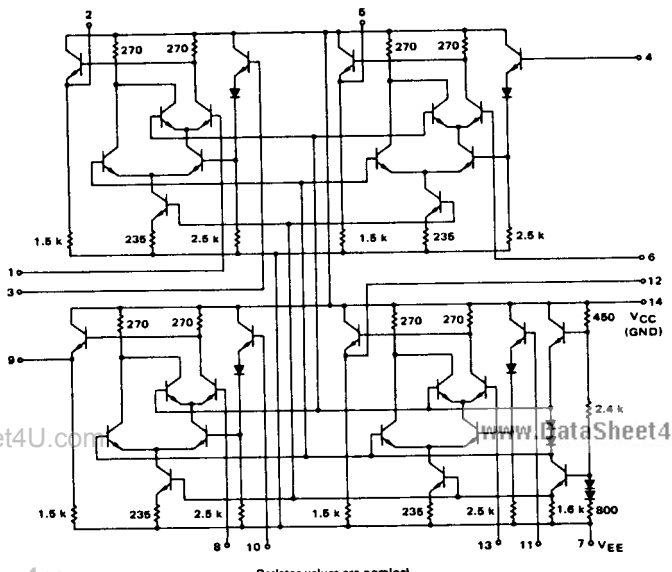
$2 = \overline{1 \cdot 3}$

DC Input Loading Factor: Pins 1, 6, 8, 13 = 1.5
Pins 3, 4, 10, 11 = 1
DC Output Loading Factor = 25
Power Dissipation = 130 mW typical

NAND GATE
SAMPLE TRUTH TABLE

Pin No.	Inputs		Output
	1	3	2
	0	0	1
	0	1	1
	1	0	1
	1	1	0

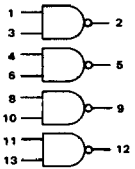
CIRCUIT SCHEMATIC



Resistor values are nominal

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner

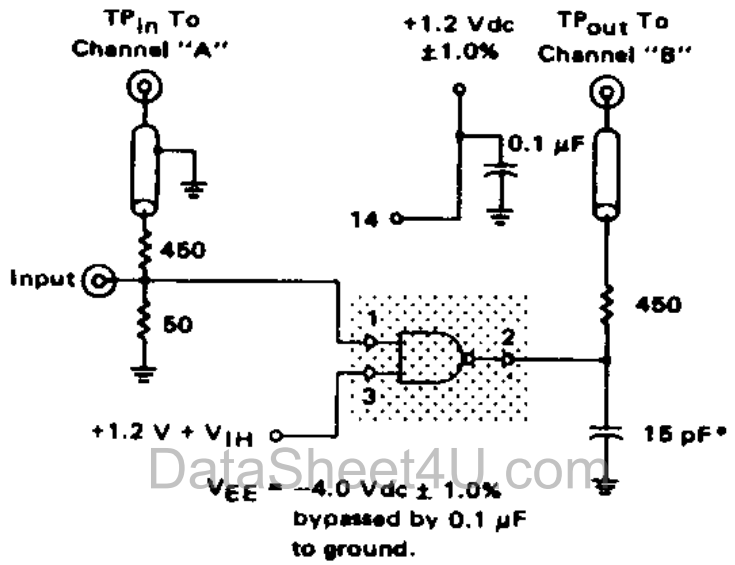


@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1248	−55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1048	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	MC1248 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1048 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-		36	-	-	mAdc	-	-	-	1,3,4,6,7,8,10,11,13	-	14
Input Current	I_{in}	1	-	-	-	150	-	-	µAdc	-	-		150	-	-	µAdc	-	3	1	7	-	14
		3	-	-	-	100	-	-	µAdc	-	-		100	-	-	µAdc	-	-	3	1,7	-	14
Input Leakage Current	I_R	1	-	-	-	0.2	-	1.0	µAdc	-	-		0.2	-	1.0	µAdc	-	-	-	1,3,7	-	14
		3	-	-	-	0.2	-	1.0	µAdc	-	-		0.2	-	1.0	µAdc	-	-	-	1,3,7	-	14
Logical "1" Output Voltage	V_{OH}[1]	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	1,3	-	-	7	2	14
			↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓		1	3	-	↓	↓	↓
																	3	1	-			
Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	-	1,3	-	7	-	14
Switching Times (Fan-Out =3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max		(+1.2 Vdc)	(+1.2 Vdc)	Pulse In	V_{EE} = −4.0 Vdc	Pulse Out	(+1.2 Vdc)
Propagation Delay	t_{PLH}	2	5.0	8.5	5.0	8.5	6.0	10	ns	5.0	8.5	5.0	8.5	6.0	9.0	ns	-	3	1	7	2	14
	t_{PHL}			6.0		8.0		9.0			8.0		8.0	5.0	8.5		-	3	1			
	t_{PLH}			8.5		8.5		10			8.5		8.5	6.0	9.0		-	1	3			
	t_{PHL}			8.0		8.0		9.0			8.0		8.0	5.0	8.5		-	1	3			
Rise Time	t_r			8.5		8.5		9.5			8.5		8.5	6.0	9.0		-	3	1			
Fall Time	t_f			8.5		8.5		10			8.5		8.5	6.0	9.0		-	3	1			

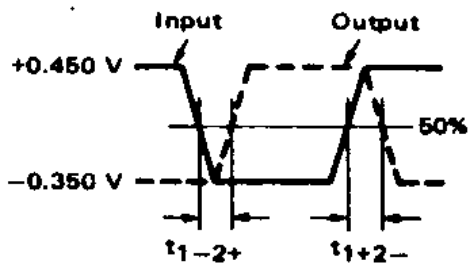
[1] V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

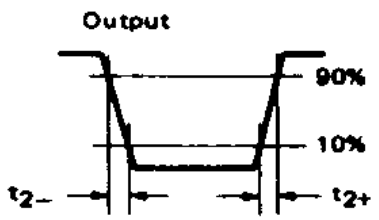


*Load Corresponds To Fan-Out = 3
Input pulse t_r and t_f = 5.0 ±0.5 ns

PROPAGATION DELAY



RISE AND FALL TIMES

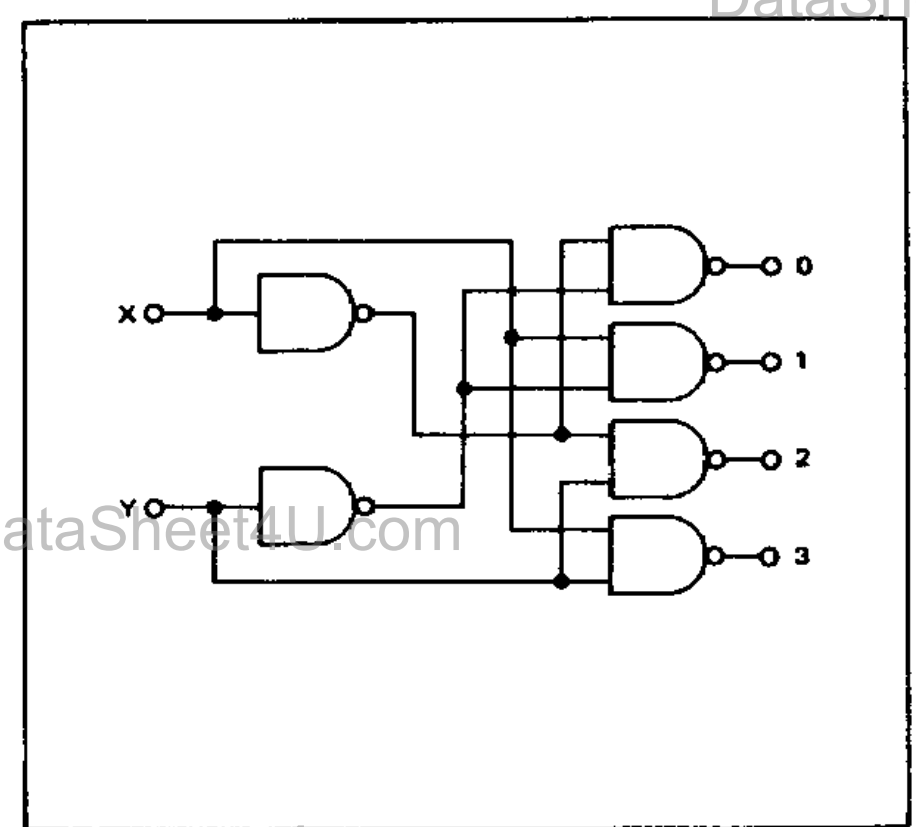


Switching waveforms shown for pulse in on pin 1 and pulse out on pin 2, however all other input-output combinations will meet the limits specified.

APPLICATIONS INFORMATION

The MC1048/1248 Quad 2-input NAND gate adds another logic function to the existing MECL II family. This gate uses series gating techniques to perform the NAND function in typically 5.0 ns. Two applications illustrating the usefulness of the NAND gate are shown below.

BINARY TO ONE-OF-FOUR LINE DECODER



DUAL R-S FLIP-FLOP USING ONE MC1048/MC1248