MEMORY Mobile FCRAM™

CMOS

128M Bit (8M word x 16 bit)

Mobile Phone Application Specific Memory

MB82DBR08163A-70L

CMOS 8,388,608-WORD x 16 BIT
Fast Cycle Random Access Memory
with Low Power SRAM Interface
Programmable Page Mode & Burst Mode

■ DESCRIPTION

The Fujitsu MB82DBR08163A is a CMOS Fast Cycle Random Access Memory (FCRAM) with asynchronous Static Random Access Memory (SRAM) interface containing 134,217,728 storages accessible in a 16-bit format. The MB82DBR08163A adopts asynchronous page mode and synchronous burst mode for fast memory access as user configurable options. The MB82DBR08163A is suited for mobile applications such as Cellular Handset and PDA.

■ FEATURES

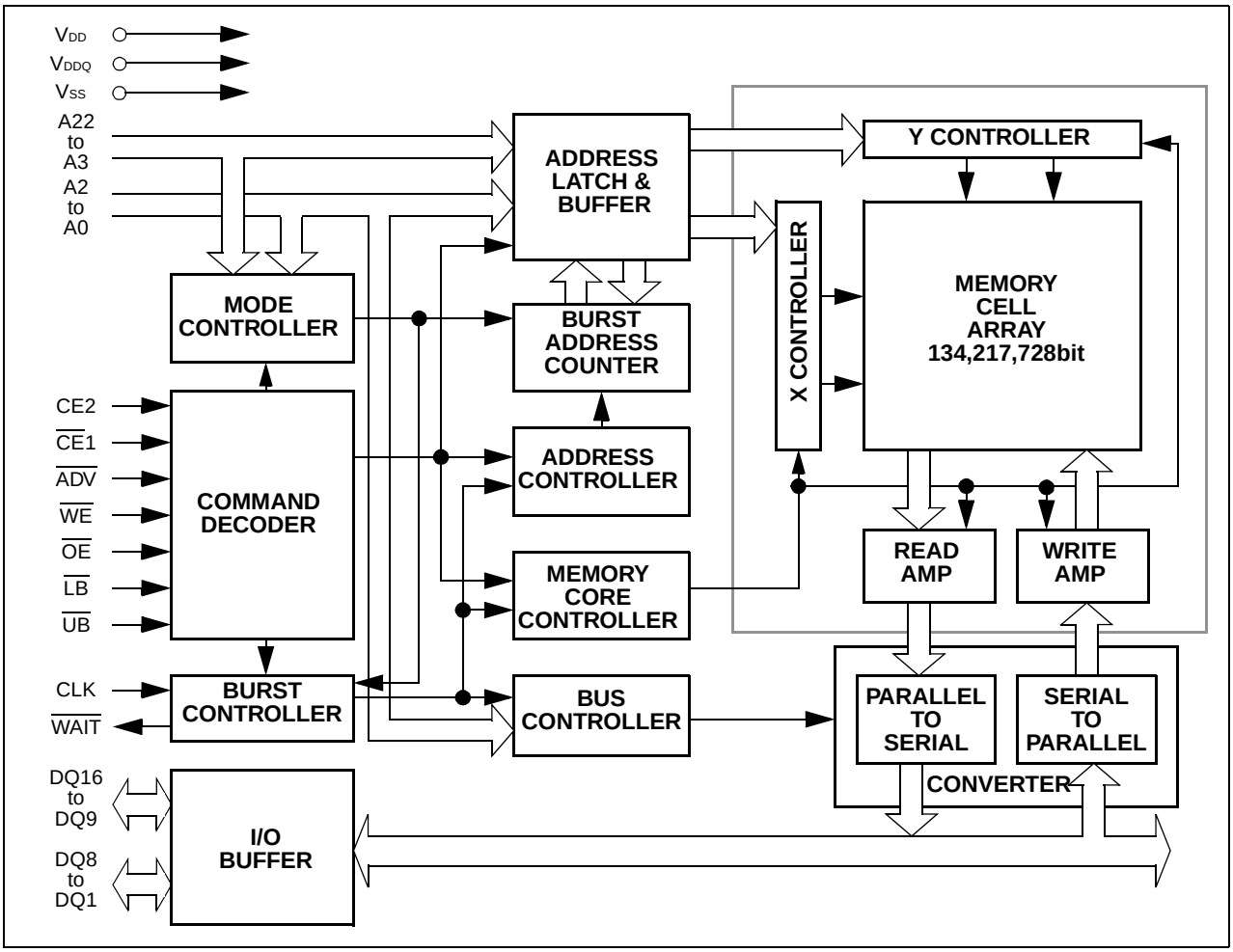
- Fast Access Cycle Time
  t_{CE} = 70ns max
- 8 words Page Read Access Capability
  t_{PAA} = 20ns max
- Burst Read/Write Access Capability
  t_{AC} = 11ns max
- Low Voltage Operating Condition
  V_{DD} = +2.6 to +3.1V
- V_{DDQ} = +1.65V to +1.95V
- Wide Operating Temperature
  T_A = -30°C to +85°C
- Byte Control by $\overline{UB}$ and $\overline{LB}$
- Low Power Consumption
  I_{DDA1} = 35mA max
  I_{DDS1} = 300 µA max
- Various Power Down mode
  Sleep, 16M-bit and 32M-bit Partial

Notice: FCRAM is a trademark of Fujitsu Limited, Japan

■ PIN DESCRIPTION

Pin Name	Description
A_{22} to A_0	Address Input
$\overline{CE1}$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
CLK	Clock Input
$\overline{ADV}$	Address Valid Input (Low Active)
$\overline{WAIT}$	Wait Signal Output
DQ_{16-9}	Upper Byte Data Input/Output
DQ_{8-1}	Lower Byte Data Input/Output
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Asynchronous Operation (Page Mode)

Mode	Note	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A22-0	DQ8-1	DQ16-9	$\overline{WAIT}$
Standby (Deselect)		H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Output Disable	*1	H	L	X	*3	H	H	X	X	*5	High-Z	High-Z	High-Z
Output Disable (No Read)				X	*3	H	L	H	H	Valid	High-Z	High-Z	High-Z
Read (Upper Byte)				X	*3	H	L	H	L	Valid	High-Z	Output Valid	High-Z
Read (Lower Byte)				X	*3	H	L	L	H	Valid	Output Valid	High-Z	High-Z
Read (Word)				X	*3	H	L	L	L	Valid	Output Valid	Output Valid	High-Z
Page Read				X	*3	H	L	L/H	L/H	Valid	*6	*6	High-Z
No Write				X	*3	L	H*4	H	H	Valid	Invalid	Invalid	High-Z
Write (Upper Byte)				X	*3	L	H*4	H	L	Valid	Invalid	Input Valid	High-Z
Write (Lower Byte)				X	*3	L	H*4	L	H	Valid	Input Valid	Invalid	High-Z
Write (Word)				X	*3	L	H*4	L	L	Valid	Input Valid	Input Valid	High-Z
Power Down	*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Notes L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

*1: Should not be kept this logic condition longer than 1µs.
Please contact local FUJITSU representative for the relaxation of 1µs limitation.

*2: Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.
Data retention depends on the selection of Partial Size.
Refer to "Power Down" in FUNCTIONAL DESCRIPTION for the details.

*3: "L" for address pass through and "H" for address latch on the rising edge of $\overline{ADV}$.

*4: $\overline{OE}$ can be V_{IL} during Write operation if the following conditions are satisfied;
(1) Write pulse is initiated by $\overline{CE1}$ (refer to $\overline{CE1}$ Controlled Write timing), or cycle time of the previous operation cycle is satisfied.
(2) $\overline{OE}$ stays V_{IL} during Write cycle.

*5: Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

*6: Output is either Valid or High-Z depending on the level of $\overline{UB}$ and $\overline{LB}$ input.

■ FUNCTION TRUTH TABLE (Continued)

Synchronous Operation (Burst Mode)

Mode	Note	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A22-0	DQ8-1	DQ16-9	$\overline{WAIT}$
Standby (Deselect)		H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Start Address Latch	*1	H	L	*3 ↑	↓	*4 X	*4 X	*6 X	*6 X	*7 Valid	*8 High-Z	*8 High-Z	*11 High-Z
Advance Burst Read to Next Address	*1	H	L	*3 ↑	H	H	L	*6 X	*6 X	X	*9 Output Valid	*9 Output Valid	Output Valid
Burst Read Suspend	*1	H	L	*3 ↑	H	H	H	*6 X	*6 X	X	High-Z	High-Z	*12 High
Advance Burst Write to Next Address	*1	H	L	*3 ↑	H	*5 L	H	*6 X	*6 X	X	*10 Input Valid	*10 Input Valid	*13 High
Burst Write Suspend	*1	H	L	*3 ↑	H	*5 H	H	*6 X	*6 X	X	Input Invalid	Input Invalid	*12 High
Terminate Burst Read		H	↑	X	H	H	X	*6 X	*6 X	X	High-Z	High-Z	High-Z
Terminate Burst Write		H	↑	X	H	X	H	*6 X	*6 X	X	High-Z	High-Z	High-Z
Power Down	*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Notes L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, ↑ = valid edge, ↓ = positive edge of Low pulse, High-Z = High Impedance

*1: Should not be kept this logic condition longer than 4µs.
Please contact local FUJITSU representative for the relaxation of 4µs limitation.

*2: Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.
Data retention depends on the selection of Partial Size.
Refer to "Power Down" in FUNCTIONAL DESCRIPTION for the details.

*3: Valid clock edge shall be set on either positive or negative edge through CR Set. CLK must be started and stable prior to memory access.

*4: Can be either V_{IL} or V_{IH} except for the case the both of $\overline{OE}$ and $\overline{WE}$ are V_{IL}. It is prohibited to bring the both of $\overline{OE}$ and $\overline{WE}$ to V_{IL}

*5: When device is operating in "$\overline{WE}$ Single Clock Pulse Control" mode, $\overline{WE}$ is don't care once write operation is determined by $\overline{WE}$ Low Pulse at the beginning of write access together with address latching. Write suspend feature is not supported in "$\overline{WE}$ Single Clock Pulse Control" mode

*6: Can be either V_{IL} or V_{IH} but must be valid before Read or Write is determined. And once $\overline{UB}$ and $\overline{LB}$ inputs are determined, they must not be changed until the end of burst.

*7: Once valid address is determined, input address must not be changed during $\overline{ADV}$=L.

*8: If $\overline{OE}$=L, output is either Invalid or High-Z depending on the level of $\overline{UB}$ and $\overline{LB}$ input. If $\overline{WE}$=L, Input is Invalid. If $\overline{OE}$=$\overline{WE}$=H, output is High-Z.

*9: Output is either Valid or High-Z depending on the level of $\overline{UB}$ and $\overline{LB}$ input.

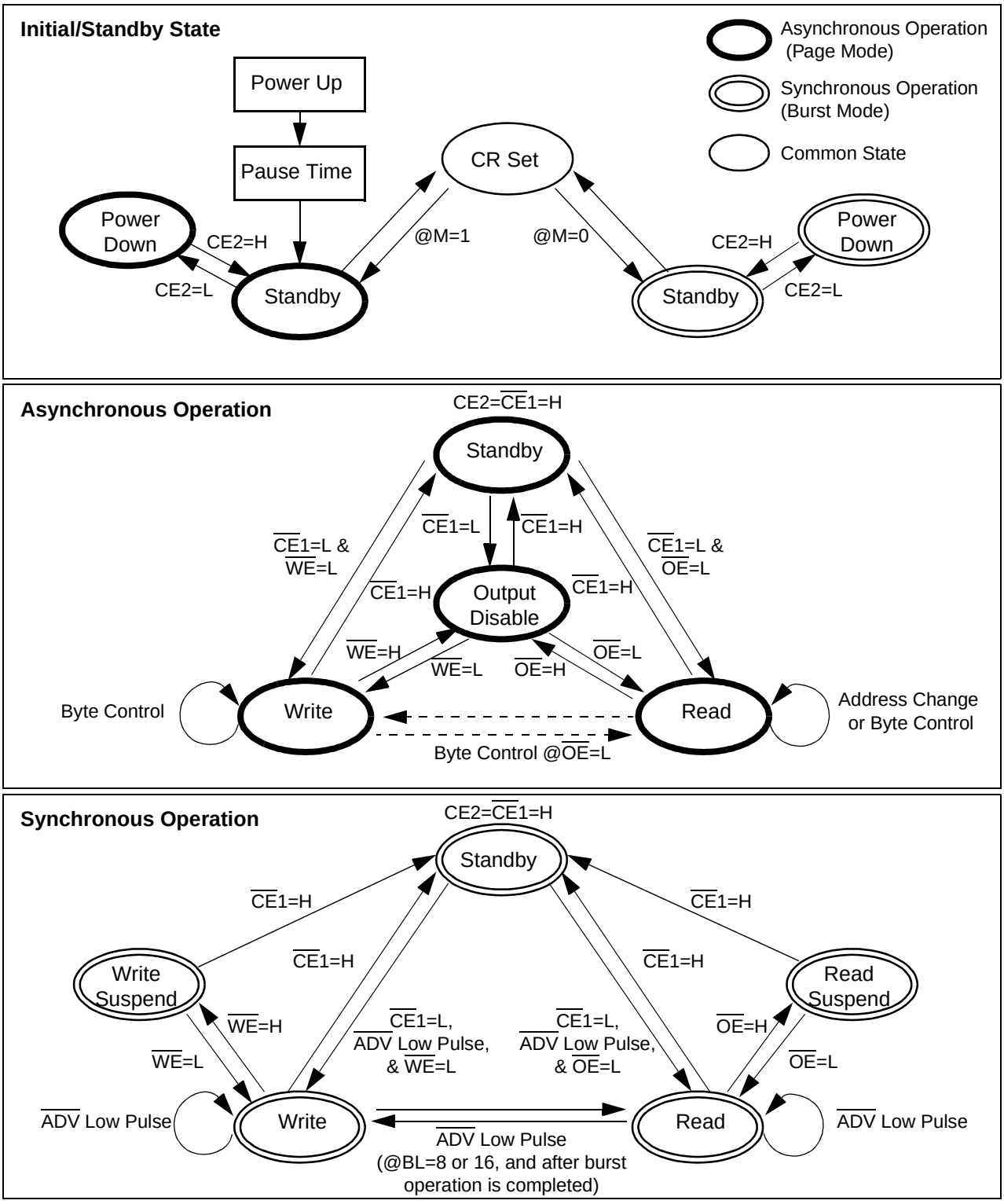
*10: Input is either Valid or Invalid depending on the level of $\overline{UB}$ and $\overline{LB}$ input.

*11: Output is either High-Z or Invalid depending on the level of $\overline{OE}$ and $\overline{WE}$ input.

*12: Keep the level from previous cycle except for suspending on last data. Refer to "$\overline{WAIT}$ Output Function" in FUNCTIONAL DESCRIPTION for the details.

*13: $\overline{WAIT}$ output is driven in High level during write operation.

■ STATE DIAGRAM



Notes Assuming all the parameters specified in AC CHARACTERISTICS are satisfied. Refer to the FUNCTIONAL DESCRIPTION, AC CHARACTERISTICS, and TIMING DIAGRAM for details.

■ FUNCTIONAL DESCRIPTION

This device supports asynchronous page read & normal write operation and synchronous burst read & burst write operation for faster memory access and features three kinds of power down modes for power saving as user configurable option.

Power-up

It is required to follow the power-up timing to start executing proper device operation. Refer to POWER-UP Timing. After Power-up, the device defaults to asynchronous page read & normal write operation mode with sleep power down feature.

Configuration Register

The Configuration Register (CR) is used to configure the type of device function among optional features. Each selection of features is set through CR Set sequence after Power-up. If CR Set sequence is not performed after power-up, the device is configured for asynchronous operation with sleep power down feature as default configuration

CR Set Sequence

The CR Set requires total 6 read/write operations with unique address. Between each read/write operation requires that device being in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	7FFFFFh (MSB)	Read Data (RDa)
2nd	Write	7FFFFFh	RDa
3rd	Write	7FFFFFh	RDa
4th	Write	7FFFFFh	X
5th	Write	7FFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address (MSB).
The second and third cycle are to write back the data (RDa) read by first cycle. If the second or third cycle is written into the different address, the CR Set is cancelled and the data written by the second or third cycle is valid as a normal write operation.
The forth and fifth cycle is to write to MSB. The data of forth and fifth cycle is don't-care. If the forth or fifth cycle is written into different address, the CR Set is also cancelled but write data may not be written as normal write operation.
The last cycle is to read from specific address key for mode selection. And read data (RDb) is invalid.

Once this CR Set sequence is performed from an initial CR set to the other new CR set, the written data stored in memory cell array may be lost. So, it should perform the CR Set sequence prior to regular read/ write operation if necessary to change from default configuration.

■ FUNCTIONAL DESCRIPTION (Continued)

Address Key

The address key has the following format.

Address Pin	Register Name	Function	Key	Description	Note
A22-A21	—	—	1	Unused bits muse be 1	*1
A20-A19	PS	Partial Size	00	32M Partial	
			01	16M Partial	
			10	Reserved for future use	*2
			11	Sleep [Default]	
A18-A16	BL	Burst Length	000	Reserved for future use	*2
			001	Reserved for future use	*2
			010	8 words	
			011	16 words	
			100	Reserved for future use	*2
			101	Reserved for future use	*2
			110	Reserved for future use	*2
			111	Continuous	
A15	M	Mode	0	Synchronous Mode (Burst Read / Write)	*3
			1	Asynchronous Mode [Default] (Page Read / Normal Write)	*4
A14-A12	RL	Read Latency	000	Reserved for future use	*2
			001	3 clocks	
			010	4 clocks	
			011	5 clocks	
			1xx	Reserved for future use	*2
A11	BS	Burst Sequence	0	Reserved for future use	*2
			1	Sequential	
A10	SW	Single Write	0	Burst Read & Burst Write	
			1	Burst Read & Single Write	*5
A9	VE	Valid Clock Edge	0	Falling Clock Edge	
			1	Rising Clock Edge	
A8	—	—	1	Unused bits muse be 1	*1
A7	WC	Write Control	0	$\overline{WE}$ Single Clock Pulse Control without Write Suspend Function	*5
			1	$\overline{WE}$ Level Control with Write Suspend Function	
A6-A0	—	—	1	Unused bits muse be 1	*1

Notes *1: A22, A21, A8, and A6 to A0 must be all "1" in any cases.

*2: It is prohibited to apply this key.

*3: If M=0, all the registers must be set with appropriate Key input at the same time.

*4: If M=1, PS must be set with appropriate Key input at the same time. Except for PS, all the other key inputs must be "1".

*5: Burst Read & Single Write is not supported at $\overline{WE}$ Single Clock Pulse Control.

■ FUNCTIONAL DESCRIPTION (Continued)

Power Down

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept low. CE2 High resume the device from power down mode.

This device has three power down modes, Sleep, 16M Partial, and 32M Partial.
The selection of power down mode is set through CR Set sequence. Each mode has following data retention features.

Mode	Data Retention Size	Retention Address
Sleep [default]	No	N/A
16M Partial	16M bit	000000h to 0FFFFFh
32M Partial	32M bit	000000h to 1FFFFFh

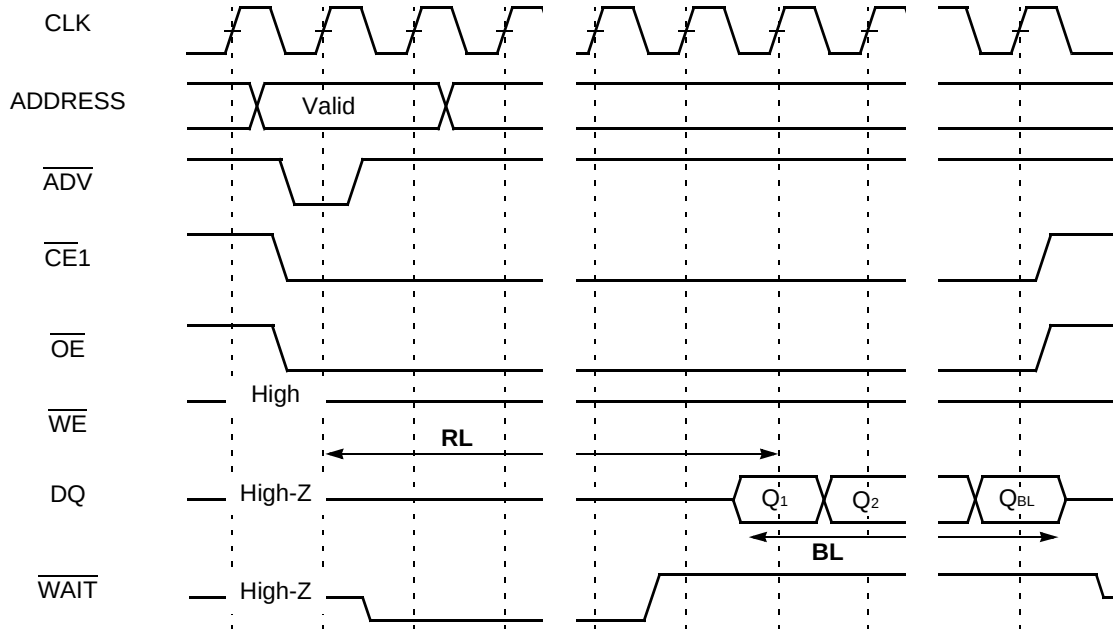
The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to perform CR Set sequence to set to Sleep mode after power-up in case of asynchronous operation.

■ FUNCTIONAL DESCRIPTION (Continued)

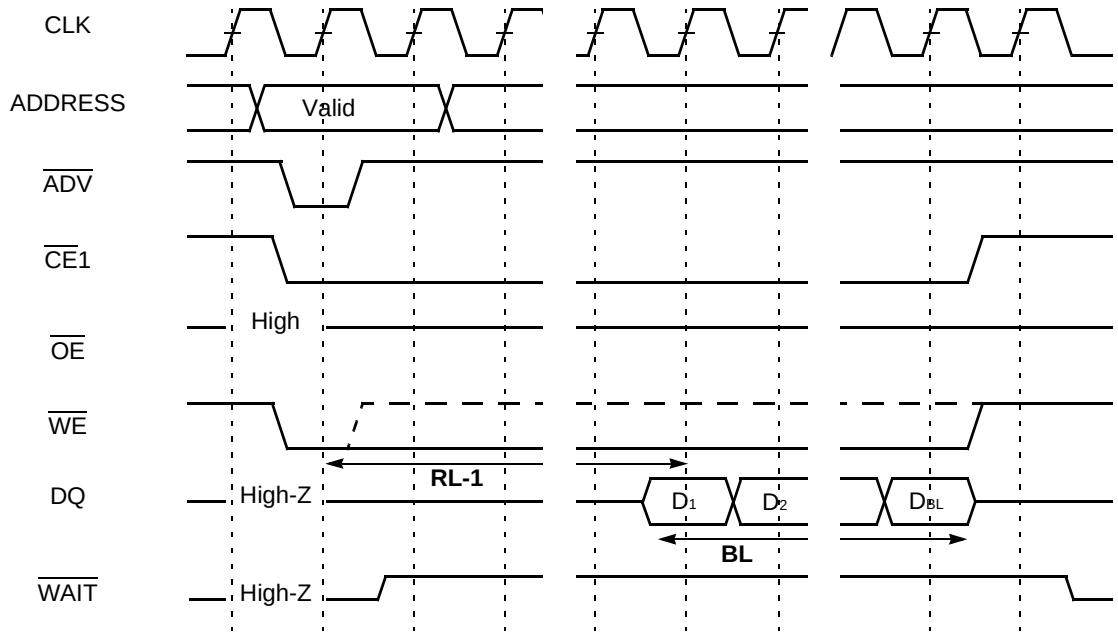
Burst Read/Write Operation

Synchronous burst read/write operation provides faster memory access that synchronized to microcontroller or system bus frequency. Configuration Register Set is required to perform burst read & write operation after power-up. Once CR Set sequence is performed to select synchronous burst mode, the device is configured to synchronous burst read/write operation mode with corresponding RL and BL that is set through CR Set sequence together with operation mode. In order to perform synchronous burst read & write operation, it is required to control new signals, CLK, $\overline{ADV}$ and $\overline{WAIT}$ that Low Power SRAMs don't have.

Burst Read Operation



Burst Write Operation



■ FUNCTIONAL DESCRIPTION (Continued)

CLK Input Function

The CLK is input signal to synchronize memory to microcontroller or system bus frequency during synchronous burst read & write operation. The CLK input increments device internal address counter and the valid edge of CLK is referred for latency counts from address latch, burst write data latch, and burst read data out. During synchronous operation mode, CLK input must be supplied except for standby state and power down state. CLK is don't care during asynchronous operation.

$\overline{\text{ADV}}$ Input Function

The $\overline{\text{ADV}}$ is input signal to indicate valid address presence on address inputs. It is applicable to synchronous operation as well as asynchronous operation. $\overline{\text{ADV}}$ input is active during $\overline{\text{CE}}$1=L and $\overline{\text{CE}}$1=H disables $\overline{\text{ADV}}$ input. All addresses are determined on the positive edge of $\overline{\text{ADV}}$.

During synchronous burst read/write operation, $\overline{\text{ADV}}$=H disables all address inputs. Once $\overline{\text{ADV}}$ is brought to High after valid address latch, it is inhibited to bring $\overline{\text{ADV}}$ Low until the end of burst or until burst operation is terminated. $\overline{\text{ADV}}$ Low pulse is mandatory for synchronous burst read/write operation mode to latch the valid address input.

During asynchronous operation, $\overline{\text{ADV}}$=H also disables all address inputs. $\overline{\text{ADV}}$ can be tied to Low during asynchronous operation and it is not necessary to control $\overline{\text{ADV}}$ to High.

$\overline{\text{WAIT}}$ Output Function

The $\overline{\text{WAIT}}$ is output signal to indicate data bus status when the device is operating in synchronous burst mode.

During burst read operation, $\overline{\text{WAIT}}$ output is enabled after specified time duration from $\overline{\text{OE}}$=L. $\overline{\text{WAIT}}$ output Low indicates data out at next clock cycle is invalid, and $\overline{\text{WAIT}}$ output becomes High one clock cycle prior to valid data out. During $\overline{\text{OE}}$ read suspend, $\overline{\text{WAIT}}$ output doesn't indicate data bus status but carries the same level from previous clock cycle (kept High) except for read suspend on the final data output. If final read data out is suspended, $\overline{\text{WAIT}}$ output become high impedance after specified time duration from $\overline{\text{OE}}$=H.

During burst write operation, $\overline{\text{WAIT}}$ output is enabled to High level after specified time duration from $\overline{\text{WE}}$=L and kept High for entire write cycles including $\overline{\text{WE}}$ write suspend. The actual write data latching starts on the appropriate clock edge with respect to Valid Clock Edge, Read Latency and Burst Length. During $\overline{\text{WE}}$ write suspend, $\overline{\text{WAIT}}$ output doesn't indicate data bus status but carries the same level from previous clock cycle (kept High) except for write suspend on the final data input. If final write data in is suspended, $\overline{\text{WAIT}}$ output become high impedance after specified time duration from $\overline{\text{WE}}$=H.

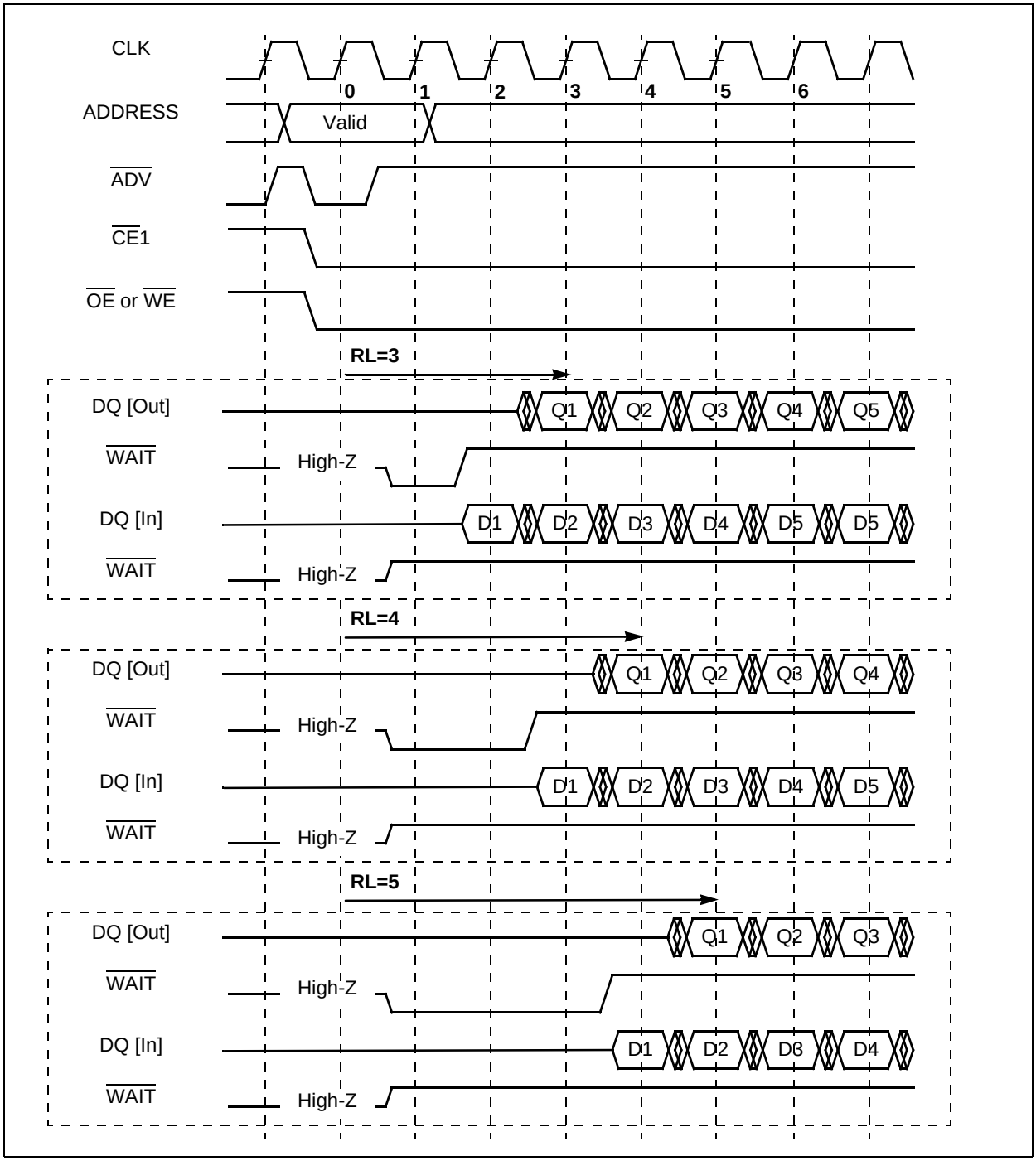
This device doesn't incur additional delay against crossing device-row boundary or internal refresh operation. Therefore, the burst operation is always started after fixed latency with respect to Read Latency. And there is no waiting cycle asserted in the middle of burst operation except for burst suspend by $\overline{\text{OE}}$ brought to High or $\overline{\text{WE}}$ brought to High. Thus, once $\overline{\text{WAIT}}$ output is enabled and brought to High, $\overline{\text{WAIT}}$ output keep High level until the end of burst or until the burst operation is terminated.

When the device is operating in asynchronous mode, $\overline{\text{WAIT}}$ output is always in High Impedance.

■ FUNCTIONAL DESCRIPTION (Continued)

Latency

Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through CR Set sequence after power-up. Once specific RL is set through CR Set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL-1. The burst operation is always started after fixed latency with respect to Read Latency set in CR.



■ FUNCTIONAL DESCRIPTION (Continued)

Address Latch by $\overline{ADV}$

The $\overline{ADV}$ indicates valid address presence on address inputs. During synchronous burst read/write operation mode, all the address are determined on the positive edge of $\overline{ADV}$ when $\overline{CE}$1=L. The specified minimum value of $\overline{ADV}$=L setup time and hold time against valid edge of clock where RL count begin must be satisfied for appropriate RL counts. Valid address must be determined with specified setup time against either the negative edge of $\overline{ADV}$ or negative edge of $\overline{CE}$1 whichever comes late. And the determined valid address must not be changed during $\overline{ADV}$=L period.

Burst Length

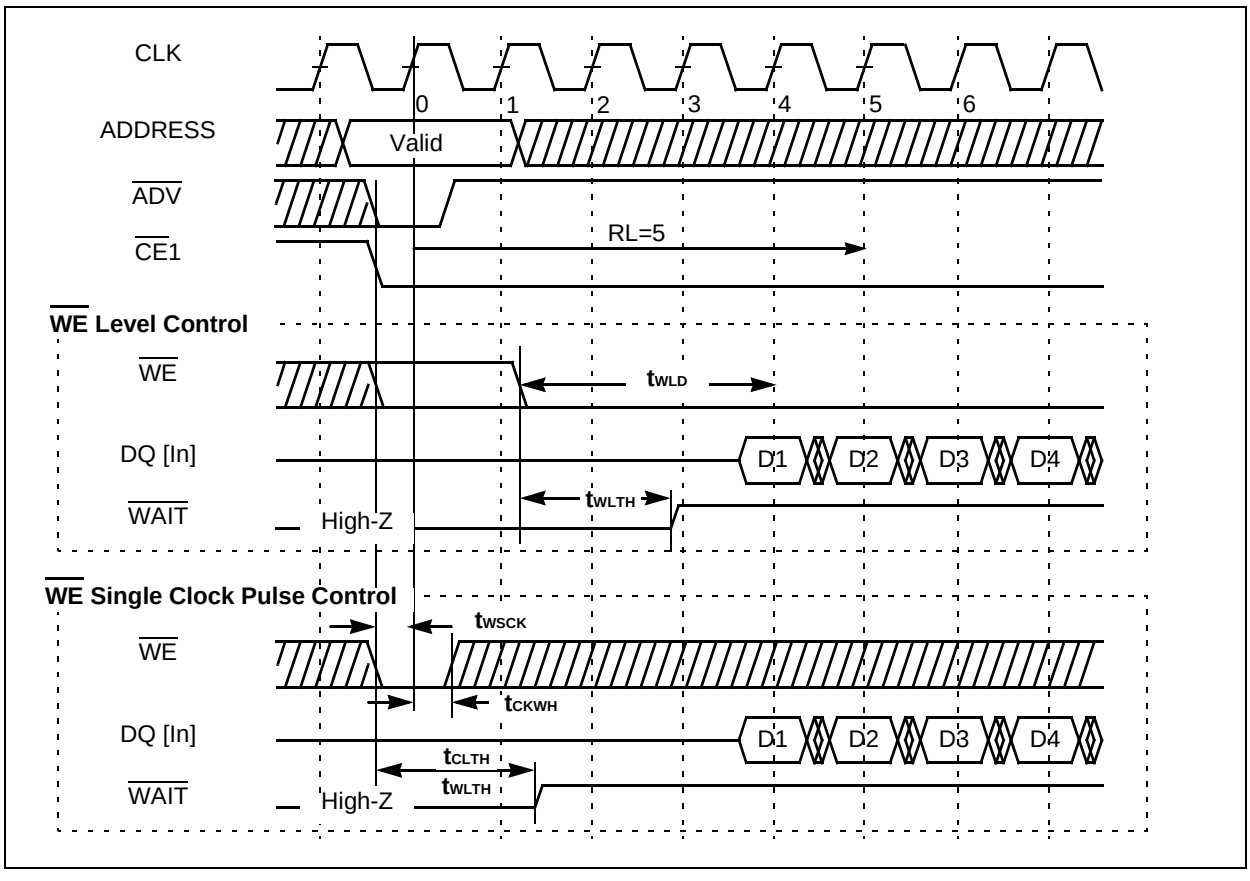
Burst Length is the number of word to be read or write during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8, 16 words boundary or continuous for entire address through CR Set sequence. The burst type is sequential that is incremental decoding scheme within a boundary address. Starting from initial address being latched, device internal address counter assign +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (=0). After completing read data out or write data latch for the set burst length, operation automatically ended except for continuous burst length. When continuous burst length is set, read/write is endless unless it is terminated by the positive edge of $\overline{CE}$1.

Single Write

Single Write is synchronous write operation with Burst Length =1. The device can be configured either to "Burst Read & Single Write" or to "Burst Read & Burst Write" through CR set sequence. Once the device is configured to "Burst Read & Single Write" mode, the burst length for synchronous write operation is always fixed 1 regardless of BL values set in CR, while burst length for read is in accordance with BL values set in CR.

Write Control

The device has two types of $\overline{WE}$ signal control method, "$\overline{WE}$ Level Control" and "$\overline{WE}$ Single Clock Pulse Control", for synchronous write operation. It is configured through CR set sequence.

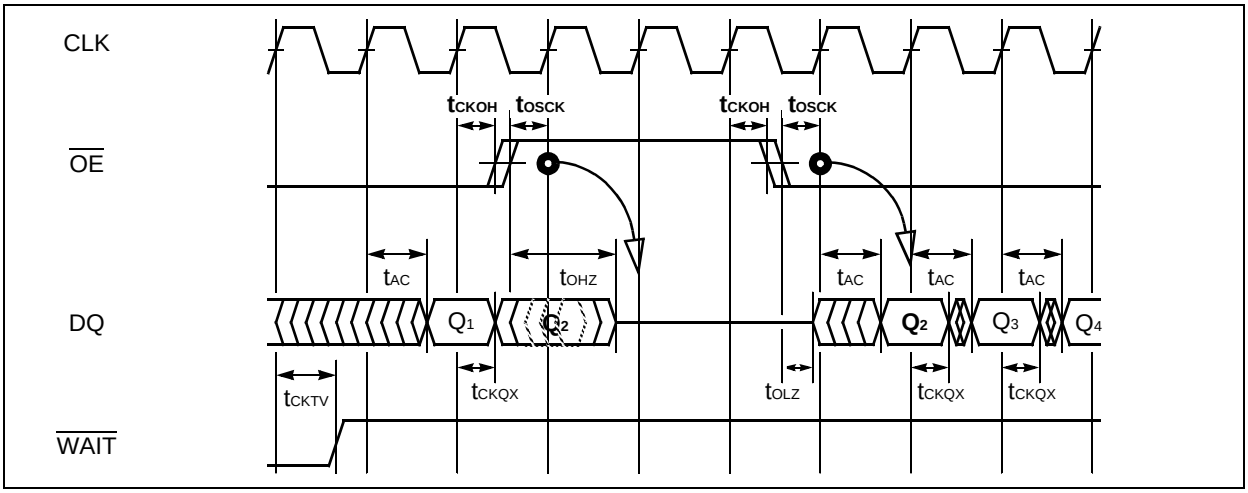


■ FUNCTIONAL DESCRIPTION (Continued)

Burst Read Suspend

Burst read operation can be suspended by $\overline{OE}$ High pulse. During burst read operation, $\overline{OE}$ brought to High suspends burst read operation. Once $\overline{OE}$ is brought to High with the specified set up time against clock where the data being suspended, the device internal counter is suspended, and the data output become high impedance after specified time duration. It is inhibited to suspend the first data out at the beginning of burst read.

$\overline{OE}$ brought to Low resumes burst read operation. Once $\overline{OE}$ is brought to Low, data output become valid after specified time duration, and internal address counter is reactivated. The last data out being suspended as the result of $\overline{OE}$=H and first data out as the result of $\overline{OE}$=L are from the same address.

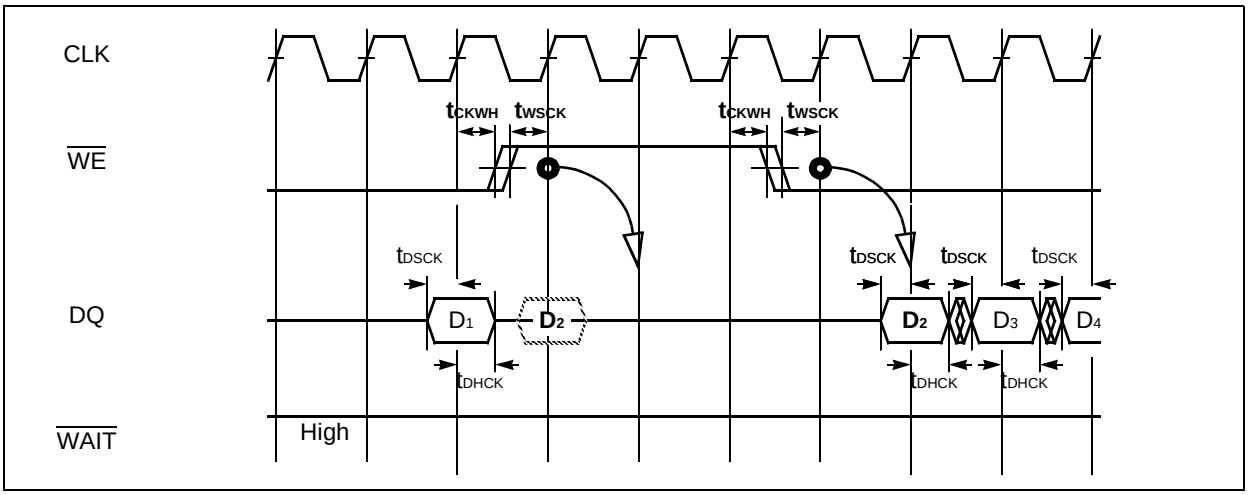


Burst Write Suspend

Burst write operation can be suspended by $\overline{WE}$ High pulse. During burst write operation, $\overline{WE}$ brought to High suspends burst write operation. Once $\overline{WE}$ is brought to High with the specified set up time against clock where the data being suspended, device internal counter is suspended, data input is ignored. It is inhibited to suspend the first data input at the beginning of burst write.

$\overline{WE}$ brought to Low resumes burst write operation. Once $\overline{WE}$ is brought to Low, data input become valid after specified time duration, and internal address counter is reactivated. The write address of the cycle where data being suspended and the first write address as the result of $\overline{WE}$=L are the same address.

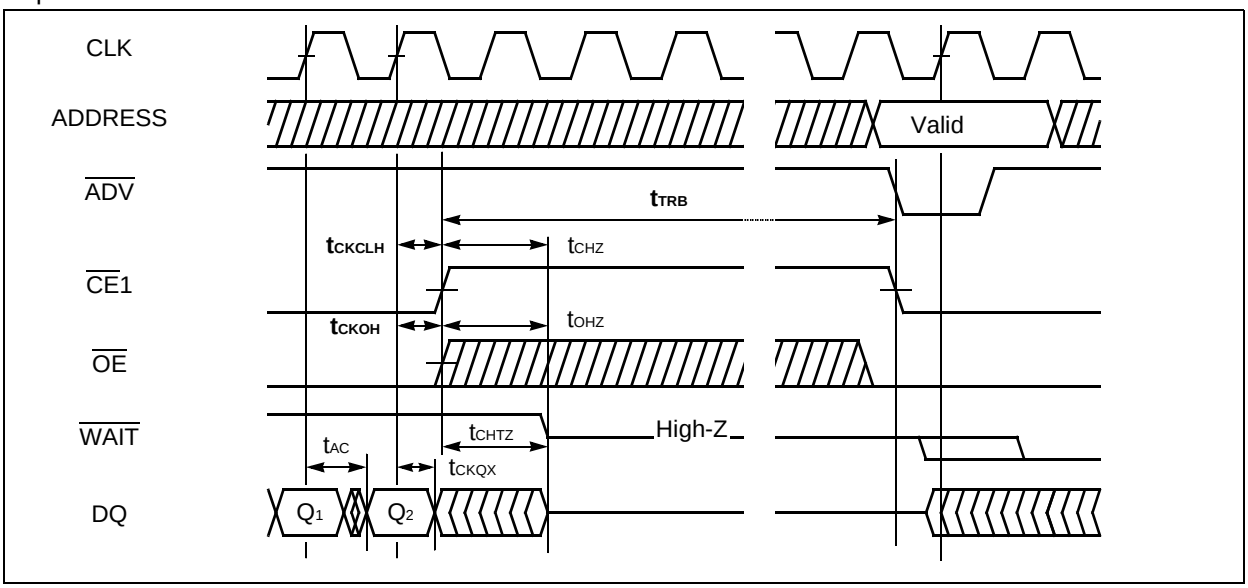
Burst write suspend function is available when the device is operating in $\overline{WE}$ level controlled burst write only.



■ FUNCTIONAL DESCRIPTION (Continued)

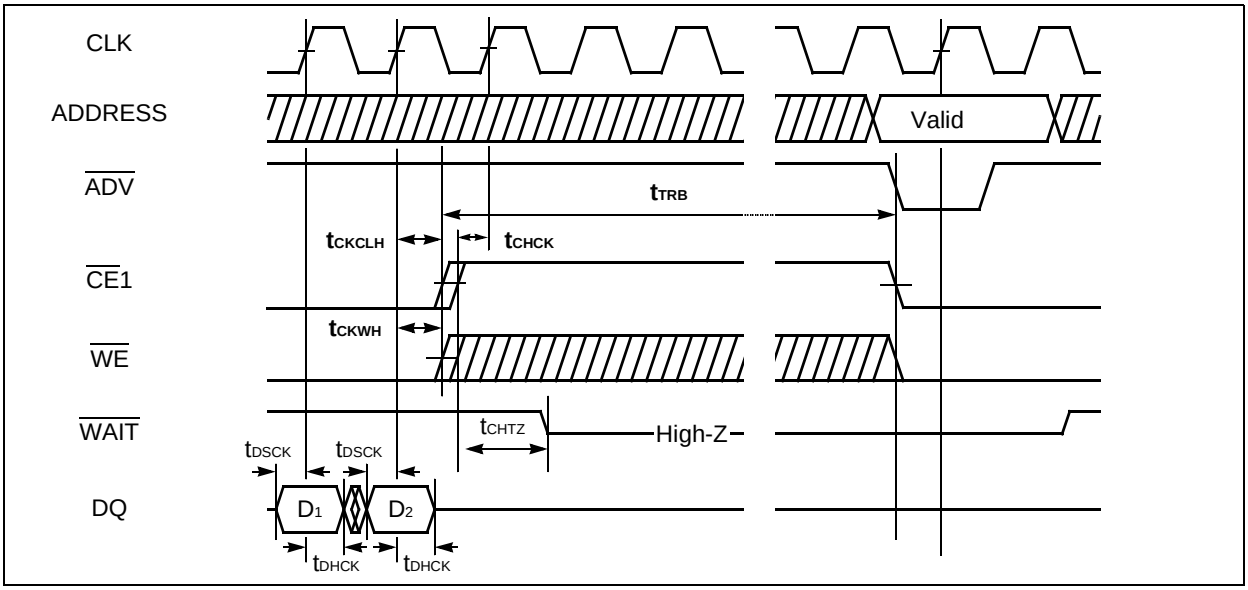
Burst Read Termination

Burst read operation can be terminated by $\overline{CE}1$ brought to High. If BL is set on Continuous, burst read operation is continued endless unless terminated by $\overline{CE}1$=H. It is inhibited to terminate burst read before first data out is completed. In order to guarantee last data output, the specified minimum value of $\overline{CE}1$=L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.



Burst Write Termination

Burst write operation can be terminated by $\overline{CE}1$ brought to High. If BL is set on Continuous, burst write operation is continued endless unless terminated by $\overline{CE}1$=H. It is inhibited to terminate burst write before first data in is completed. In order to guarantee last write data being latched, the specified minimum values of $\overline{CE}1$=L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.



■ ABSOLUTE MAXIMUM RATINGS (See WARNING below.)

Parameter	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to +3.6	V
Voltage of V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	-0.5 to +2.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +2.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS (See WARNING below.)

(Referenced to V_{SS})

Parameter	Notes	Symbol	Min.	Max.	Unit
Supply Voltage		V_{DD}	2.6	3.1	V
I/O Supply Voltage		V_{DDQ}	1.65	1.95	V
Ground		V_{SS}	0	0	V
High Level Input Voltage	*1	V_{IH}	V_{DDQ}*0.8	V_{DDQ}+0.2	V
Low Level Input Voltage	*2	V_{IL}	-0.3	V_{DDQ}*0.2	V
Ambient Temperature		T_A	-30	85	°C

Notes *1: Maximum DC voltage on input and I/O pins is V_{DDQ}+0.2V. During voltage transitions, inputs may positive overshoot to V_{DDQ}+1.0V for periods of up to 5 ns.

*2: Minimum DC voltage on input or I/O pins is -0.3V. During voltage transitions, inputs may negative overshoot V_{SS} to -1.0V for periods of up to 5ns.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ DC CHARACTERISTICS
(Under Recommended Operating Conditions unless otherwise noted) Note *1,*2,*3

Parameter	Symbol	Test Conditions		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DDQ}		-1.0	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DDQ}, Output Disable		-1.0	+1.0	µA
Output High Voltage Level	V_{OH}	V_{DDQ} = V_{DDQ}(min), I_{OH} = –0.5mA		1.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1mA		—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	V_{DD} = V_{DD} max., V_{DDQ} = V_{DDQ} max., V_{IN} = V_{IH} or V_{IL}, CE2 ≤ 0.2V	SLEEP	—	10	µA
	I_{DDP16}		16M Partial	—	120	µA
	I_{DDP32}		32M Partial	—	150	µA
V_{DD} Standby Current	I_{DDS}	V_{DD} = V_{DD} max., V_{DDQ} = V_{DDQ} max., $\overline{V_{IN}}$ (including CLK)= V_{IH} or V_{IL}, $\overline{CE1}$ = CE2 = V_{IH}		—	1.5	mA
	I_{DDS1}	V_{DD} = V_{DD} max., V_{DDQ} = V_{DDQ} max., V_{IN} (including CLK) ≤ 0.2V or $\overline{V_{IN}}$ (including CLK) ≥ V_{DDQ} – 0.2V, $\overline{CE1}$ = CE2 ≥ V_{DDQ} – 0.2V		—	300	µA
	I_{DDS2}	V_{DD} = V_{DD} max., V_{DDQ} = V_{DDQ} max., tCK=min. $\overline{V_{IN}}$ ≤ 0.2V or V_{IN} ≥ V_{DDQ} – 0.2V, $\overline{CE1}$ = CE2 ≥ V_{DDQ} – 0.2V		—	350	µA
V_{DD} Active Current	I_{DDA1}	V_{DD} = V_{DD} max., V_{DDQ} = V_{DDQ} max., $\overline{V_{IN}}$ = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA	t_{RC} / t_{WC} = minimum	—	35	mA
	I_{DDA2}		t_{RC} / t_{WC} = 1µs	—	5	mA
V_{DD} Page Read Current	I_{DDA3}	V_{DD} = V_{DD} max., $\overline{V_{DDQ}}$ = V_{DDQ} max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA, t_{PRC} = min.		—	15	mA
V_{DD} Burst Access Current	I_{DDA4}	V_{DD} = V_{DD} max., $\overline{V_{DDQ}}$ = V_{DDQ} max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, t_{CK} = t_{CK} min., BL = Continuous, I_{OUT}=0mA,		—	30	mA

Notes *1: All voltages are referenced to Vss.
*2: DC Characteristics are measured after following POWER-UP timing.
*3: I_{OUT} depends on the output load conditions.

■ AC CHARACTERISTICS
(Under Recommended Operating Conditions unless otherwise noted)

ASYNCHRONOUS READ OPERATION (PAGE MODE)

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{RC}	70	1000	ns	*1, *2
$\overline{CE}$1 Access Time	t_{CE}	—	70	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	70	ns	*3, *5
$\overline{ADV}$ Access Time	t_{AV}		70	ns	*3
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Page Address Access Time	t_{PAA}	—	20	ns	*3, *6
Page Read Cycle Time	t_{PRC}	20	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}$1 Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}$1 High to Output High-Z	t_{CHZ}	—	20	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	20	ns	*3
$\overline{LB}$, $\overline{UB}$ High to Output High-Z	t_{BHZ}	—	20	ns	*3
Address Setup Time to $\overline{CE}$1 Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*8
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	5	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5, *9
Address Hold Time from $\overline{CE}$1 High	t_{CHAH}	–5	—	ns	*10
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–5	—	ns	
$\overline{CE}$1 High Pulse Width	t_{CP}	15	—	ns	

Notes *1: Maximum value is applicable if $\overline{CE}$1 is kept at Low without change of address input of A3 to A22. If needed by system operation, please contact local FUJITSU representative for the relaxation of 1µs limitation.

*2: Address should not be changed within minimum t_{RC}.

*3: The output load 50pF with 50ohm termination to V_{DDQ}*0.5 V.

*4: The output load 5pF without any other load.

*5: Applicable to A3 to A22 when $\overline{CE}$1 is kept at Low.

*6: Applicable only to A0, A1 and A2 when $\overline{CE}$1 is kept at Low for the page address access.

*7: In case Page Read Cycle is continued with keeping $\overline{CE}$1 stays Low, $\overline{CE}$1 must be brought to High within 4µs. In other words, Page Read Cycle must be closed within 4µs.

*8: t_{VPL} is specified from the negative edge of either $\overline{CE}$1 or $\overline{ADV}$ whichever comes late.

*9: Applicable when at least two of address inputs among applicable are switched from previous state.

*10: t_{RC}(min) and t_{PRC}(min) must be satisfied.

■ AC CHARACTERISTICS (Continued)

ASYNCHRONOUS WRITE OPERATION

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{WC}	70	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*3
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*4
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	5	—	ns	
$\overline{CE}1$ Write Pulse Width	t_{CW}	45	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*3
$\overline{LB}$, $\overline{UB}$ Write Pulse Width	t_{BW}	45	—	ns	*3
$\overline{CE}1$ Write Recovery Time	t_{WRC}	15	—	ns	*5
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	ns	*5
$\overline{LB}$, $\overline{UB}$ Write Recovery Time	t_{BR}	15	1000	ns	*5
Data Setup Time	t_{DS}	15	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time for Write	t_{OHCL}	–5	—	ns	*6
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*7
$\overline{LB}$, $\overline{UB}$ Write Pulse Overlap	t_{BWO}	30	—	ns	
$\overline{CE}1$ High Pulse Width	t_{CP}	15	—	ns	

Notes *1: Maximum value is applicable if $\overline{CE}1$ is kept at Low without any address change. If the relaxation is needed by system operation, please contact local FUJITSU representative for the relaxation of 1 µs limitation.

*2: Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WRC}, t_{WR} or t_{BR}).

*3: Write pulse is defined from High to Low transition of $\overline{CE}1$, $\overline{WE}$ or $\overline{LB}$ / $\overline{UB}$, whichever occurs last.

*4: t_{VPL} is specified from the negative edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.

*5: Write recovery is defined from Low to High transition of $\overline{CE}1$, $\overline{WE}$ or $\overline{LB}$ / $\overline{UB}$, whichever occurs first.

*6: If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High within 5ns after $\overline{CE}1$ is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

*7: If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met and data bus is in High-Z.

■ AC CHARACTERISTICS (Continued)

SYNCHRONOUS OPERATION - CLOCK INPUT (BURST MODE)

Parameter		Symbol	Value		Unit	Notes
			Min.	Max.		
Clock Period	RL=5	t_{CK}	13	—	ns	*1
	RL=4		18	—	ns	*1
	RL=3		30	—	ns	*1
Clock High Time		t_{CKH}	4	—	ns	
Clock Low Time		t_{CKL}	4	—	ns	
Clock Rise/Fall Time		t_{CKT}	—	3	ns	*2

Notes *1: Clock period is defined between valid clock edges.
*2: Clock rise/fall time is defined between V_{IH} Min. and V_{IL} Max.

SYNCHRONOUS OPERATION - ADDRESS LATCH (BURST MODE)

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Address Setup Time to $\overline{ADV}$ Low	t_{ASVL}	–5	—	ns	*1
Address Setup Time to $\overline{CE}1$ Low	t_{ASCL}	–5	—	ns	*1
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	5	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*2
$\overline{ADV}$ Low Setup Time to CLK	t_{VSCK}	5	—	ns	*3
$\overline{ADV}$ Low Setup Time to $\overline{CE}1$ Low	t_{VLCL}	5	—	ns	*1
$\overline{CE}1$ Low Setup Time to CLK	t_{CLCK}	5	—	ns	*3
$\overline{ADV}$ Low Hold Time from CLK	t_{CKVH}	1	—	ns	*3
Burst End ADV High Hold Time from CLK	t_{VHVL}	13	—	ns	

Notes *1: t_{ASCL} is applicable if $\overline{CE}1$ brought to Low after $\overline{ADV}$ is brought to Low under the condition where t_{VLCL} is satisfied. The both of t_{ASCL} and t_{ASVL} must be satisfied if t_{VLCL} is not satisfied.
*2: t_{VPL} is specified from the negative edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.
*3: Applicable to the 1st valid clock edge.

■ AC CHARACTERISTICS (Continued)

SYNCHRONOUS READ OPERATION (BURST MODE)

Parameter		Symbol	Value		Unit	Notes
			Min.	Max.		
Burst Read Cycle Time		t_{RCB}	—	8000	ns	
CLK Access Time		t_{AC}	—	11	ns	*1
Output Hold Time from CLK		t_{CKQX}	3	—	ns	*1
$\overline{CE}1$ Low to $\overline{WAIT}$ Low		t_{CLTL}	5	20	ns	*1
$\overline{OE}$ Low to $\overline{WAIT}$ Low		t_{OLTL}	0	20	ns	*1
$\overline{ADV}$ Low to $\overline{WAIT}$ Low		t_{VLTL}	0	20	ns	*1
CLK to $\overline{WAIT}$ Valid Time		t_{CKTV}	—	11	ns	*1
$\overline{WAIT}$ Valid Hold Time from CLK		t_{CKTX}	3	—	ns	*1
$\overline{CE}1$ Low to Output Low-Z		t_{CLZ}	5	—	ns	*2
$\overline{OE}$ Low to Output Low-Z		t_{OLZ}	0	—	ns	*2
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z		t_{BLZ}	0	—	ns	*2
$\overline{CE}1$ High to Output High-Z		t_{CHZ}	—	20	ns	*1
$\overline{OE}$ High to Output High-Z		t_{OHZ}	—	20	ns	*1
$\overline{LB}$, $\overline{UB}$ High to Output High-Z		t_{BHZ}	—	20	ns	*1
$\overline{CE}1$ High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*1
$\overline{OE}$ High to $\overline{WAIT}$ High-Z		t_{OHTZ}	—	20	ns	*1
$\overline{OE}$ Low Setup Time to 1st Data-out		t_{OLQ}	30	—	ns	
$\overline{UB}$, $\overline{LB}$ Setup Time to 1st Data-out		t_{BLQ}	26	—	ns	*3
$\overline{OE}$ Setup Time to CLK		t_{OSCK}	5	—	ns	
$\overline{OE}$ Hold Time from CLK		t_{CKOH}	5	—	ns	
Burst End $\overline{CE}1$ Low Hold Time from CLK		t_{CKCLH}	5	—	ns	
Burst End $\overline{UB}$, $\overline{LB}$ Hold Time from CLK		t_{CKBH}	5	—	ns	
Burst Terminate Recovery Time	BL=8,16	t_{TRB}	26	—	ns	*4
	BL=Continuous		70	—	ns	*4

Notes *1: The output load 50pF with 50ohm termination to V_{DDQ}*0.5 V.
*2: The output load 5pF without any other load.
*3: Once they are determined, they must not be changed until the end of burst.
*4: Defined from the Low to High transition of $\overline{CE}1$ to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}1$ whichever occurs late.

■ AC CHARACTERISTICS (Continued)

SYNCHRONOUS WRITE OPERATION (BURST MODE)

Parameter		Symbol	Value		Unit	Notes
			Min.	Max.		
Burst Write Cycle Time		t_{WCB}	—	8000	ns	
Data Setup Time to Clock		t_{DSCK}	5	—	ns	
Data Hold Time from CLK		t_{DHCK}	3	—	ns	
$\overline{WE}$ Low Setup Time to 1st Data In		t_{WLD}	30	—	ns	
$\overline{UB}$, $\overline{LB}$ Setup Time for Write		t_{BS}	–5	—	ns	*1
$\overline{WE}$ Setup Time to CLK		t_{WSCK}	5	—	ns	
$\overline{WE}$ Hold Time from CLK		t_{CKWH}	5	—	ns	
$\overline{CE}$1 Low to $\overline{WAIT}$ High		t_{CLTH}	5	20	ns	*2
$\overline{WE}$ Low to $\overline{WAIT}$ High		t_{WLTH}	0	20	ns	*2
$\overline{CE}$1 High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*2
$\overline{WE}$ High to $\overline{WAIT}$ High-Z		t_{WHTZ}	—	20	ns	*2
Burst End $\overline{CE}$1 Low Hold Time from CLK		t_{CKCLH}	5	—	ns	
Burst End $\overline{CE}$1 High Setup Time to next CLK		t_{CHCK}	5	—	ns	
Burst End $\overline{UB}$, $\overline{LB}$ Hold Time from CLK		t_{CKBH}	5	—	ns	
Burst Write Recovery Time		t_{WRB}	26		ns	*3
Burst Terminate Recovery Time	BL=8,16	t_{TRB}	26	—	ns	*4
	BL=Continuous	t_{TRB}	70	—	ns	*4

Notes *1: Defined from the valid input edge to the High to Low transition of either $\overline{ADV}$, $\overline{CE}$1, or $\overline{WE}$, whichever occurs last. And once they are determined, they must not be changed until the end of burst.

*2: The output load 50pF with 50ohm termination to V_{DDQ}*0.5 V.

*3: Defined from the valid clock edge where last data-in being latched at the end of burst write to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}$1 whichever occurs late for the next access.

*4: Defined from the Low to High transition of $\overline{CE}$1 to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}$1 whichever occurs late for the next access.

■ AC CHARACTERISTICS (Continued)

POWER DOWN PARAMETERS

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	20	—	ns	*1
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	70	—	ns	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	µs	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [not in SLEEP mode]	t_{CHHP}	1	—	µs	*2
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	*1

Notes *1: Applicable also to power-up.
*2: Applicable when Partial mode is set.

OTHER TIMING PARAMETERS

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
CE2 High Hold Time after Power-up	t_{C2HL}	50	—	µs	
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time (except for CLK)	t_T	1	25	ns	*2, *3

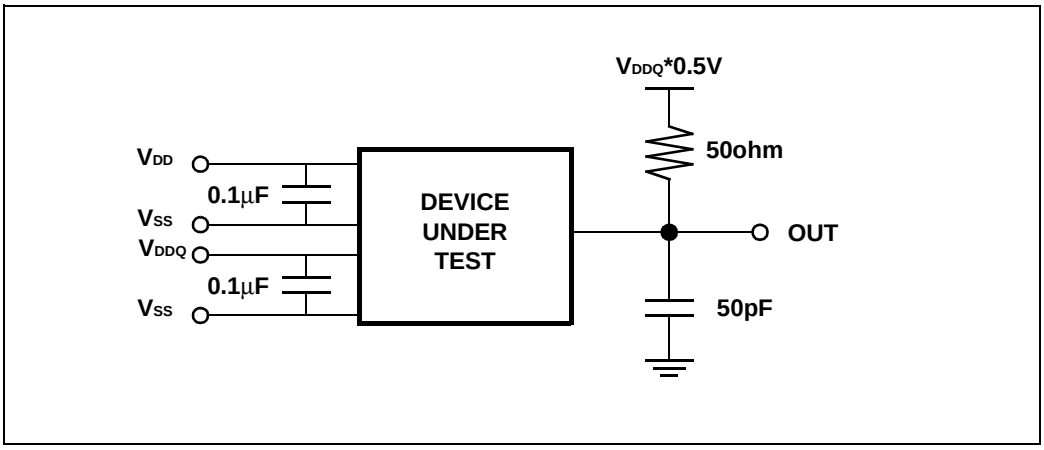
Notes *1: Some data might be written into any address location if t_{CHWX}(min) is not satisfied.
*2: Except for clock input transition time.
*3: The Input Transition Time (t_T) at AC testing is shown in below. If actual t_T is longer than specified values, it may violate AC specification of some timing parameters.

■ AC CHARACTERISTICS (Continued)

AC TEST CONDITIONS

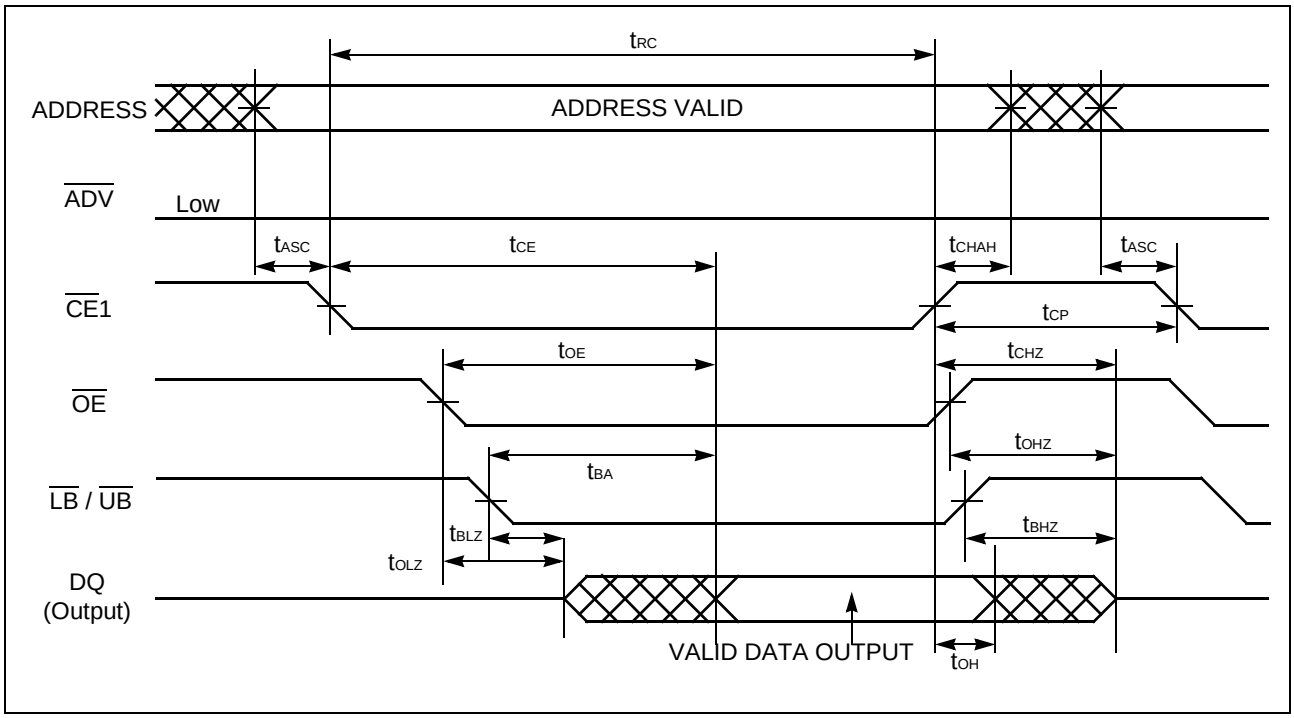
Symbol	Description		Test Setup	Value	Unit	Note
V_{IH}	Input High Level			V_{DDQ} * 0.8	V	
V_{IL}	Input Low Level			V_{DDQ} * 0.2	V	
V_{REF}	Input Timing Measurement Level			V_{DDQ} * 0.5	V	
t_T	Input Transition Time	Async.	Between V_{IL} and V_{IH}	5	ns	
		Sync.		3	ns	

AC MEASUREMENT OUTPUT LOAD CIRCUIT



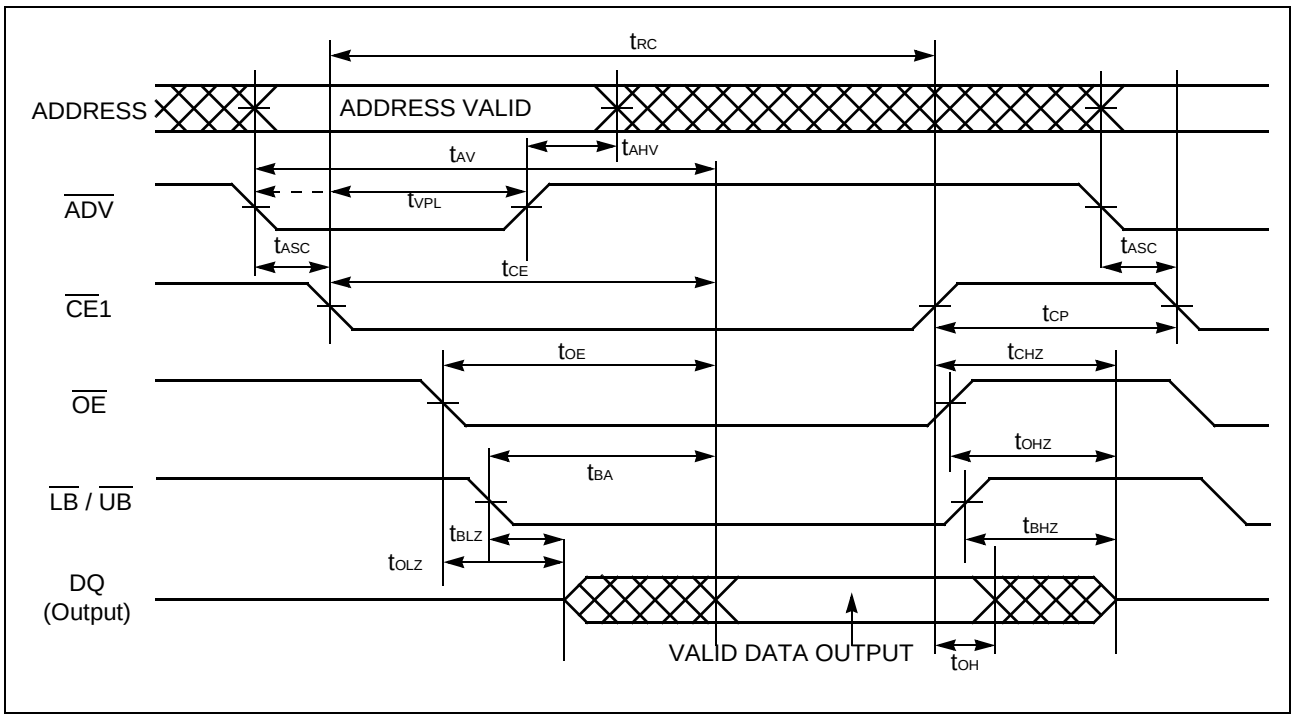
■ TIMING DIAGRAMS

Asynchronous Read Timing #1-1 (Basic Timing) See Note.



Note: This timing diagram assumes CE2=H and $\overline{WE}$=H.

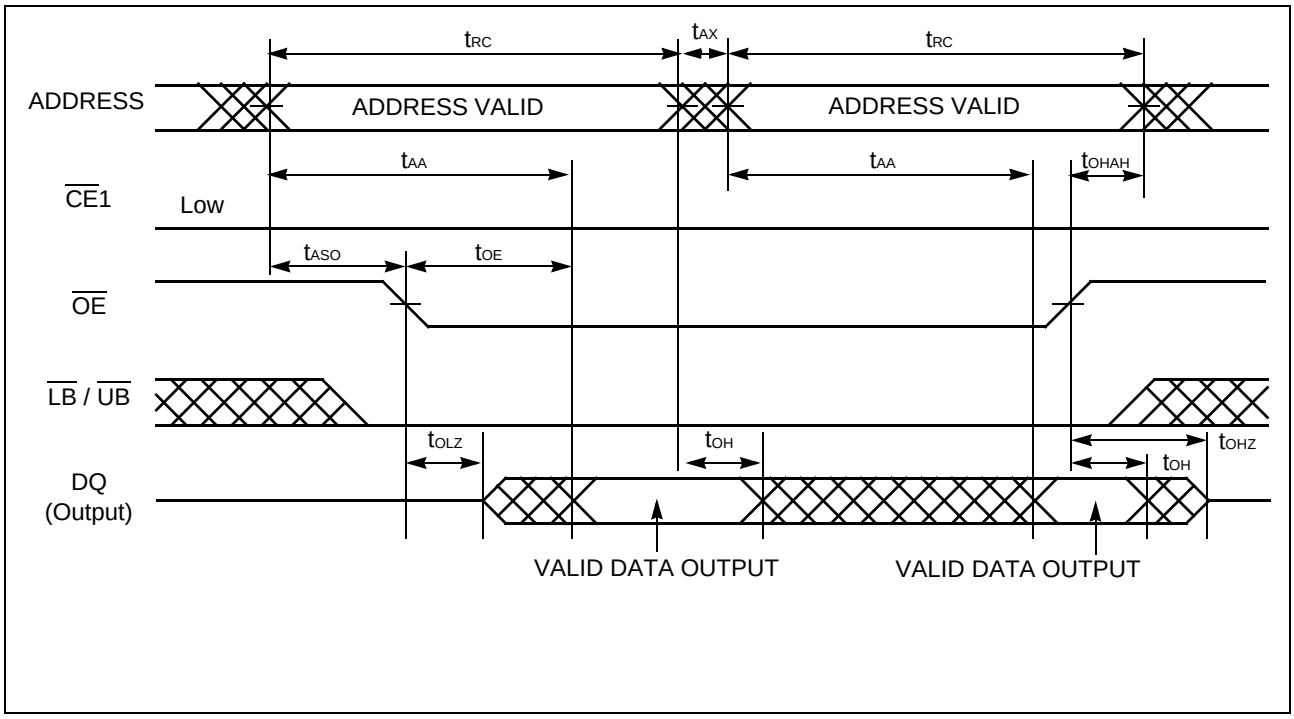
Asynchronous Read Timing #1-2 (Basic Timing) See Note.



Note: This timing diagram assumes CE2=H and $\overline{WE}$=H.

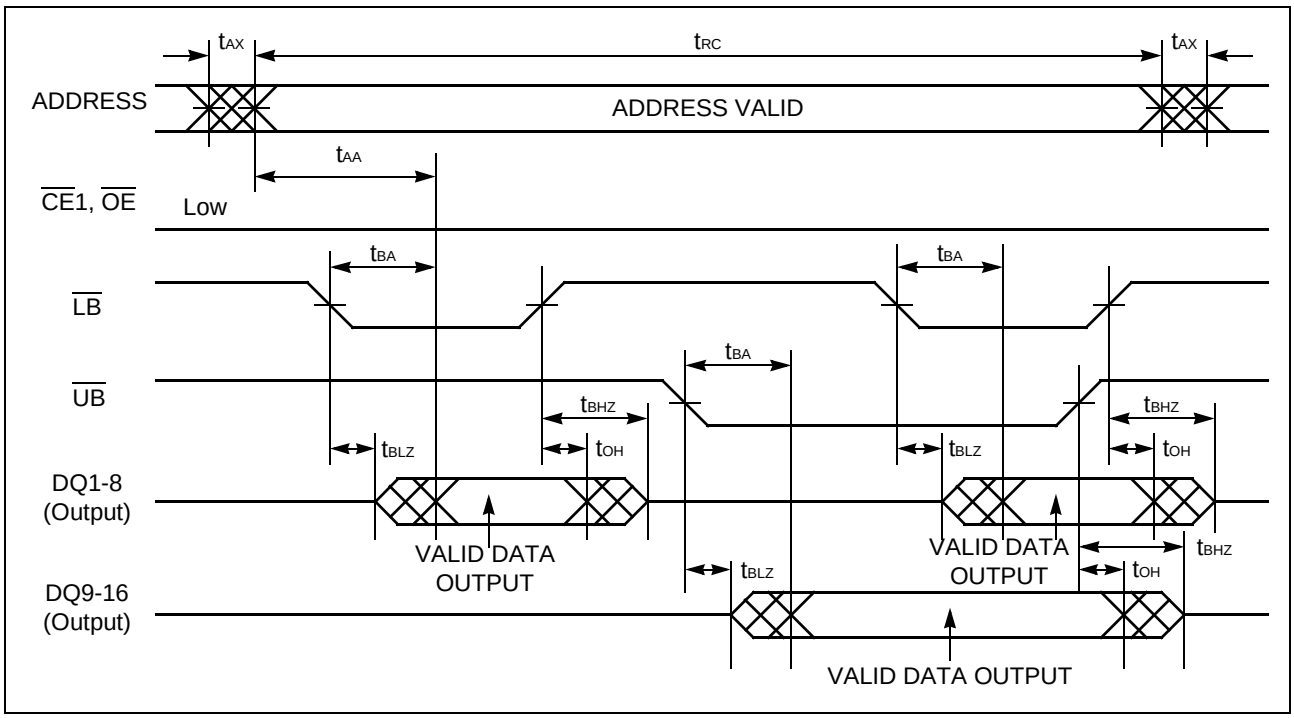
■ TIMING DIAGRAMS (Continued)

Asynchronous Read Timing #2 ($\overline{OE}$ & Address Access) See Note.



Notes: This timing diagram assumes CE2=H, $\overline{ADV}$=L and $\overline{WE}$=H.

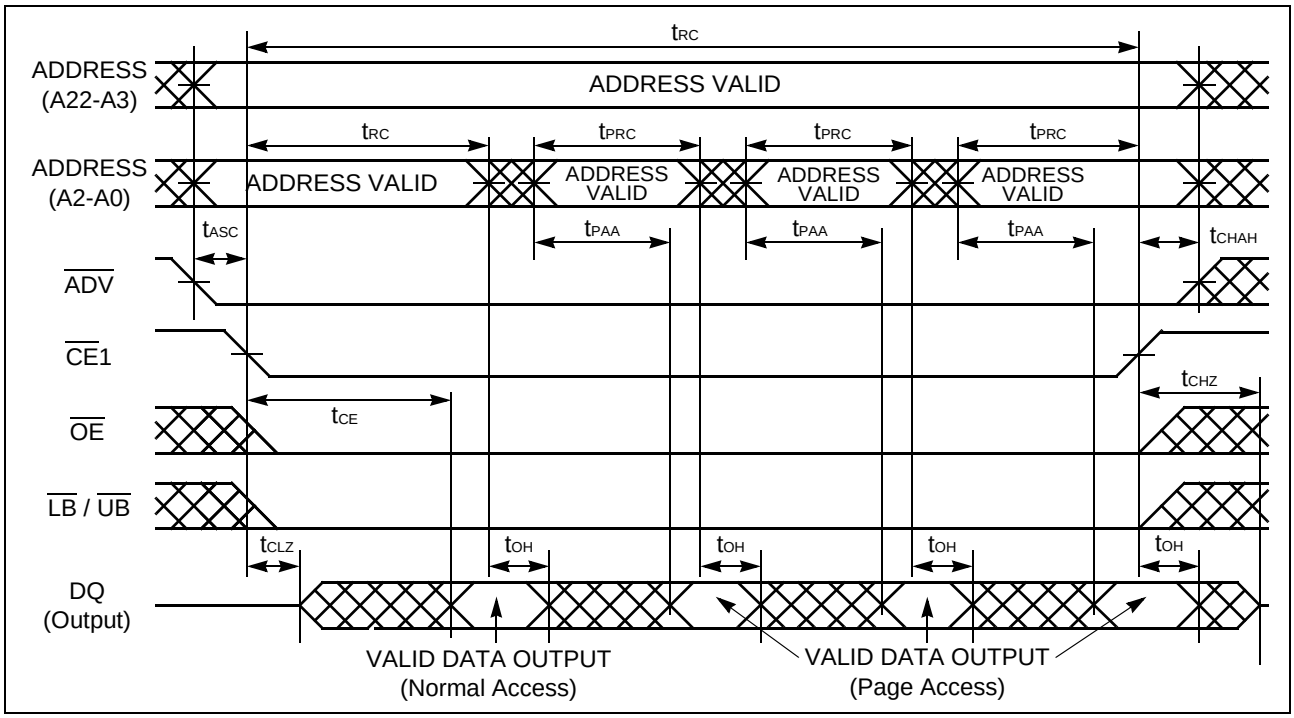
Asynchronous Read Timing #3 ($\overline{LB}$ / $\overline{UB}$ Byte Access) See Note.



Note: This timing diagram assumes CE2=H, $\overline{ADV}$=L and $\overline{WE}$=H.

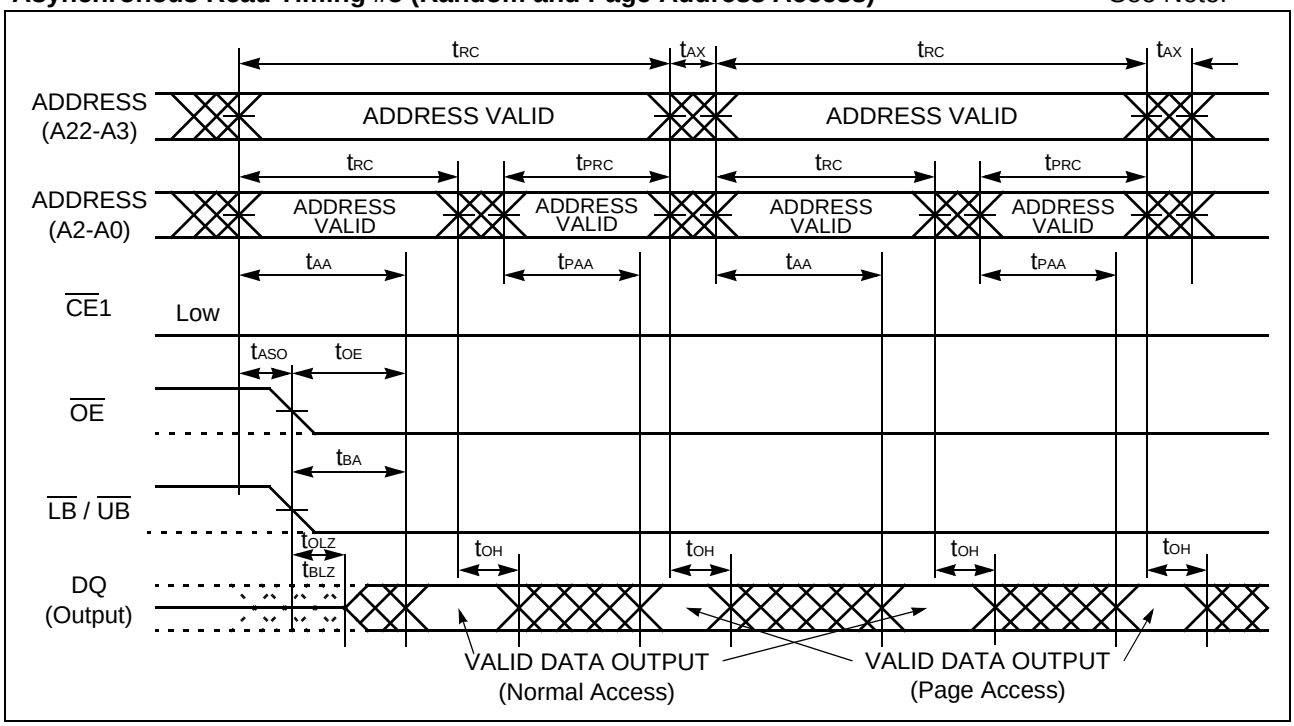
■ TIMING DIAGRAMS (Continued)

Asynchronous Read Timing #4 (Page Address Access after $\overline{CE1}$ Control Access) See Note.



Notes: This timing diagram assumes CE2=H and $\overline{WE}$=H.

Asynchronous Read Timing #5 (Random and Page Address Access) See Note.

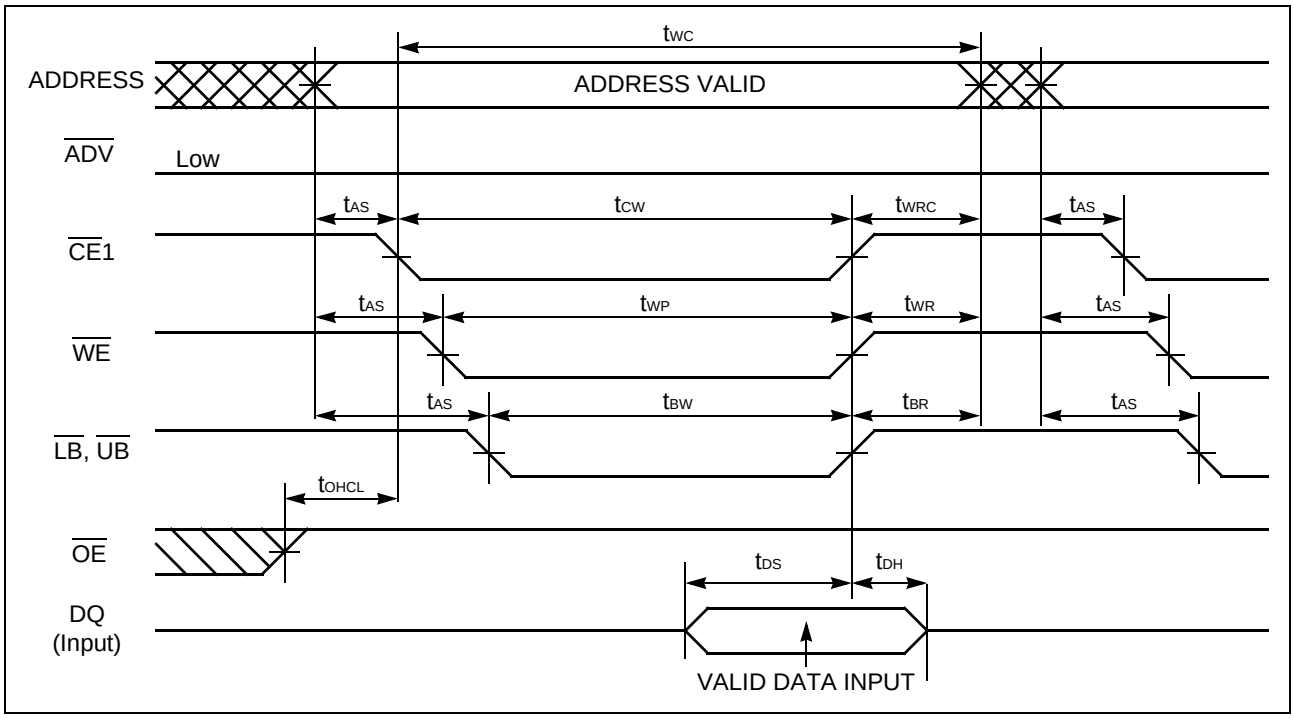


Notes *1: This timing diagram assumes CE2=H, $\overline{ADV}$=L and $\overline{WE}$=H.

*2: Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE1}$ and $\overline{OE}$ are Low.

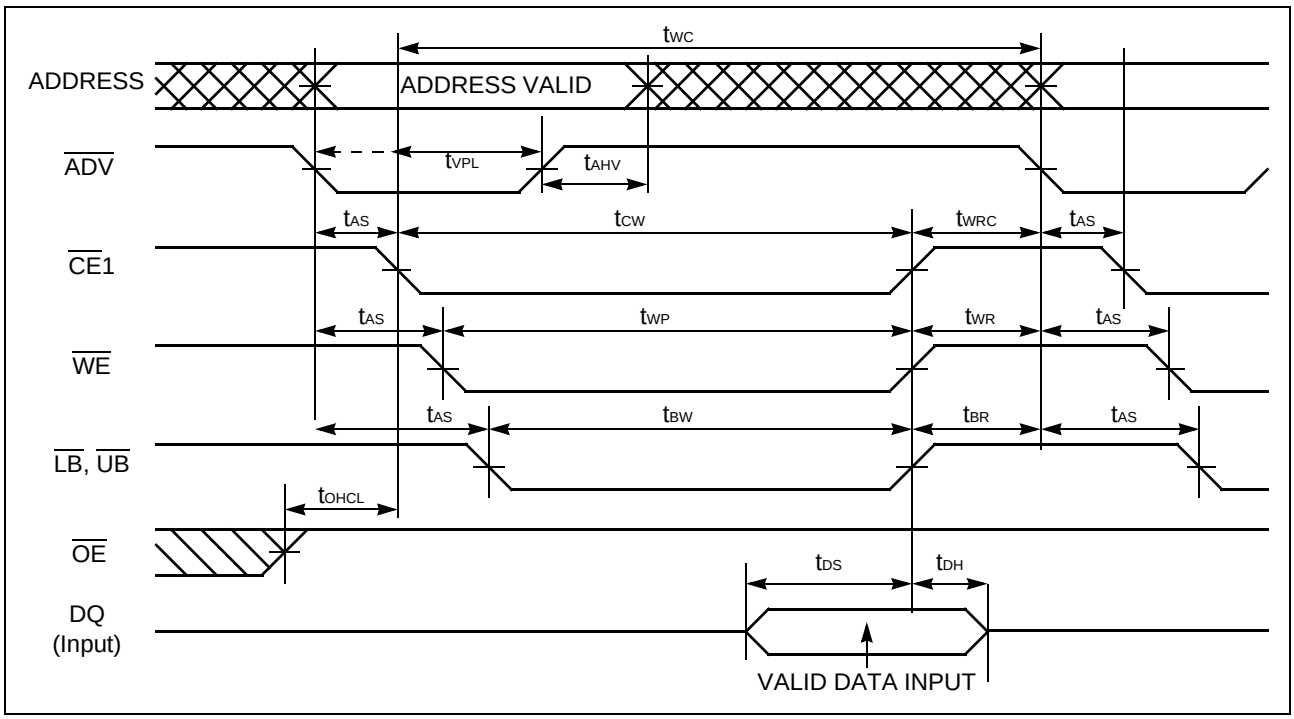
■ TIMING DIAGRAMS (Continued)

Asynchronous Write Timing #1-1 (Basic Timing) See Note.



Notes: This timing diagram assumes CE2=H and $\overline{ADV}$=L.

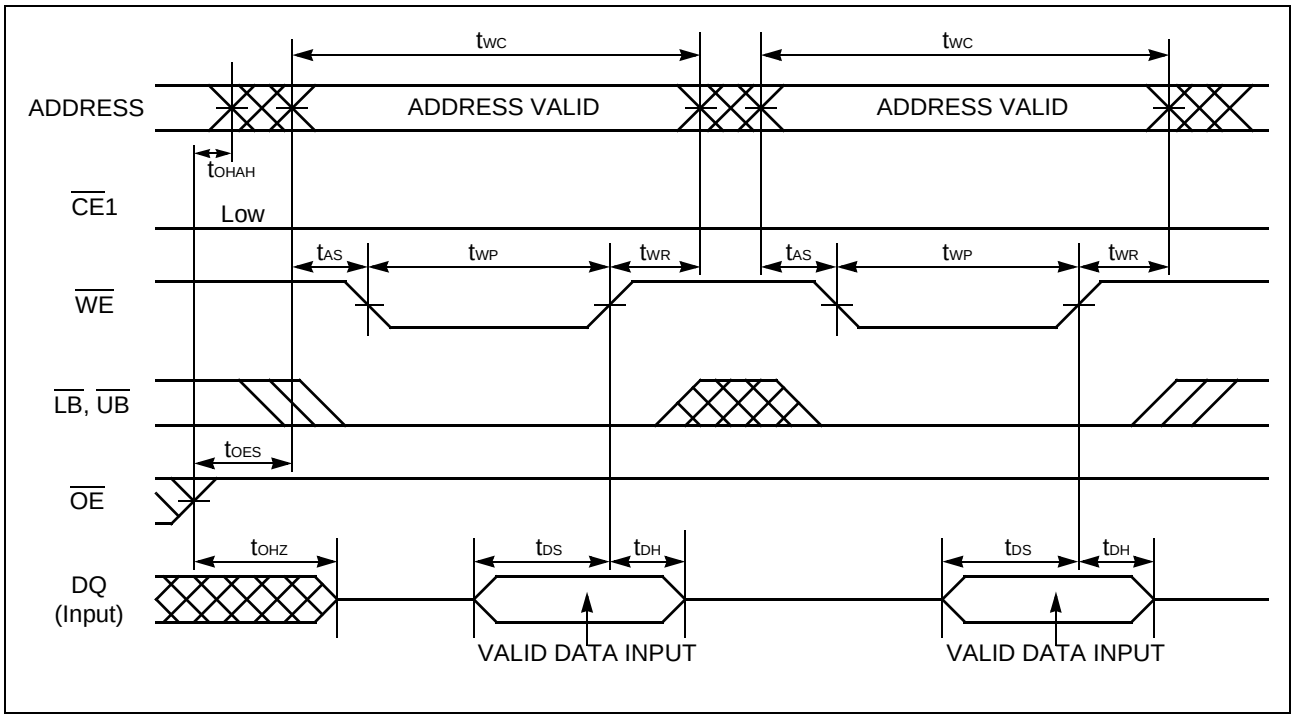
Asynchronous Write Timing #1-2 (Basic Timing) See Note.



Notes: This timing diagram assumes CE2=H.

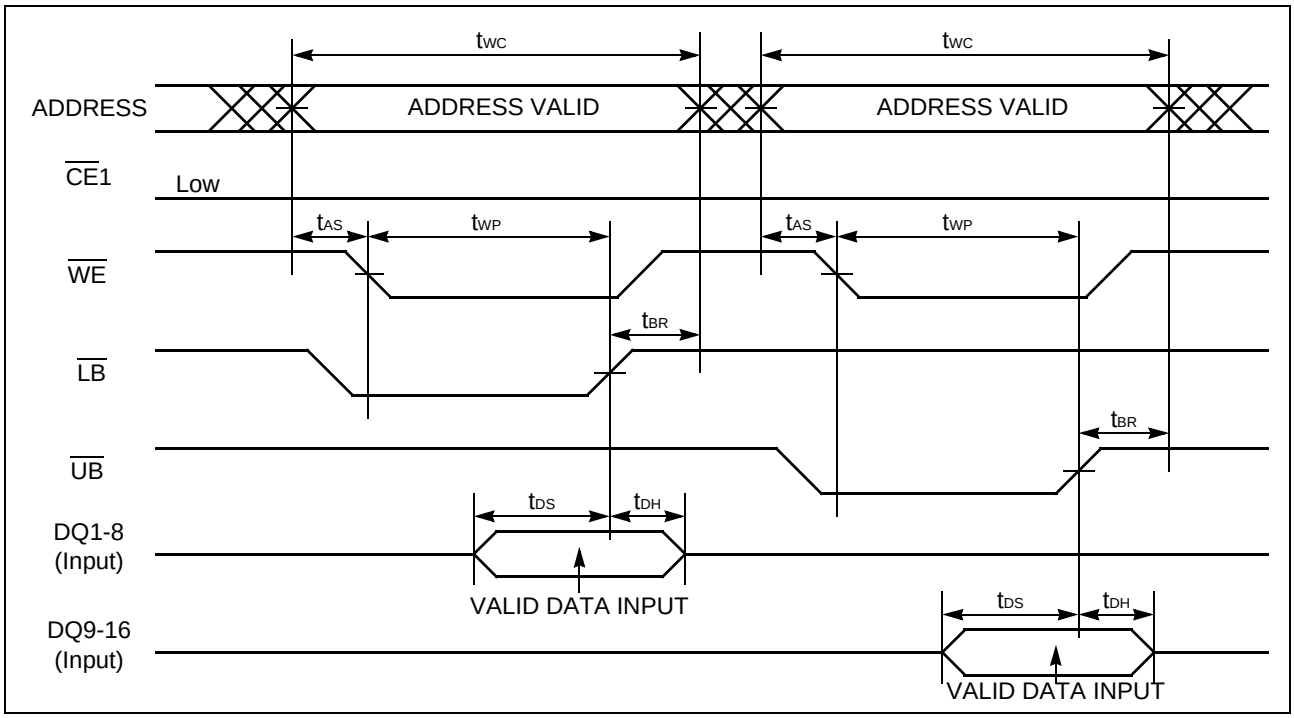
■ TIMING DIAGRAMS (Continued)

Asynchronous Write Timing #2 ($\overline{WE}$ Control) See Note.



Note: This timing diagram assumes CE2=H and $\overline{ADV}$=L.

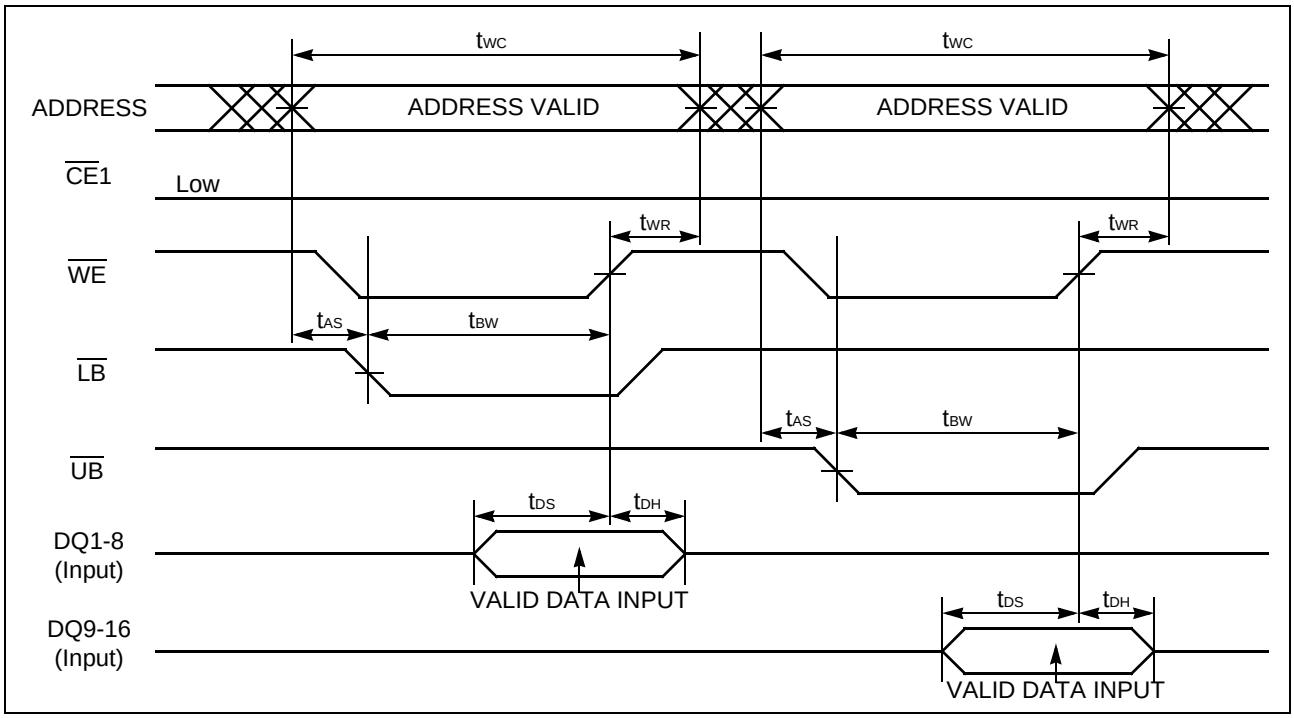
Asynchronous Write Timing #3-1 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) See Note.



Note: This timing diagram assumes CE2=H, $\overline{ADV}$=L and $\overline{OE}$=H.

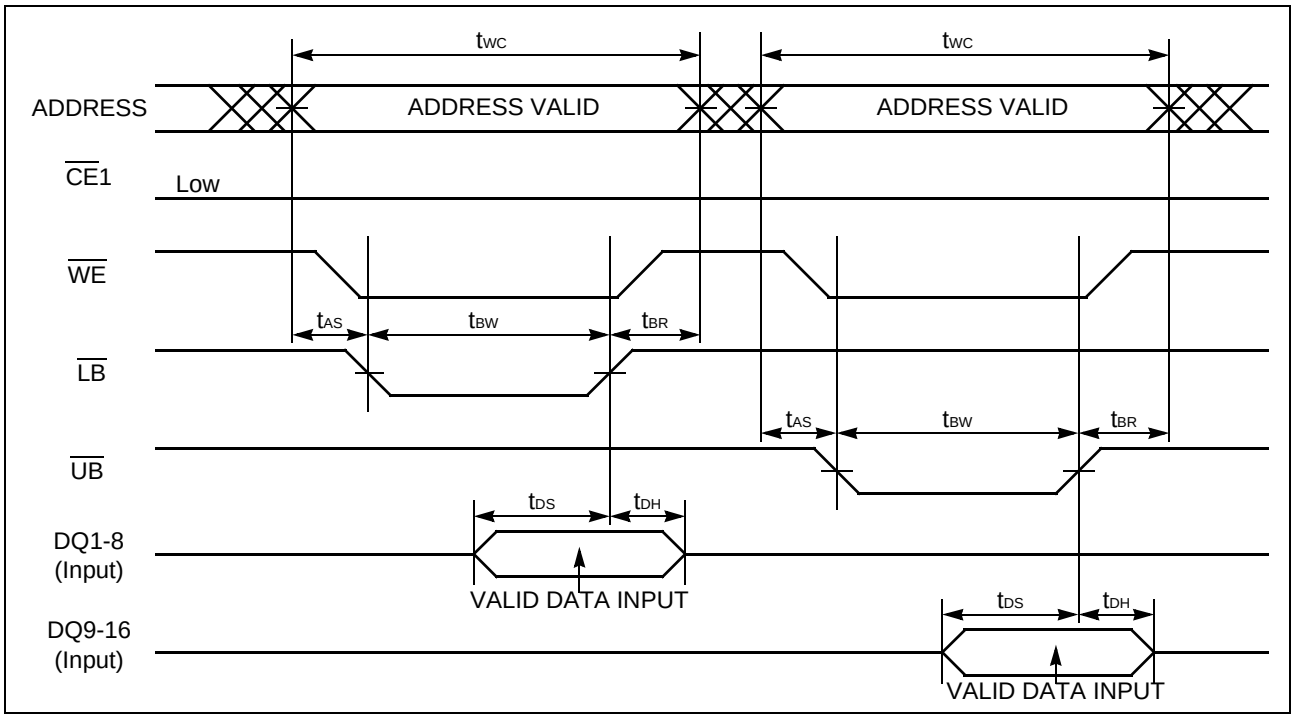
■ TIMING DIAGRAMS (Continued)

Asynchronous Write Timing #3-2 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) See Note.



Note: This timing diagram assumes CE2=H, $\overline{ADV}$=L and $\overline{OE}$=H.

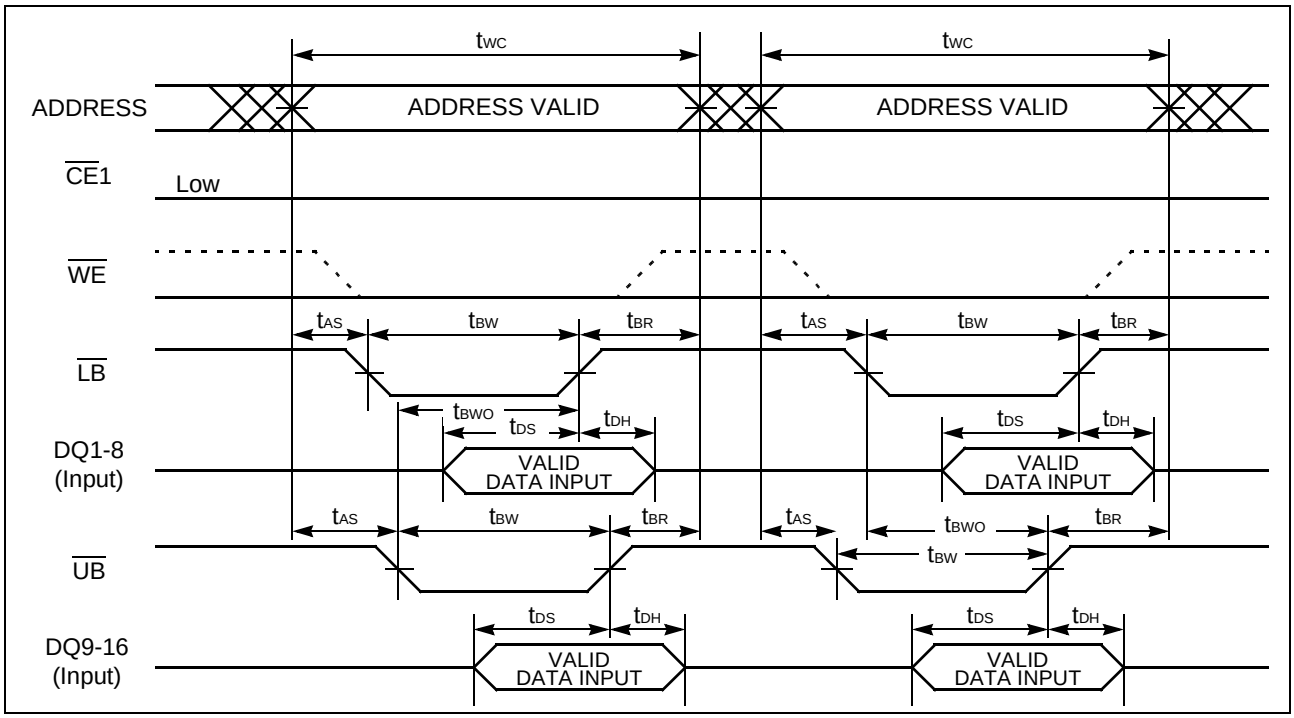
Asynchronous Write Timing #3-3 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) See Note.



Note: This timing diagram assumes CE2=H, $\overline{ADV}$=L and $\overline{OE}$=H.

■ TIMING DIAGRAMS (Continued)

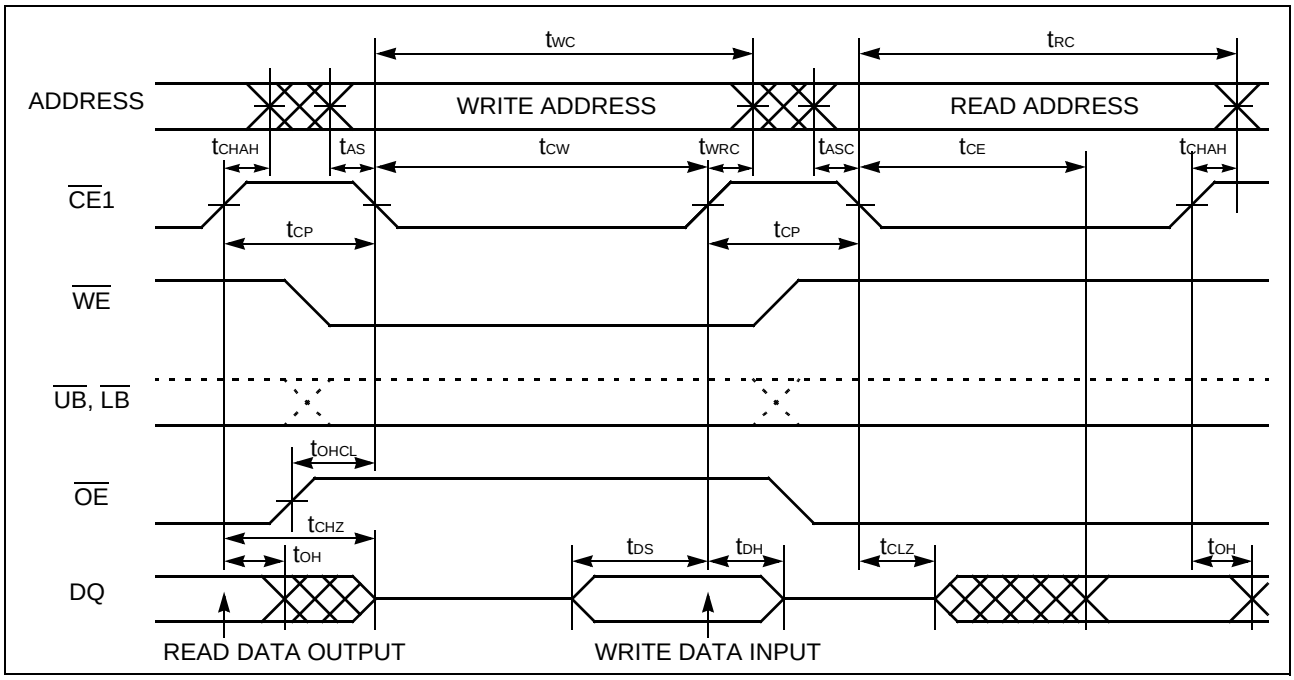
Asynchronous Write Timing #3-4 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) See Note.



Note: This timing diagram assumes CE2=H, $\overline{ADV}$=L and $\overline{OE}$=H.

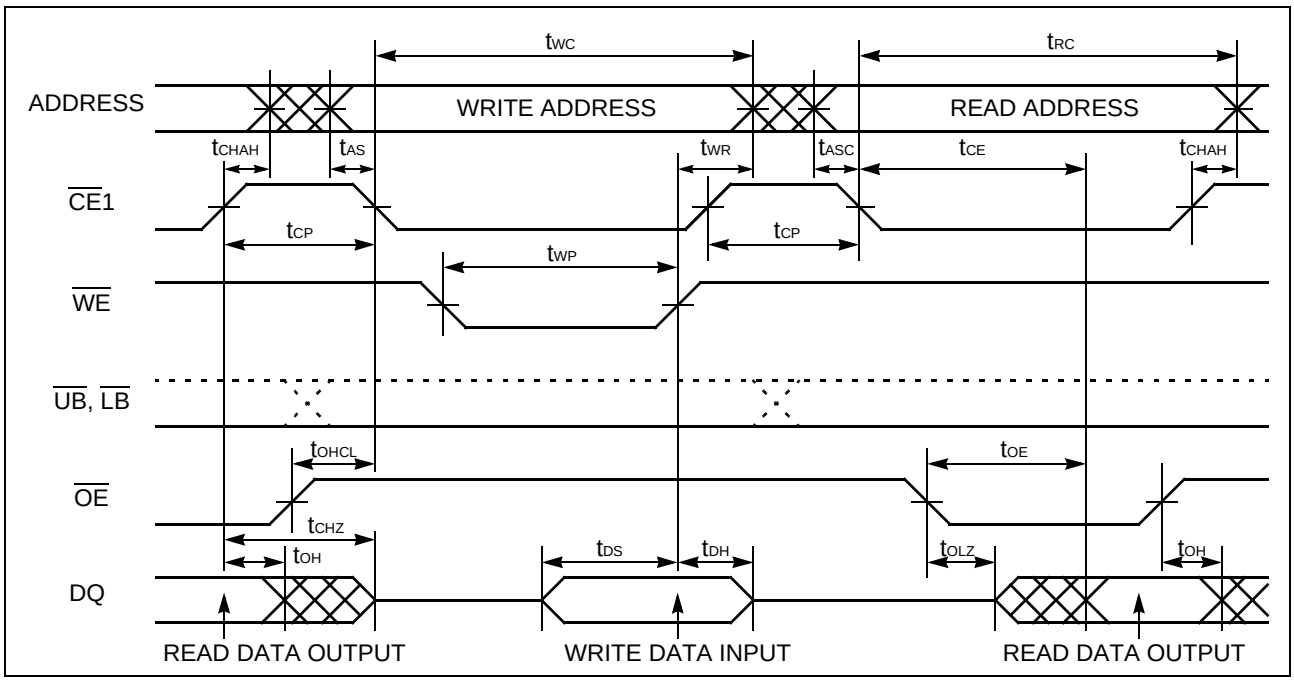
■ TIMING DIAGRAMS (Continued)

Asynchronous Read / Write Timing #1-1 ($\overline{CE1}$ Control) See Note.



Notes *1: This timing diagram assumes CE2=H and $\overline{ADV}$=L.
*2: Write address is valid from either $\overline{CE1}$ or $\overline{WE}$ of last falling edge.

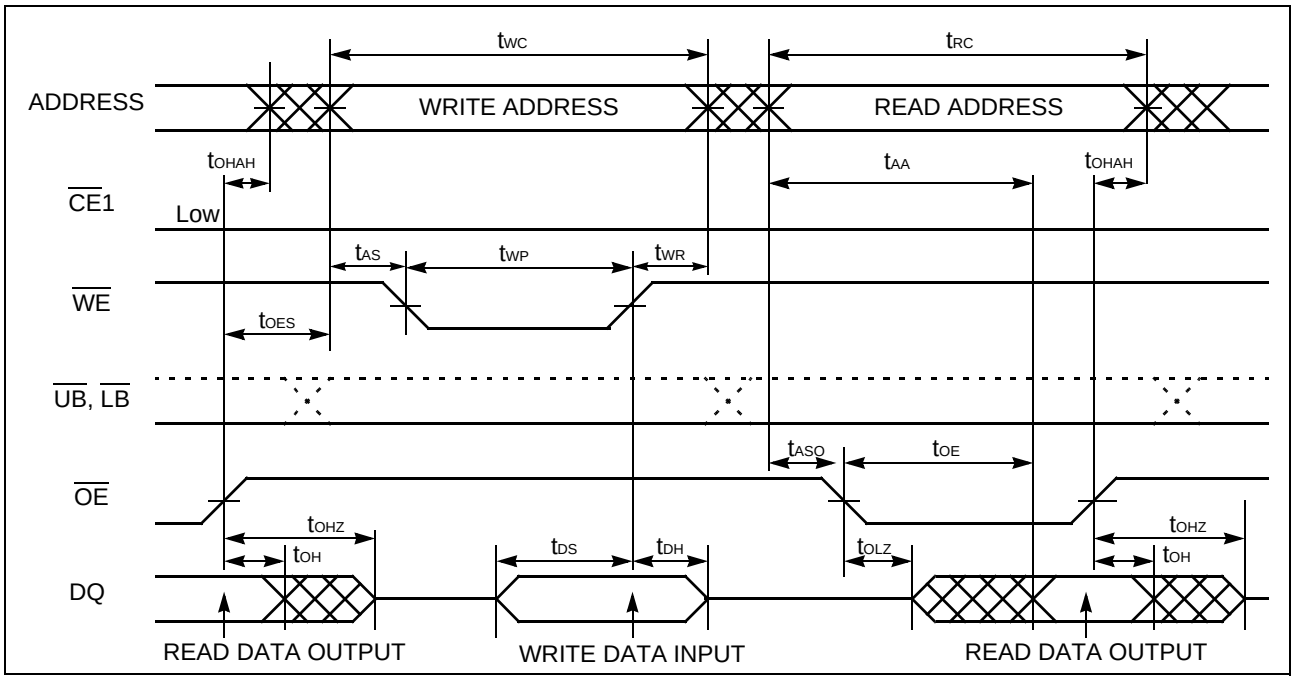
Asynchronous Read / Write Timing #1-2 ($\overline{CE1}$ / $\overline{WE}$ / $\overline{OE}$ Control) See Note.



Notes *1: This timing diagram assumes CE2=H and $\overline{ADV}$=L.
*2: $\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE1}$ controlled write at Read-Write-Read sequence.

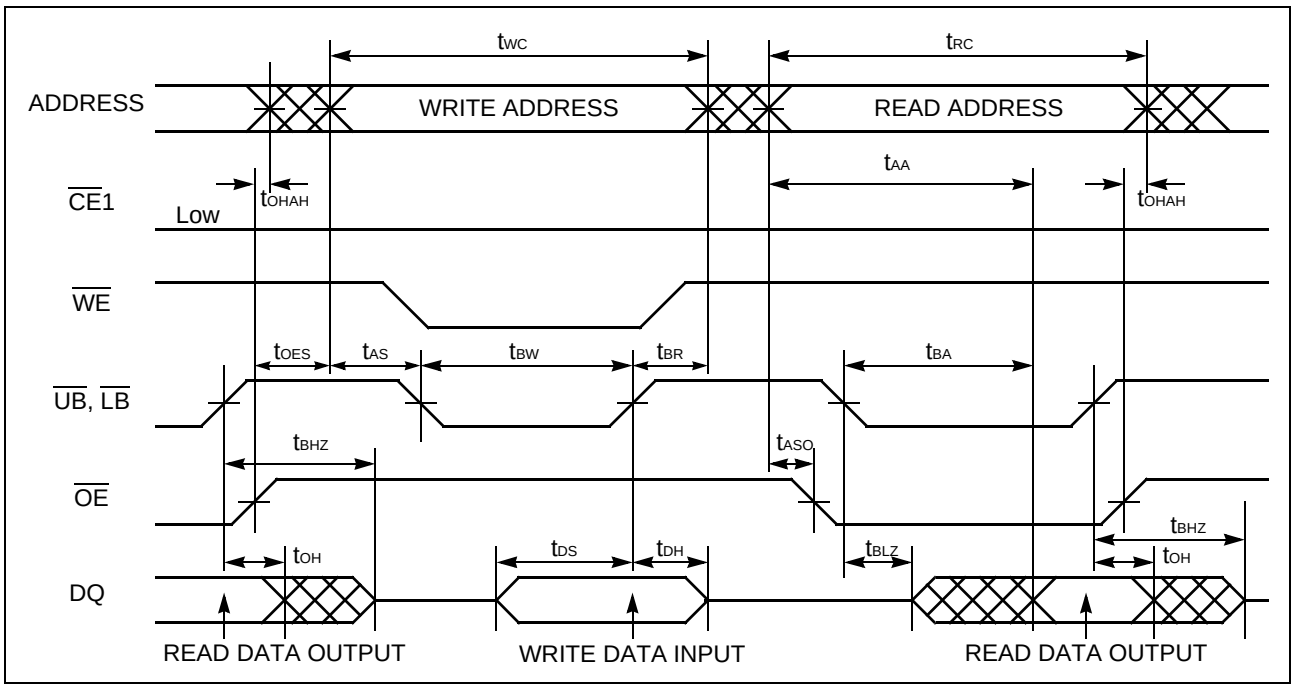
■ TIMING DIAGRAMS (Continued)

Asynchronous Read / Write Timing #2 ($\overline{OE}$, $\overline{WE}$ Control) See Note.



Notes *1: This timing diagram assumes CE2=H and $\overline{ADV}$=L.
*2: $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

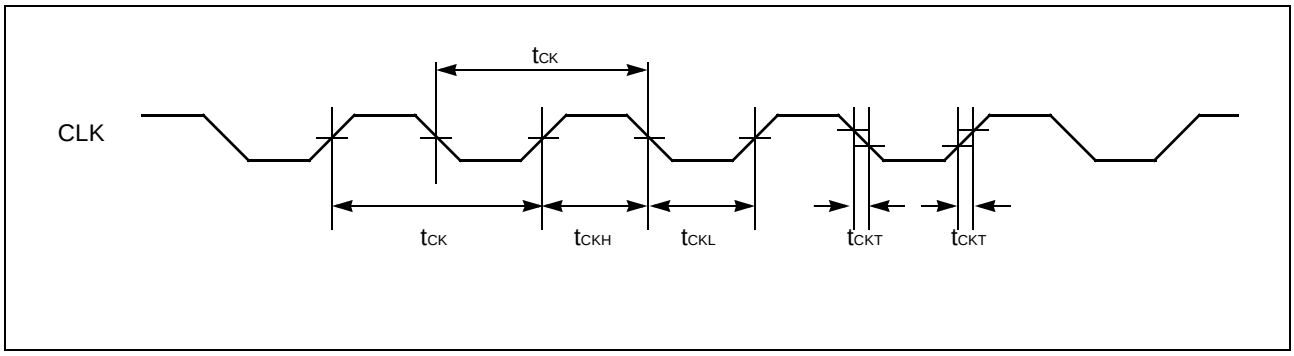
Asynchronous Read / Write Timing #3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control) See Note.



Notes *1: This timing diagram assumes CE2=H and $\overline{ADV}$=L.
*2: $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

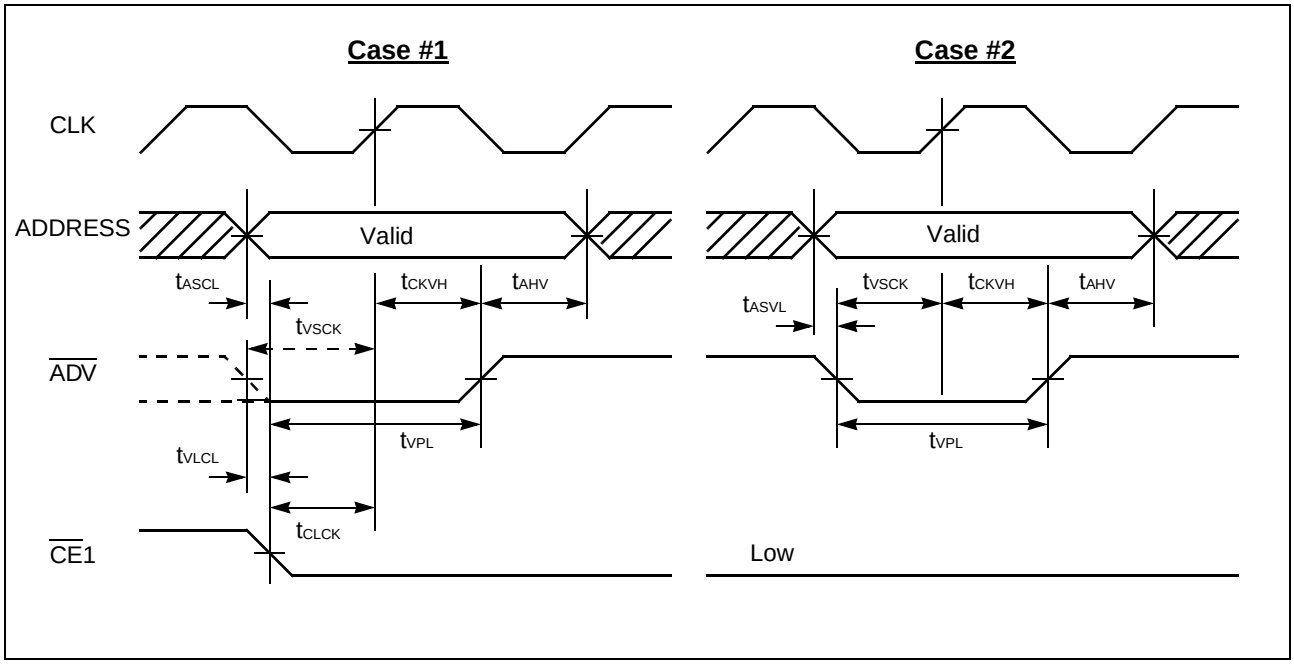
■ TIMING DIAGRAMS (Continued)

Clock Input Timing See Note.



Notes *1: Stable clock input must be required during $\overline{CE}1$=L.
*2: t_{CK} is defined between valid clock edges.
*3: t_{CKT} is defined between V_{IH} Min. and V_{IL} Max.

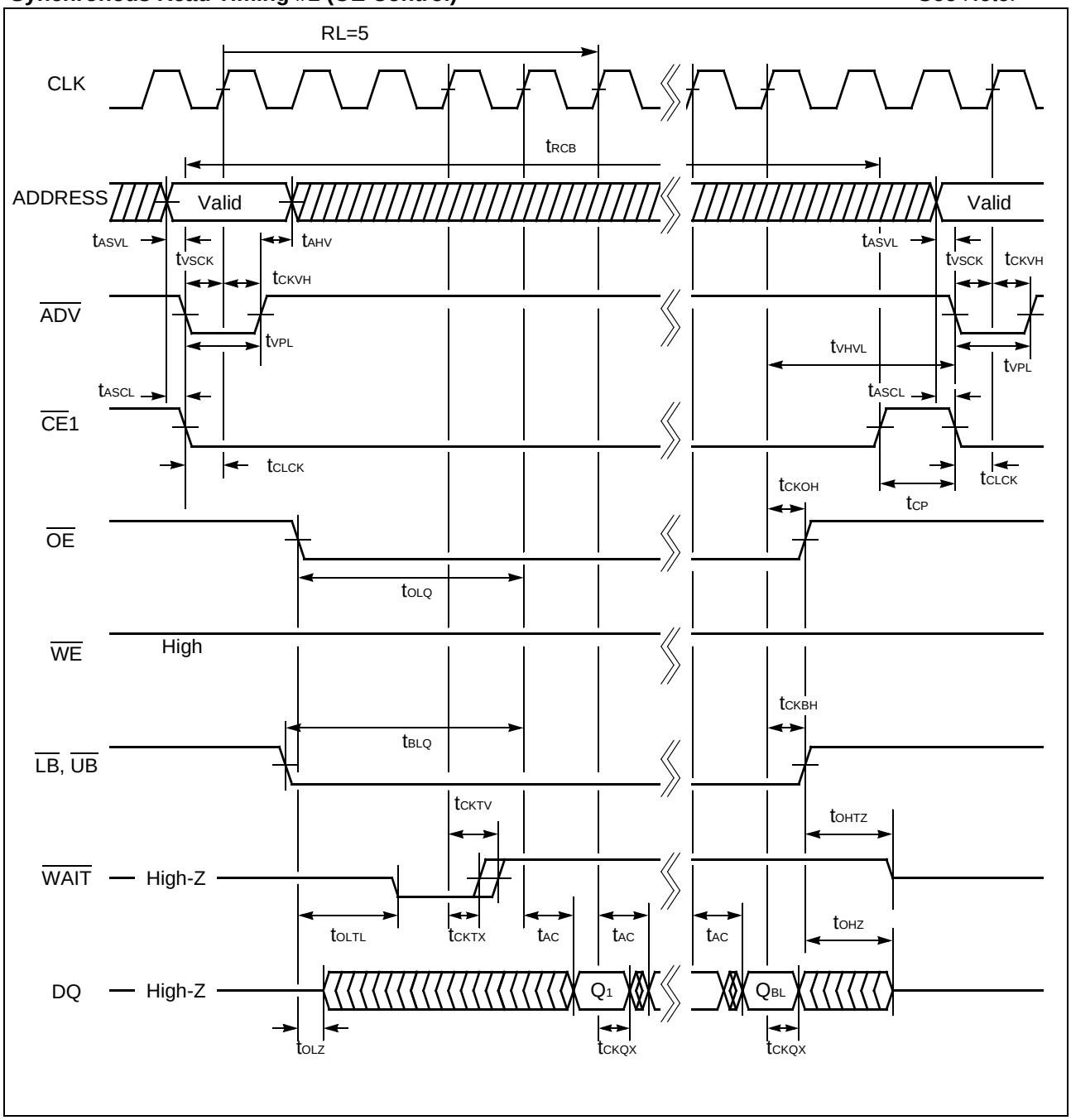
Address Latch Timing (Synchronous Mode) See Note.



Notes *1: Case #1 is the timing when $\overline{CE}1$ is brought to Low after $\overline{ADV}$ is brought to Low.
Case #2 is the timing when $\overline{ADV}$ is brought to Low after $\overline{CE}1$ is brought to Low.
*2: t_{VPL} is specified from the negative edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.
At least one valid clock edge must be input during $\overline{ADV}$=L.
*3: t_{VSCK} and t_{CLCK} are applied to the 1st valid clock edge during $\overline{ADV}$=L.

■ TIMING DIAGRAMS (Continued)

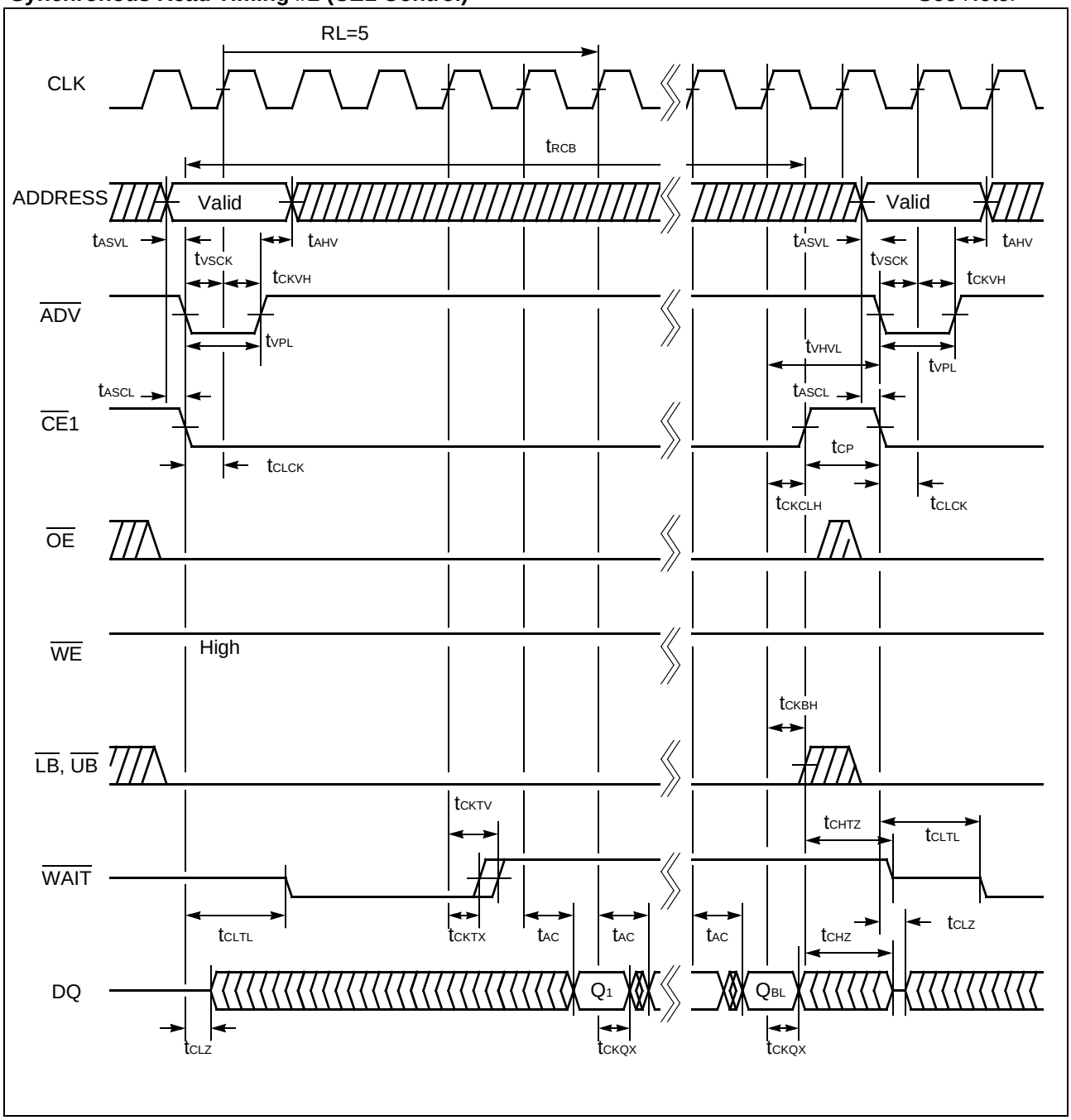
Synchronous Read Timing #1 ($\overline{OE}$ Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

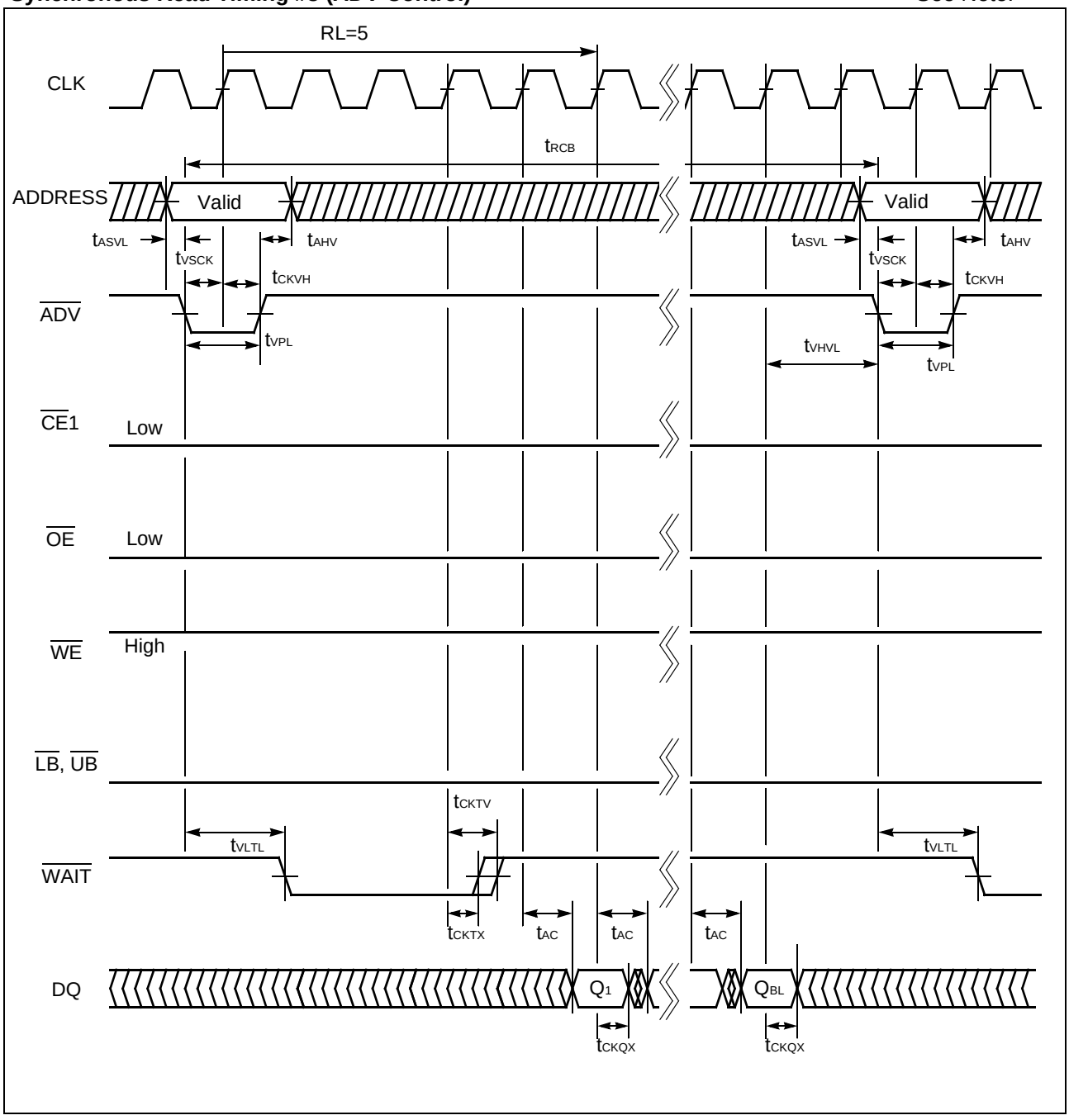
Synchronous Read Timing #2 ($\overline{CE1}$ Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

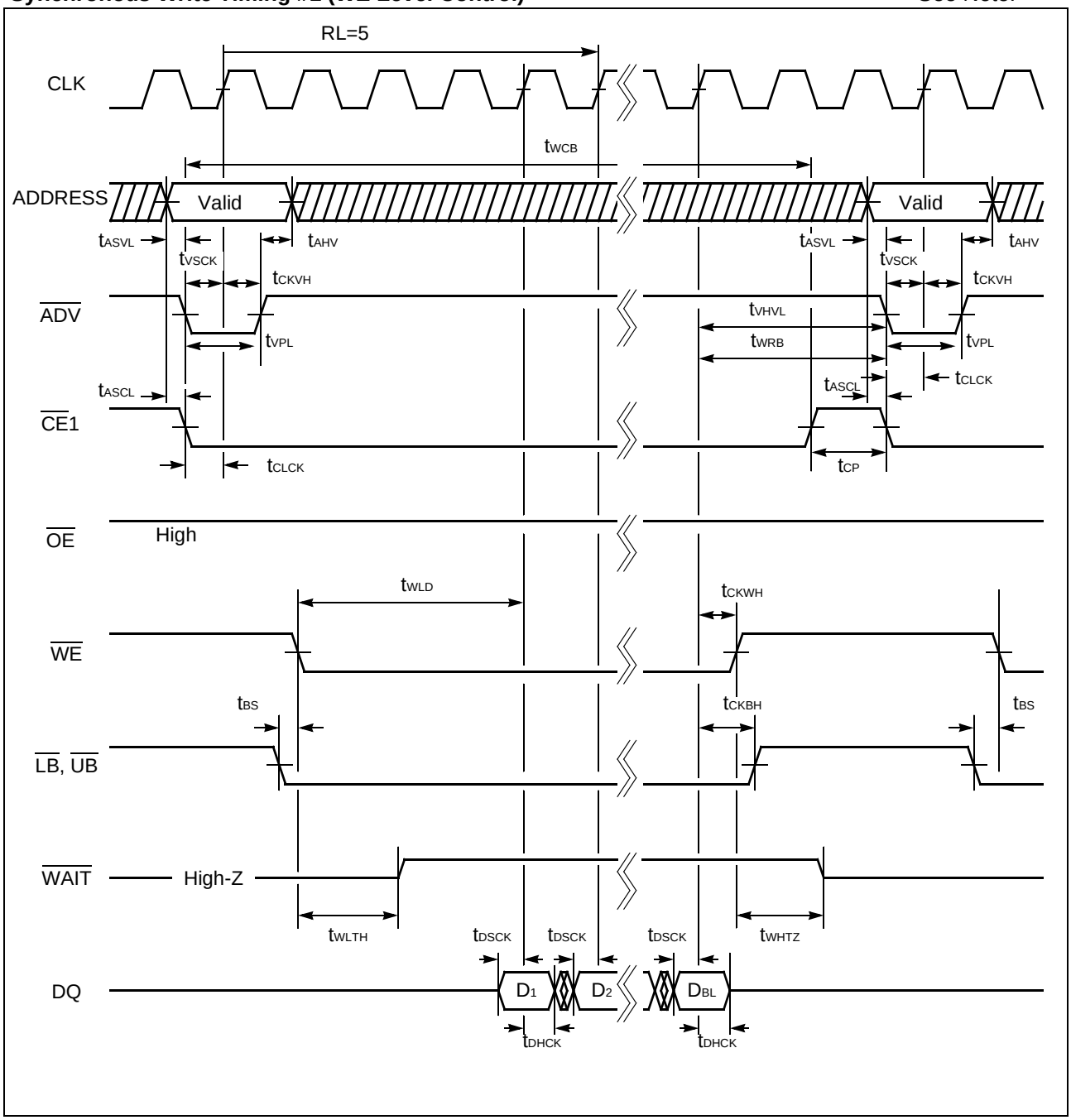
Synchronous Read Timing #3 ($\overline{\text{ADV}}$ Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

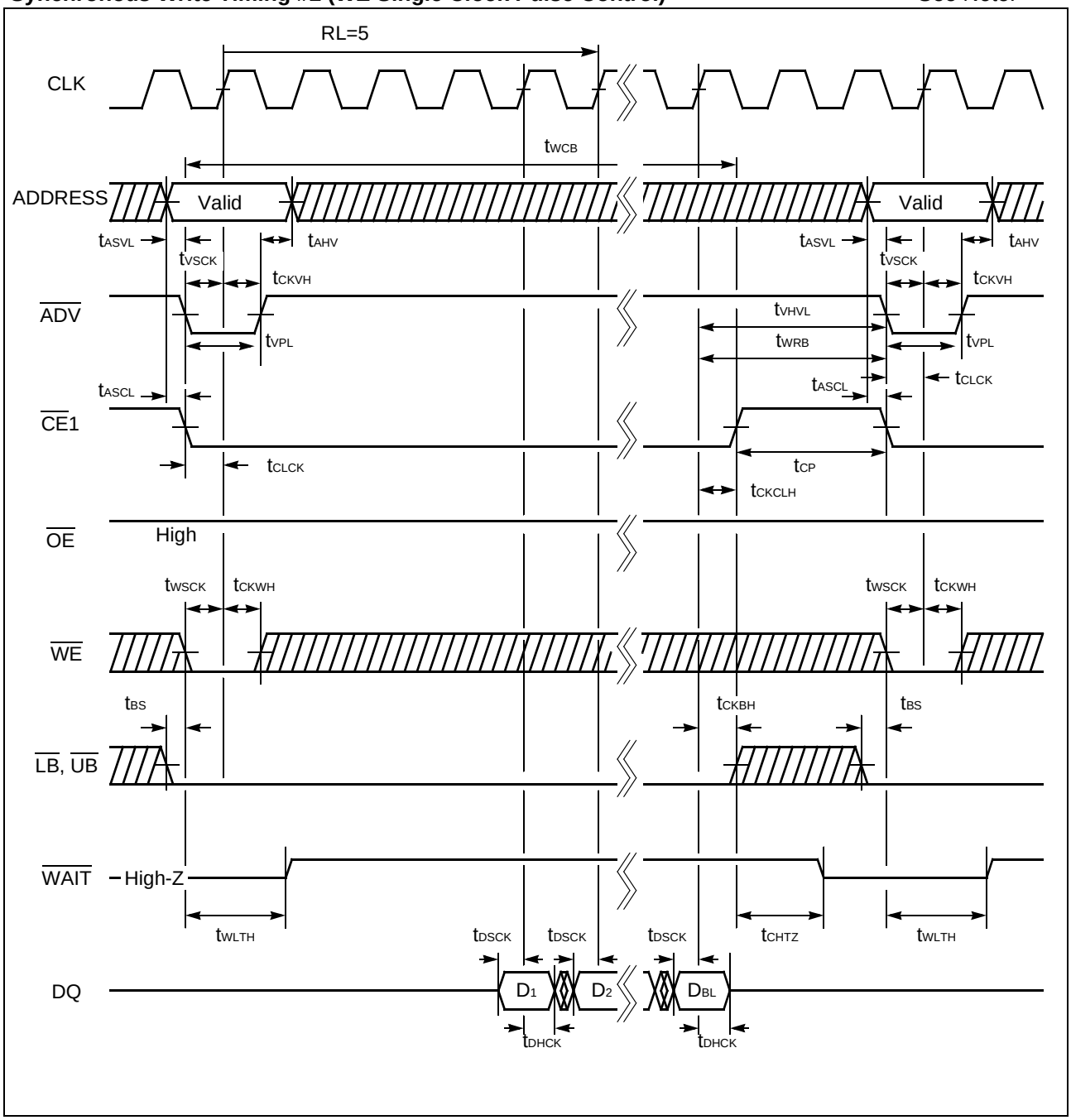
Synchronous Write Timing #1 ($\overline{WE}$ Level Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

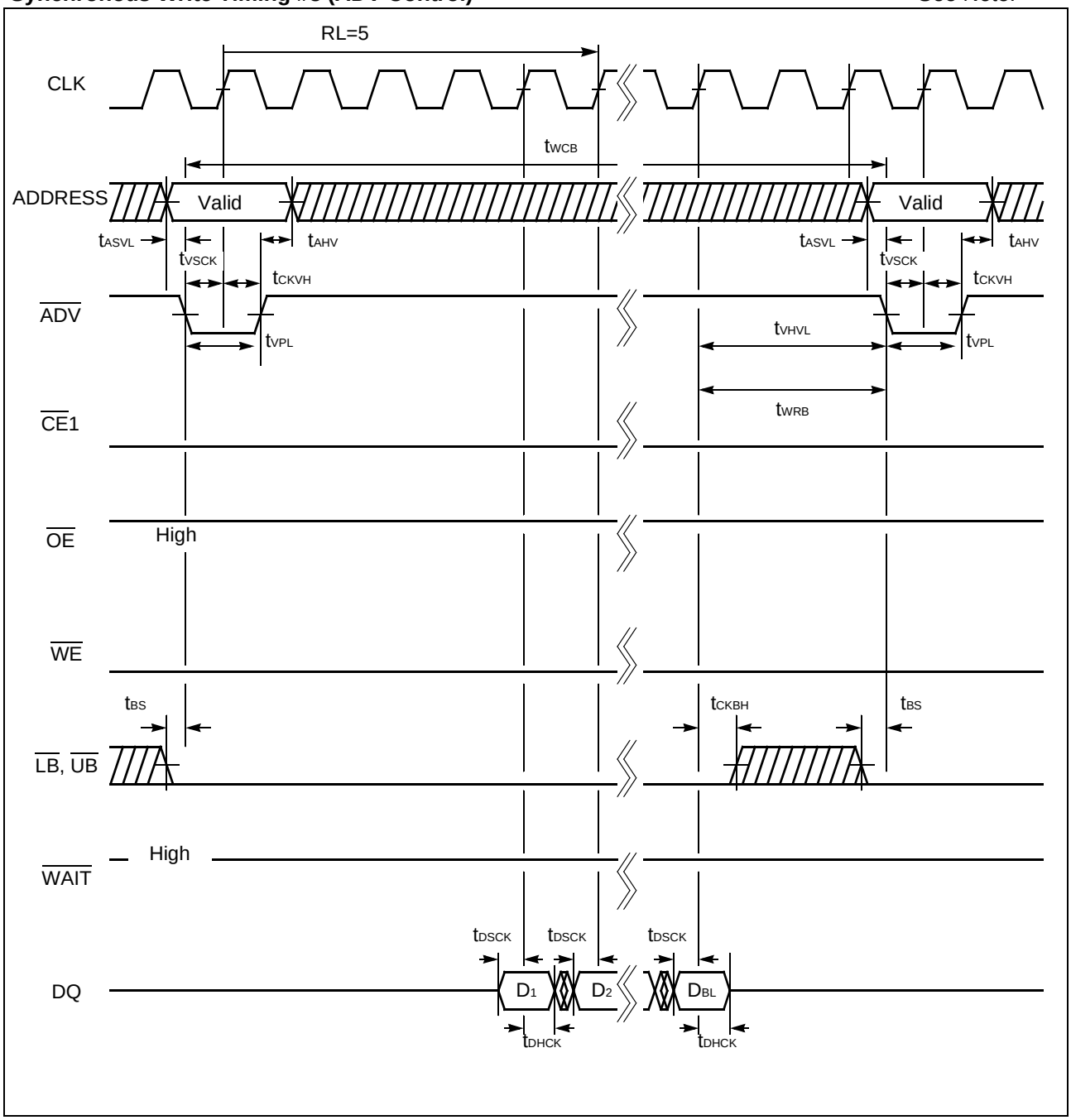
Synchronous Write Timing #2 ($\overline{WE}$ Single Clock Pulse Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

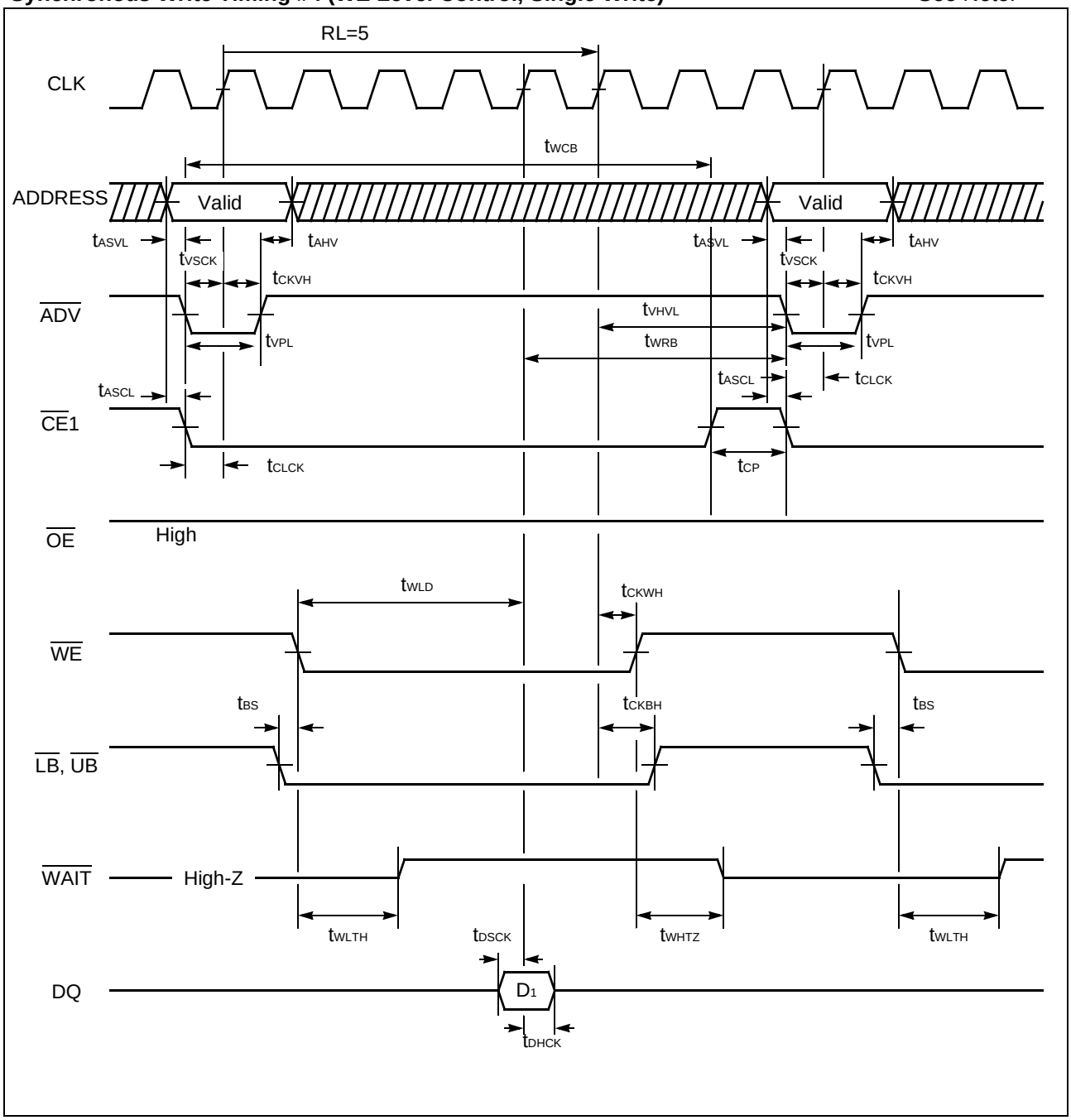
Synchronous Write Timing #3 ($\overline{\text{ADV}}$ Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

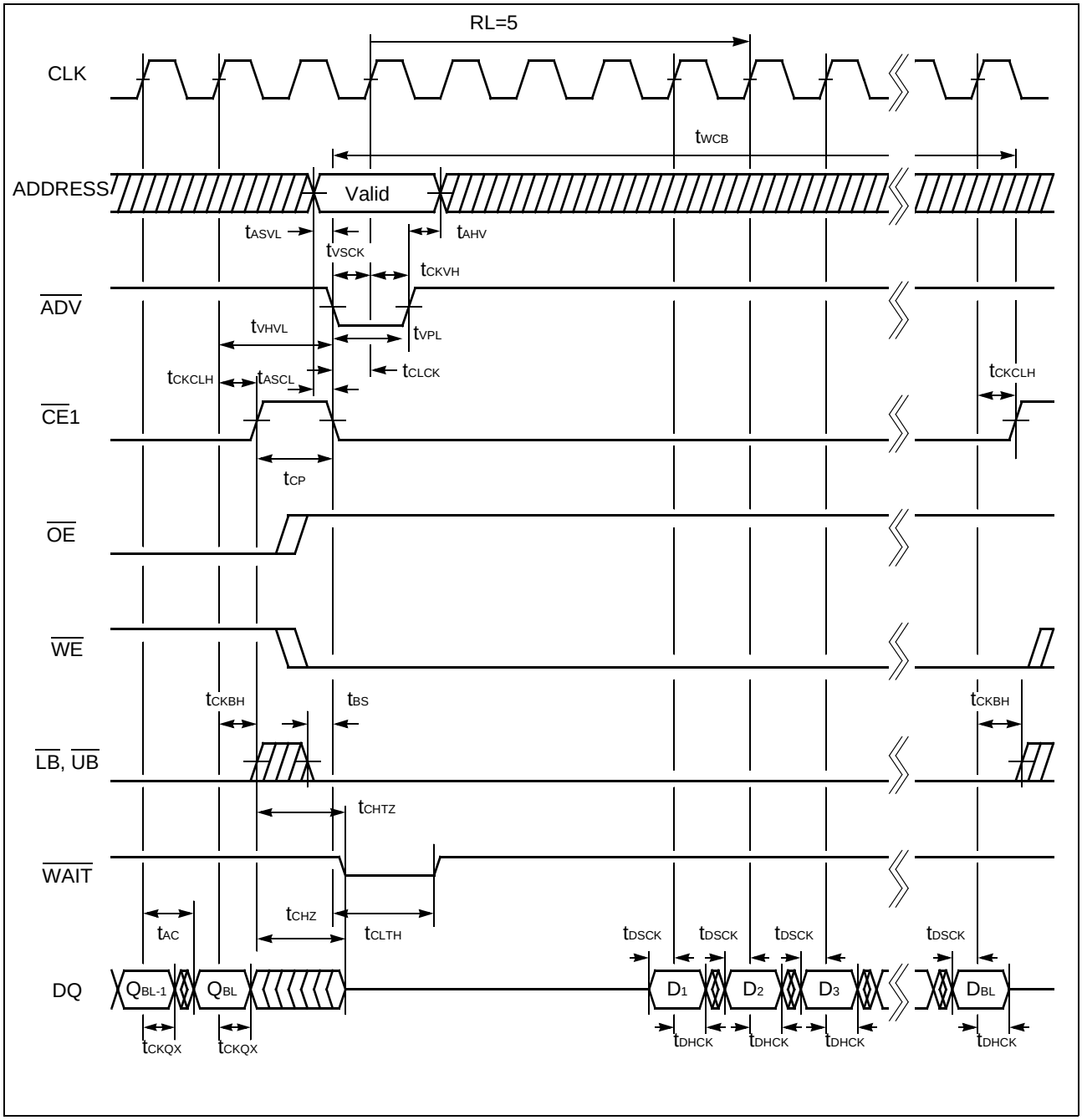
Synchronous Write Timing #4 ($\overline{WE}$ Level Control, Single Write) See Note.



Notes *1: This timing diagram assumes CE2=H, the valid clock edge on rising edge and single write operation.
*2: Write data is latched on the valid clock edge.

■ TIMING DIAGRAMS (Continued)

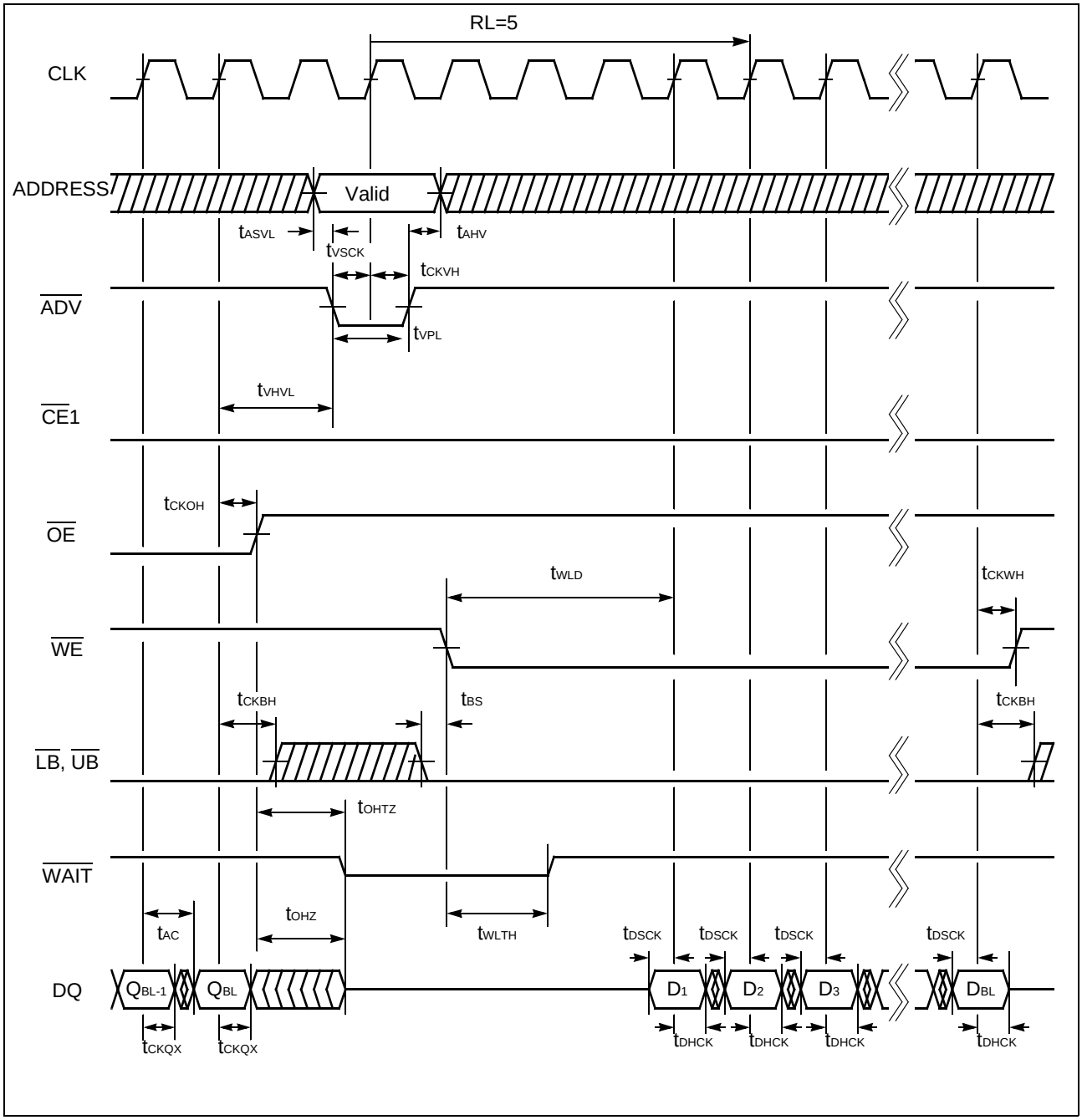
Synchronous Read to Write Timing #1($\overline{CE1}$ Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

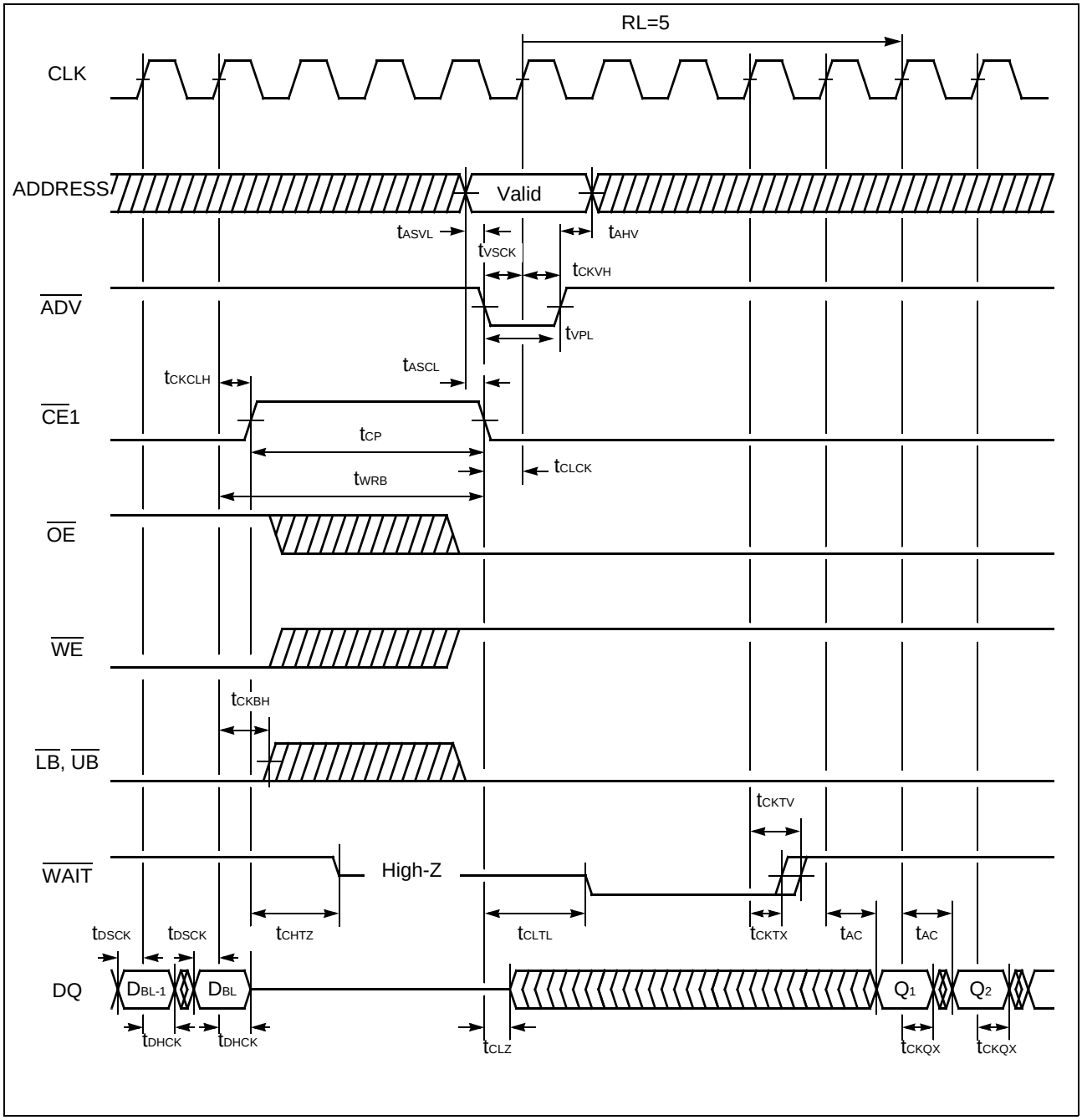
Synchronous Read to Write Timing #2($\overline{\text{ADV}}$ Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

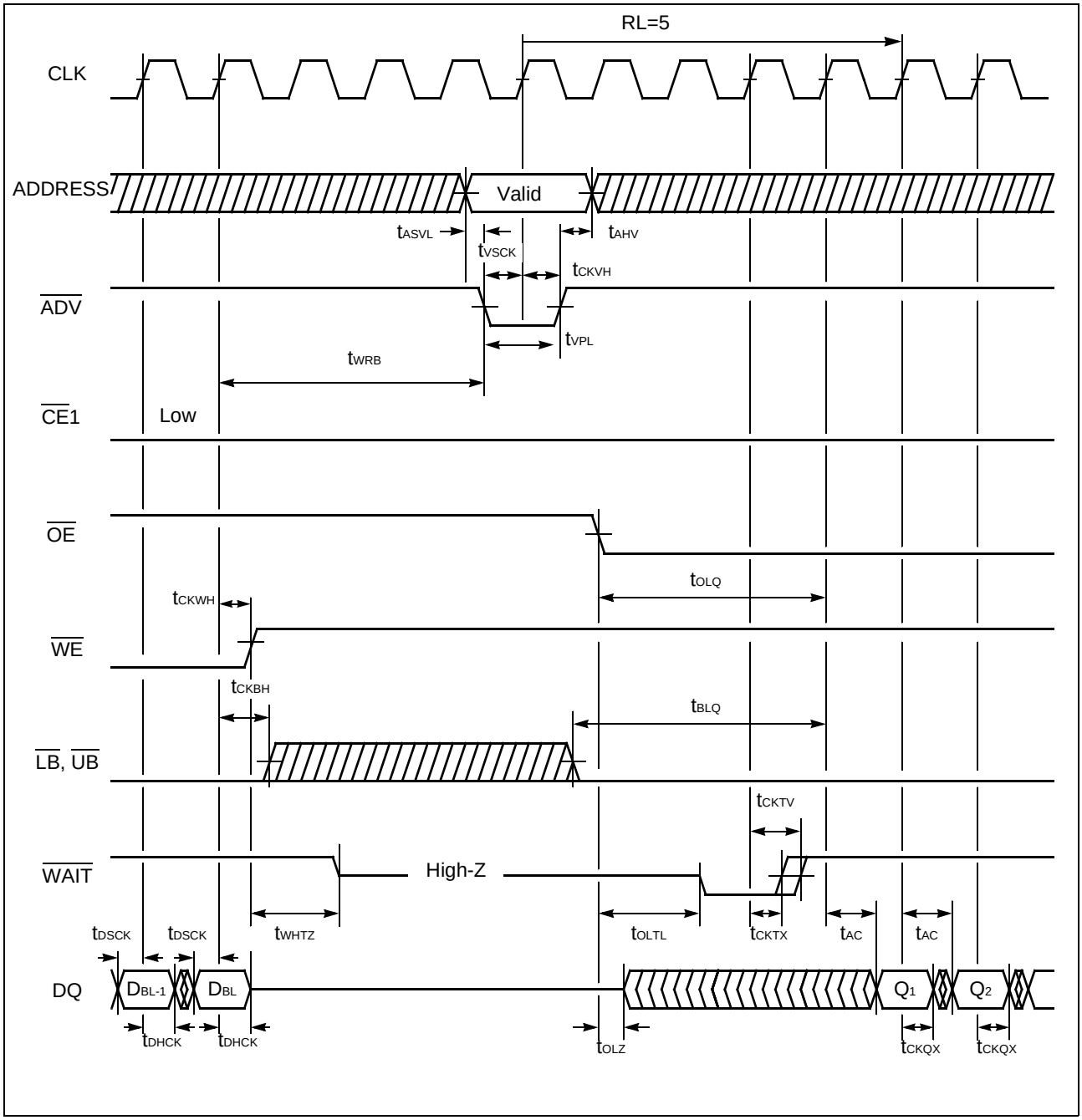
Synchronous Write to Read Timing #1 ($\overline{CE1}$ Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

■ TIMING DIAGRAMS (Continued)

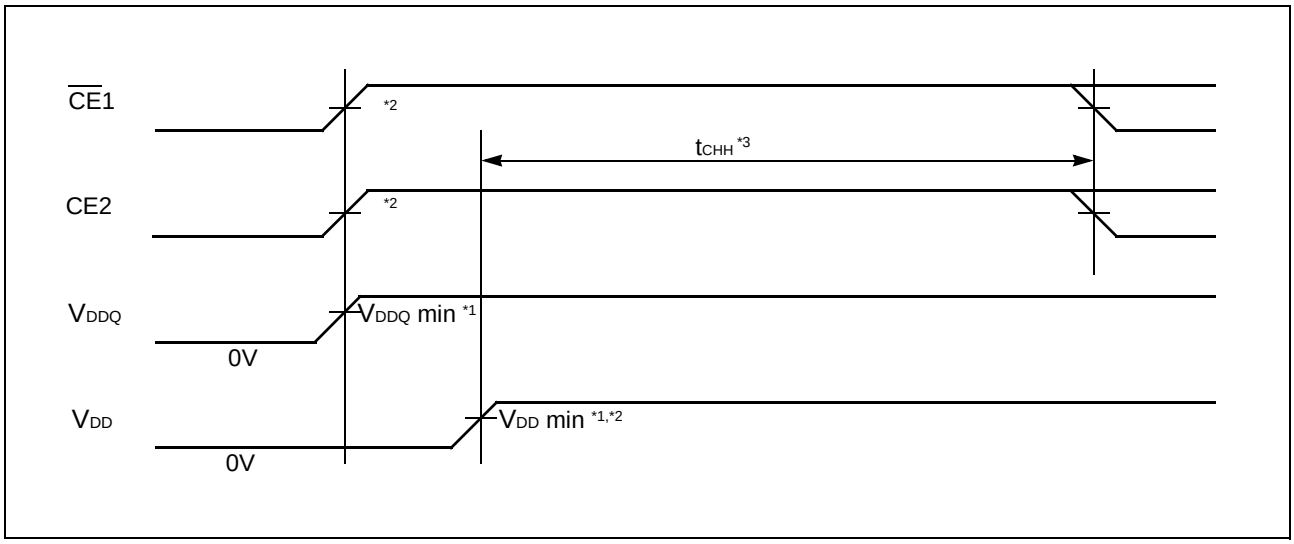
Synchronous Write to Read Timing #2 ($\overline{\text{ADV}}$ Control) See Note.



Note: This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.

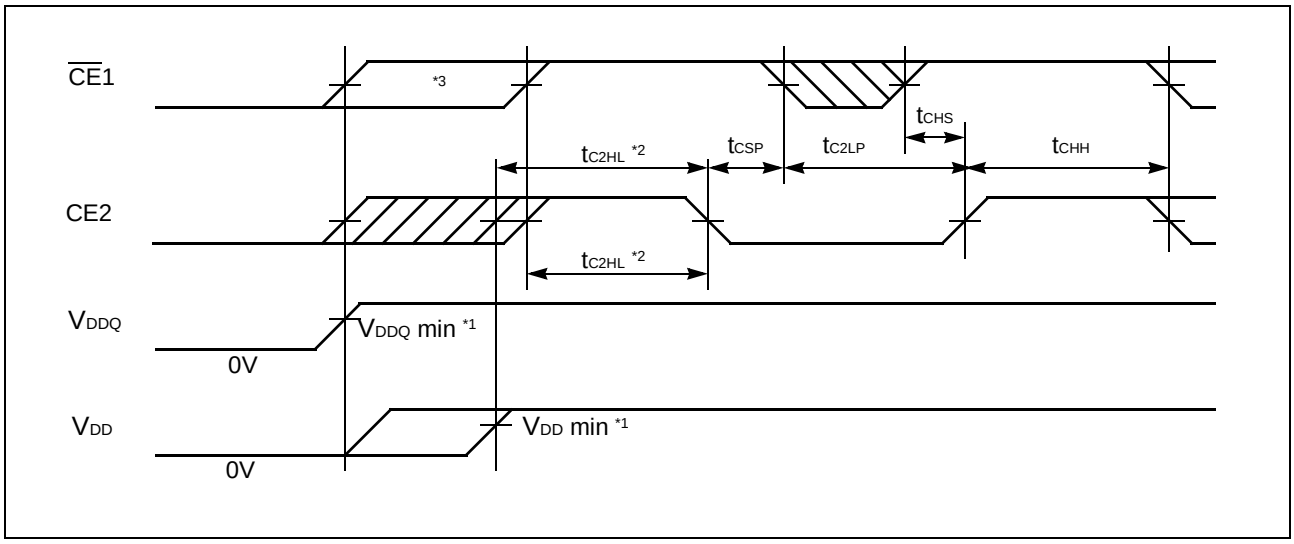
■ TIMING DIAGRAMS (Continued)

POWER-UP Timing #1 See Note.



Notes *1: V_{DDQ} shall be applied and reach the specified minimum level prior to V_{DD} applied.
*2: The both of $\overline{CE}1$ and CE2 shall be brought to High together with V_{DDQ} prior to V_{DD} applied. Otherwise POWER-UP Timing#2 must be applied for proper operation.
*3: The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both $\overline{CE}1$ and CE2.

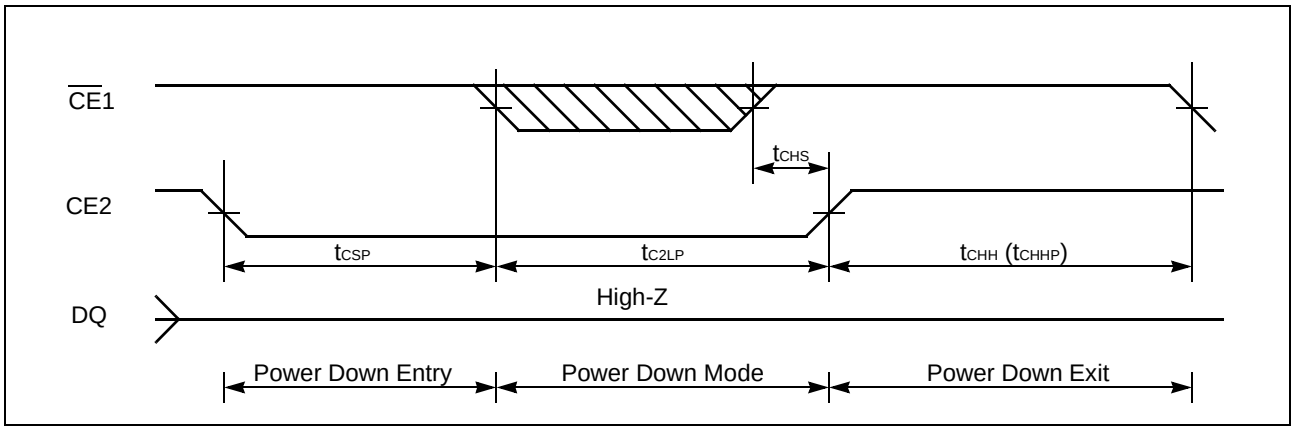
POWER-UP Timing #2 See Note.



Notes *1: V_{DDQ} shall be applied and reach specified minimum level prior to V_{DD} applied.
*2: The t_{C2HL} specifies from CE2 Low to High transition after V_{DD} reaches specified minimum level. If CE2 became High prior to V_{DD} reached specified minimum level, t_{C2HL} is defined from V_{DD} minimum.
*3: $\overline{CE}1$ shall be brought to High prior to or together with CE2 Low to High transition.

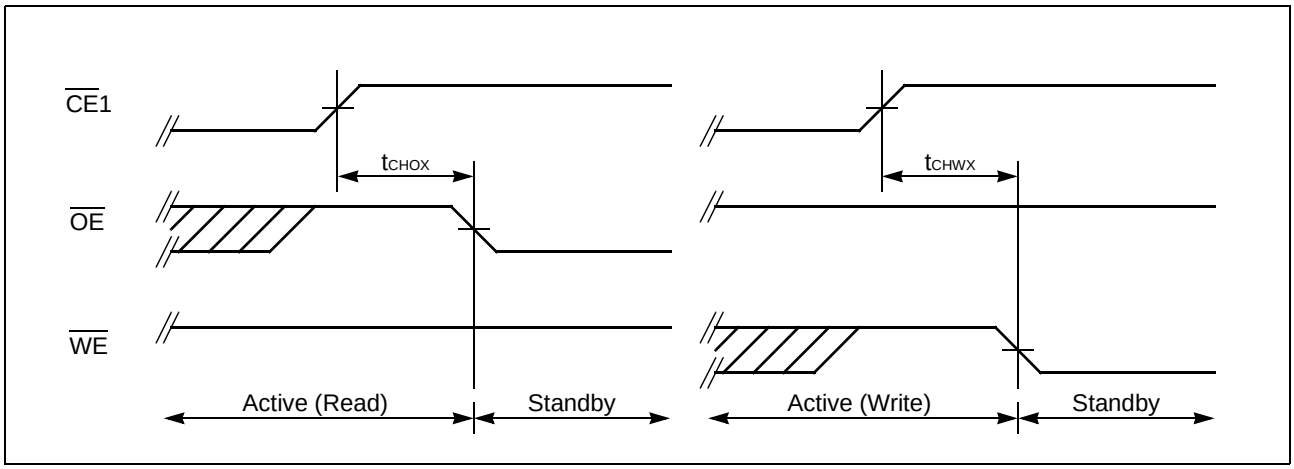
■ TIMING DIAGRAMS (Continued)

POWER DOWN Entry and Exit Timing See Note.



Note: This Power Down mode can be also used as a reset timing if POWER-UP timing above could not be satisfied and Power-Down program was not performed prior to this reset.

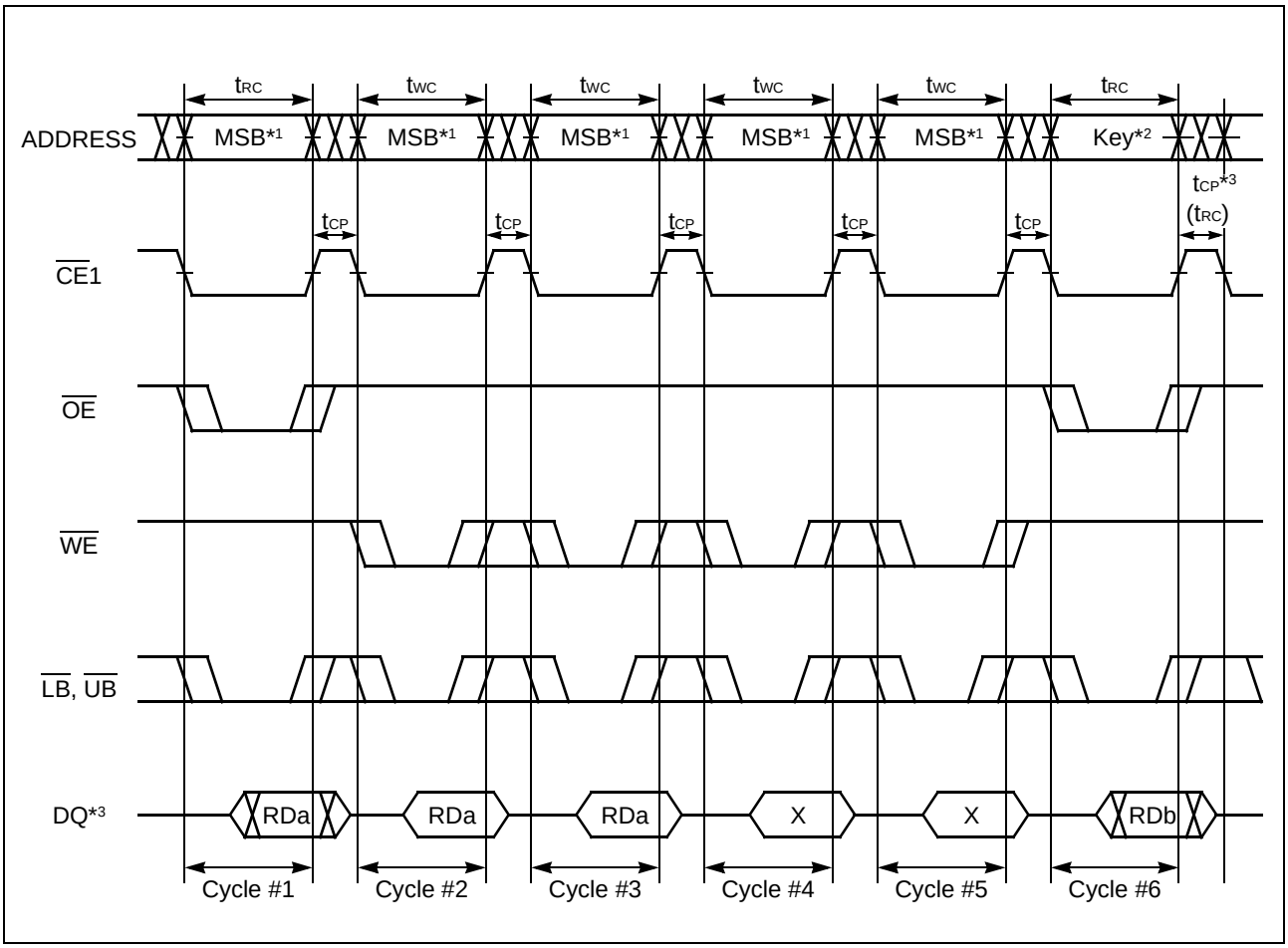
Standby Entry Timing after Read or Write See Note.



Note: Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.
If either of timing is not satisfied, it takes t_{RC} (min) period for Standby mode from $\overline{CE1}$ Low to High transition.

■ TIMING DIAGRAMS (Continued)

Configuration Register Set Timing #1 (Asynchronous Operation) See Note.



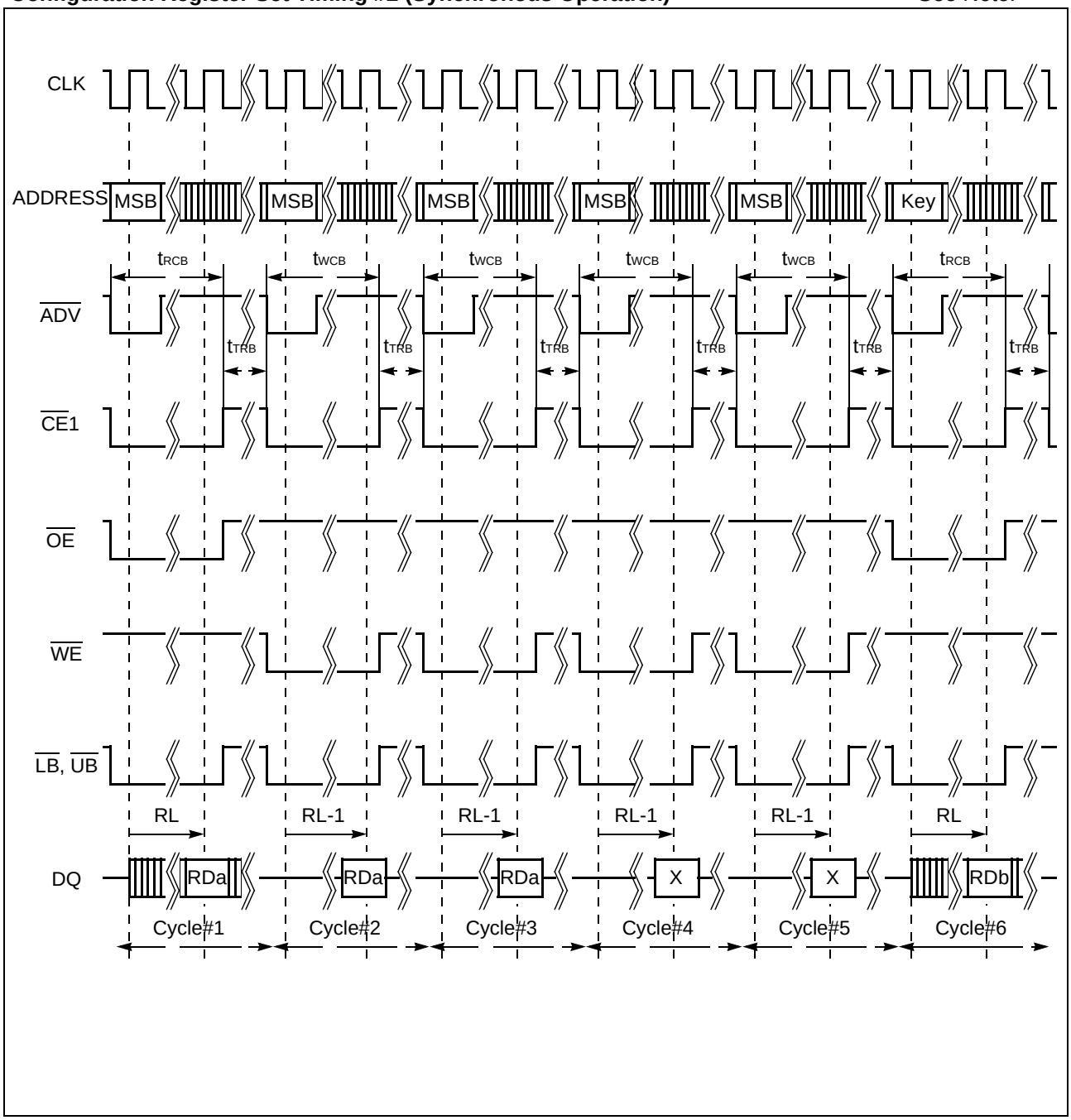
Notes *1: The all address inputs must be High from Cycle #1 to #5.

*2: The address key must confirm the format specified in FUNCTIONAL DESCRIPTION. If not, the operation and data are not guaranteed.

*3: After t_{CP} or t_{RC} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation. t_{CP} and t_{RC} are applicable to returning to asynchronous mode and to synchronous mode respectively.

■ TIMING DIAGRAMS (Continued)

Configuration Register Set Timing #2 (Synchronous Operation) See Note.



Notes *1: The all address inputs must be High from Cycle #1 to #5.

*2: The address key must confirm the format specified in FUNCTIONAL DESCRIPTION. If not, the operation and data are not guaranteed.

*3: After t_{TRB} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.

■ BONDING PAD

Bonding Pad Layout

Please contact local FUJITSU representative for pad layout and pad coordinate information.

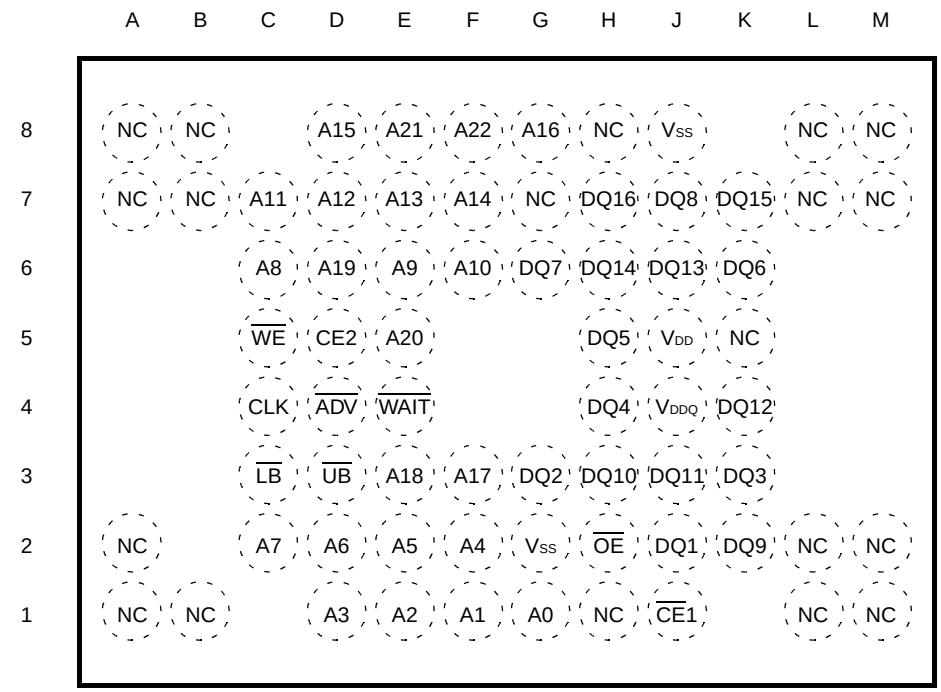
Bonding Pad Description

Pin Name	Description
A_{22} to A_0	Address Input
$\overline{CE}1$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
CLK	Clock Input
$\overline{ADV}$	Address Valid Input (Low Active)
$\overline{WAIT}$	Wait Signal Output
DQ_{16-9}	Upper Byte Data Input/Output
DQ_{8-1}	Lower Byte Data Input/Output
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground
TEST/OPEN	Test/Open (This pad should be left open. Do not use.)

■ PACKAGE FOR ENGINEERING SAMPLES

Ball Assignment

(TOP VIEW)



(BGA-71P-M03)

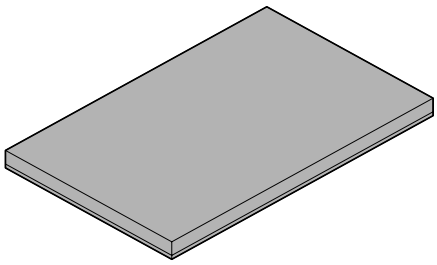
Ball Description

Pin Name	Description
A_{22} to A_0	Address Input
$\overline{CE}1$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
CLK	Clock Input
$\overline{ADV}$	Address Valid Input (Low Active)
$\overline{WAIT}$	Wait Signal Output
DQ_{8-1}	Lower Byte Data Input/Output
DQ_{16-9}	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground
NC	No Connection

■ PACKAGE FOR ENGINEERING SAMPLES (Continued)

Package View

71-pin Plastic FBGA Package

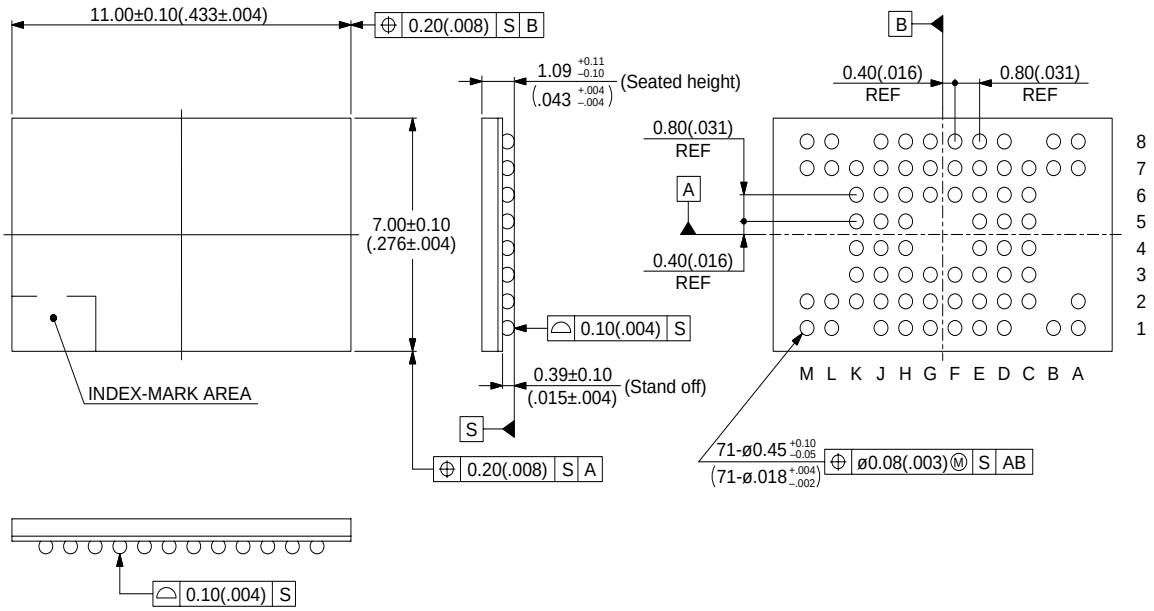


(BGA-71P-M03)

Note: This is for engineering sample only.

Package Dimensions

71-pin plastic FBGA
(BGA-71P-M03)



Dimensions in mm (inch)

Note: This is for engineering sample only.

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