LH538000

CMOS 8M (1M × 8 / 512K × 16) Mask-Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- $\overline{BYTE}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  64-pin, 14 × 20 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH538000 is a mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

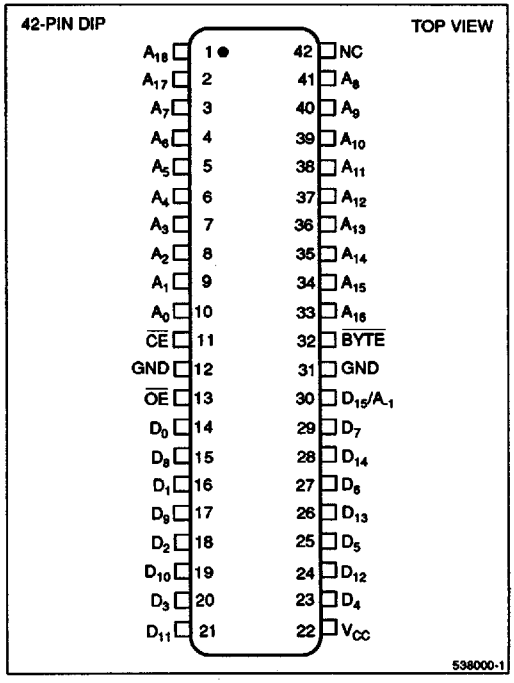

Figure 1. Pin Connections for DIP Package

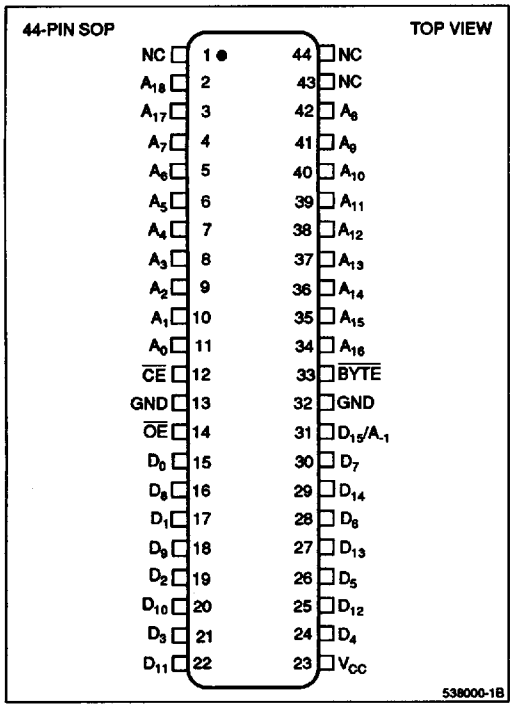

Figure 3. Pin Connections for SOP Package

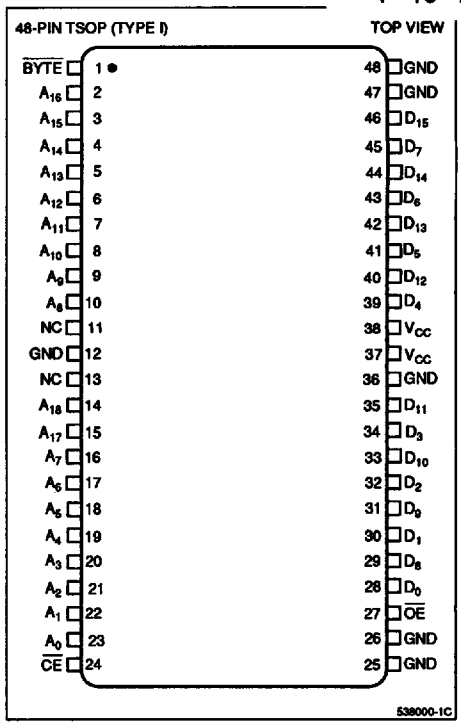

Figure 4. Pin Connections for TSOP Package

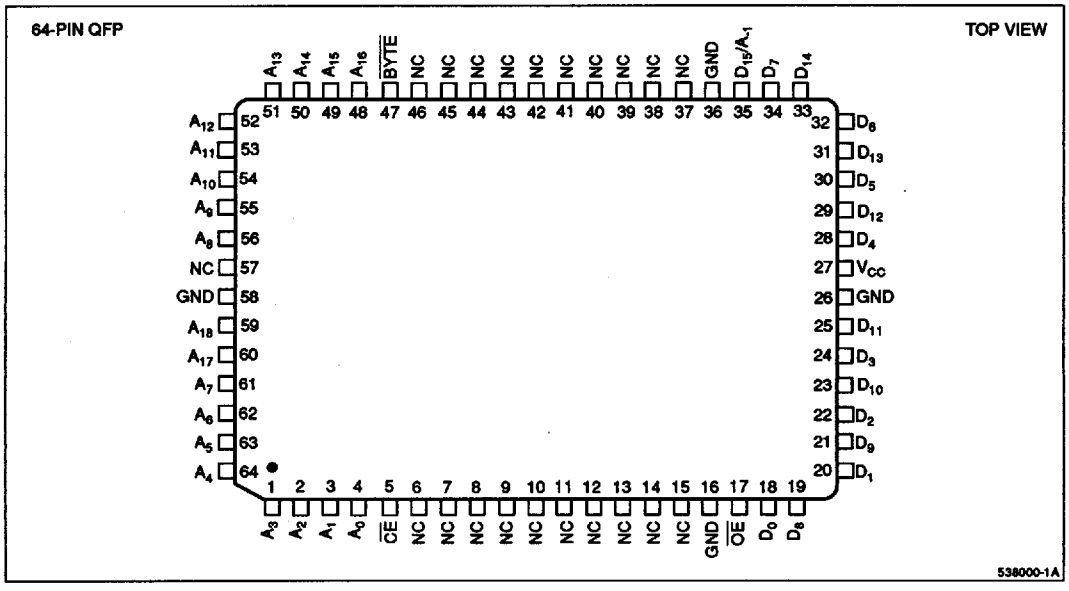

Figure 2. Pin Connections for QFP Package

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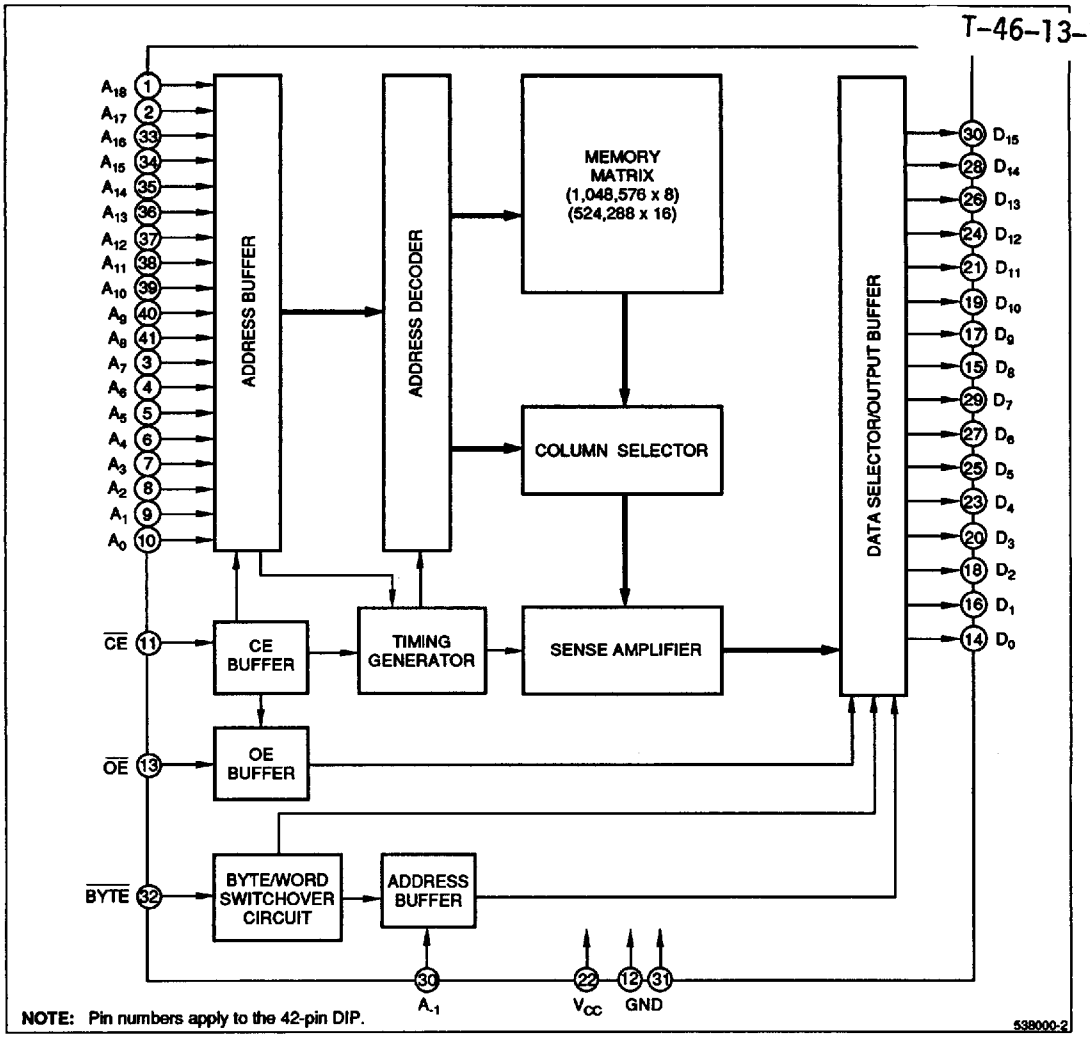

Figure 5. LH538000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address Input (Byte Mode)	1
A_0 - A_{18}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output Enable input	
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

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$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	H	X	X	Non selected	High-Z		Operating (I_{CC})
L	L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	
L	L	L	L	Byte	D_0 - D_7	High-Z	
L	L	L	H	Byte	D_8 - D_{15}	High-Z	

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
	I_{CC3}	t_{RC} = 200 ns		45	mA	3
	I_{CC4}	t_{RC} = 1 µs		35		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}$ /$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

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PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

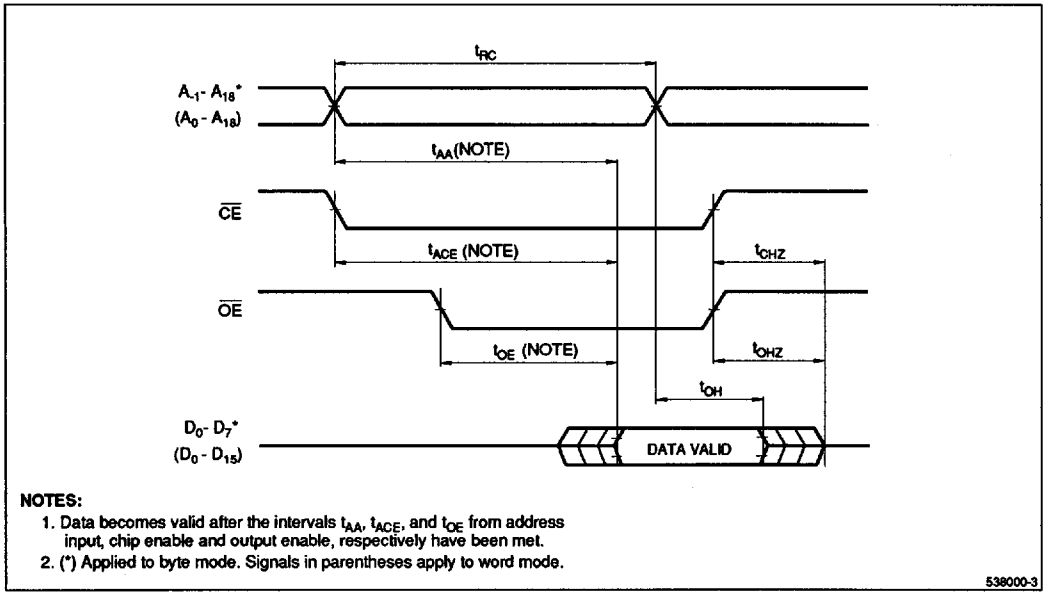
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable and output enable, respectively have been met.
2. (*) Applied to byte mode. Signals in parentheses apply to word mode.

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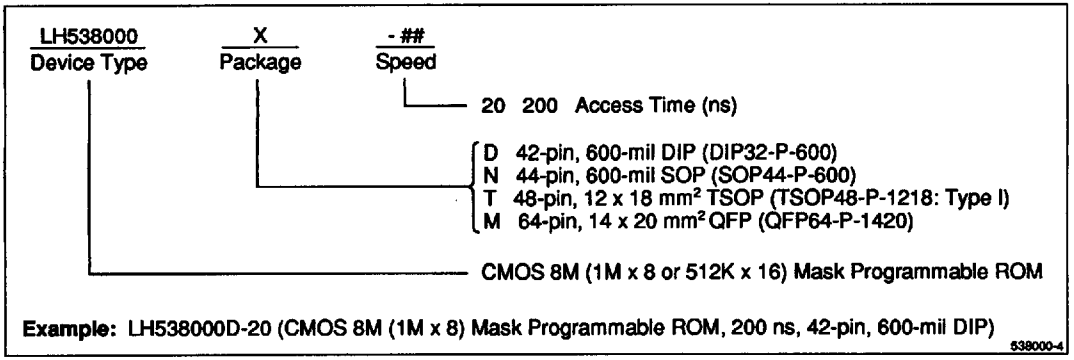
Figure 6. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION

T-46-13-15



Example: LH538000D-20 (CMOS 8M (1M x 8) Mask Programmable ROM, 200 ns, 42-pin, 600-mil DIP)