L64760 Interframe Processor

Description

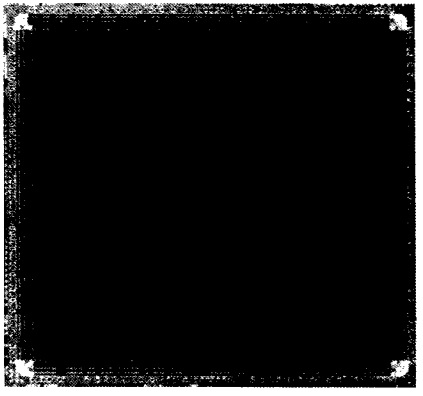
The L64760 performs many of the functions required for the interframe prediction of the CCITT (Consultative Committee on International Telephones and Telegraphs) video compression standard. The current frame data and the motion compensated (optional) previous frame data are supplied as inputs to the device. The loop filtering will be performed if the previous frame data has been motion compensated. The decision is then made to process the data in an intraframe or interframe mode by comparing the energy of the luminance data in the current frame to the energy of the difference between the current and previous frame luminance data. The signal with less energy is sent to the DCT (Discrete Cosine Transform) processor (decision made according to RM8). The reconstructed pixel values are generated by summing the prediction value with the output of the IDCT (Inverse Discrete Cosine Transform).

In decoder mode, the inter-intra decision is transmitted from the variable length decoder and the internal decision circuit is not used.

All delays associated with internal or external processes are compensated internally and hence are transparent to the user.

The device also generates strobes for the variable length coder (L64750) and the quantizer (L64740). In addition, the quantization stepsize from the channel data buffer is latched by the L64760 and sent to the quantization processor at the next macroblock boundary.

The internal inter-intra decision can be overridden externally for forced updating.



L64760 Chip

Features

- Compatible with CCITT H.261
- Loop filter
- Internal/external intra-inter decision
- Performs pixel reconstruction
- System delays internally compensated
- Up to 20/30 MHz clock rates
- Simple external control
- 100-pin CPGA or PPGA (Ceramic or Plastic Pin Grid Array) or PQFP (Plastic Quad Flat Pack) package

Pin Listing and Description

(SIGNAL.0 is always the LSB)

CFI.0:7
Eight-bit data input bus for current frame pixel data. The data is input one macroblock at a time, with each 8 x 8 pixel block raster scanned. This bus is not used in decoder mode.

PFI.0:7
Eight-bit data input bus for previous frame pixel data which has been motion compensated (if desired). The data is input one macroblock at a time, with each 8 x 8 pixel block raster scanned.

PFO.0:7
Eight-bit data output bus for previous frame pixel data. The data is output one macroblock at a time, with each 8 x 8 pixel block raster scanned. This data updates the previous frame data store.

PPIXO.0:8
Nine-bit predicted pixel output bus for data to be coded by the DCT processor. The data is output one macroblock at a time, with each 8 x 8 pixel block raster scanned. This bus is not used in decoder mode.

Pin Listing and Description (SIGNAL.0 is always the LSB) (Continued)

DSYNC
Indicates, when HIGH, the beginning of a block of data on the PPIXO bus (used in encoder mode only).

RP1XI:08
Nine-bit reconstructed pixel input bus for data reconstructed by the IDCT processor. The data is input one macroblock at a time, with each 8 x 8 pixel block in the L64730 output format.

MCI
Motion compensation input flag. When HIGH, it indicates that the current macroblock input on the PFI bus has been motion compensated and should be filtered. This flag is not used in decoder mode.

FSI
Frame start input flag. Indicates, when HIGH, that the first pixel of frame is being input on the PFI and CFI (encoder mode) buses.

BSI
Block start input flag. Indicates, when HIGH, that the first pixel of block is being input on the PFI and CFI (encoder mode) buses.

FSO
Frame start output flag. Indicates, when HIGH, that the first pixel of frame is being output on the PFO bus.

BSO
Block start output flag. Indicates, when HIGH, that the first pixel of block is being output on the PFO bus.

CFSO
Frame start output flag for the variable length coder. Indicates, when HIGH, that the first pixel of frame is being output on the quantizer event bus.

QINTER
Indicates, when HIGH, that the quantization processor should be in intra mode.

QSYNC
Indicates, when HIGH, the beginning of a block of data on the quantization processor COEFFI bus (used in encoder mode only).

QQ.0:4
Five-bit quantization stepsize to be used by the quantization processor.

QUANTI.0:4
Five-bit quantization stepsize input from the channel buffer (not used in decoder mode).

FORCEII
Flag, when HIGH, indicates that the inter-intra decision for the current macroblocks input on CFI and PFI buses is being made externally. The decision itself is input on the INTER pin. Only sampled during encoder mode at the beginning of a macroblock on the PFI bus.

INTER
When HIGH, indicates that the current macroblock input on CFI and PFI buses should be coded with interframe processing. Only sampled during encoder mode when FORCEII is HIGH at the beginning of a macroblock on the PFI bus.

PADR.0:3
Four-bit parameter address input bus. Used to pass the address (identity) of the parameter being transferred on the PDAT bus.

PDAT.0:6
Bidirectional Parameter DATA bus. Used to pass parameters to (encoder mode) and from (decoder mode) the variable length coder.

CLK
System clock. Controls all system functions at LOW to HIGH transitions.

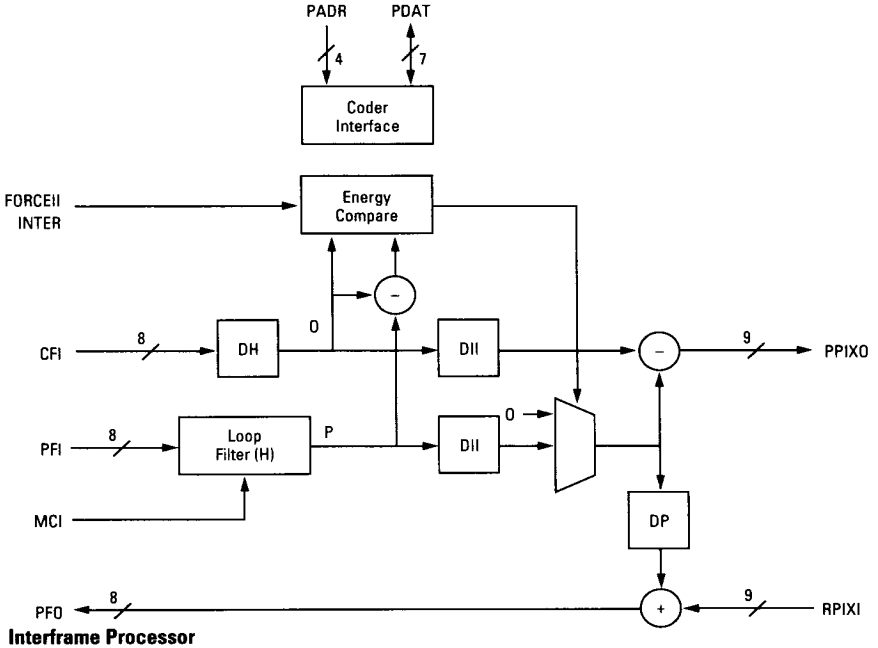
ENC
Encoder mode input flag. When HIGH, the device operates in encoder mode. For decoder mode, ENC, FORCEII and MCI must be LOW.

TESTO
TEST Output pin. Should be left unconnected.

Pin Description Summary

Pin	No. of Pins	I/O	Description
CFI.0:7	8	I	Data input bus
PFI.0:7	8	I	Data input bus
PFO.0:7	8	O	Data output bus
PPIXO.0:8	9	O	Data output bus
DSYNC	1	I	Begin Data Block Flag
RP1XI:08	9	I	Data Input Bus
MCI	1	I	Motion Compensation Input Flag
FSI	1	I	Frame Start Input Flag
BSI	1	I	Block Start Input Flag
FSO	1	O	Frame Start Output Flag
BSO	1	O	Block Start Output Flag
CFSO	1	O	Frame Start Output Flag
QINTER	1	O	Inter Mode Flag
QSYNC	1	O	Begin Data Block Flag
QQ.0:4	5	O	Quantization Stepsize
QUANTI.0:4	5	I	Quantization Stepsize
FORCEII	1	I	Internal/External decision flag
INTER	1	I	Inter-Frame Mode Flag
PADR.0:3	4	I	Address Input Bus
PDAT.0:6	7	I/O	Data Bus
CLK	1	I	Clock
ENC	1	I	Encoder Mode Input Flag
TEST0	1	O	Test Output. No Connect

Block Diagram



Interframe Processor

Architecture

The interframe processor performs the operations associated with video encoders and decoders operating with temporal prediction.

In encoder mode, the current and previous frame data are input on the CFI and PFI buses, respectively, one macroblock at a time. The macroblocks are comprised of four 8 x 8 luminance blocks followed by two chrominance blocks. For CCITT H.261 operation, the four luminance blocks are followed by the two 8 x 8 chrominance blocks. Each of the 8 x 8 data blocks is input in a raster scanned order. The six blocks of data must be followed by one or more block times in which video data is not being processed. This is required to provide time for the L64750 to encode and decode the header information.

The data on the PFI bus will be filtered by the Loop Filter to remove some of the blocking artifacts if MCI is HIGH. The delay element, DH, delays the data on the CFI bus accordingly. The energy of the original data (O) and the prediction error (O-P) are compared and the signal with the least energy is supplied on the PPIXO bus to be transformed by the DCT, quantized and coded. If FORCEII is HIGH, the energy comparison is ignored. The O signal is sent to the DCT if INTER is LOW and the O-P signal is sent to the DCT if INTER is HIGH. For both cases, the DII blocks delay the data streams to compensate for the delay encountered in the Energy Compare block.

The reconstructed pixels from the IDCT are input on RPIXI bus and are summed with the predicted value if the temporal prediction was employed, or unchanged if temporal prediction was not used. The block DP compensates for the external delay associated with the forward and inverse DCT and quantization (when using L64730 and L64740). The updated prediction value is output on the PFO bus in the same order as data is input on the PFI bus.

The data on the PFI and CFI buses is accompanied by two flags; FSI and BSI which indicate that the first pixels of the image and block, respectively, are on the CFI and PFI buses. Similarly, the data on the PFO bus is accompanied by two flags; FSO and BSO which indicate that the first pixel of the image and block, respectively, is on the bus.

The DSYNC, QSYNC and CFS are flags which indicate to the DCT, quantization and variable length coding processors, respectively, that the data being received on the corresponding input ports are the beginning of a block for the DCT and quantization processors and the beginning of a frame for the coder.

The device communicates parameters with the coder through the coder interface. When the coder places the appropriate address for the parameter on the PADR bus, the L64760 will place the corresponding parameter on the PDAT. The parameters that are transferred in this manner are the inter-intra mode bit, a bit indicating that the loop filter is active and the quantization stepsize.

In decoder mode, only a subset of the circuit is used. The current frame data input is not available and hence the CFI bus is not used and the inter-intra decision is not determined by the device. Similarly, the PPIXO bus is inactive. The basic function of the device is to perform the loop filter and final pixel reconstruction.

The operating parameters are sent from the coder to the interframe processor in a manner similar to that described for the encoder case.

Performance

The interframe processor operates at pixel rates of 30-40 Mpixels/sec. This level of performance is sufficient for processing broadcast quality video in addition to the CCITT format video.

Operating Modes

The operation mode is set via the FORCEII, MCI, INTER and ENC pins. Table 1 summarizes the basic operations.

Table 1. Operating Modes

ENC	FORCEII	INTER	MCI	Normal Mode
1	0	X	0	Encoder, use internal inter-intra decision, loop filter off
1	0	X	1	Encoder, use internal inter-intra decision, loop filter on
1	1	1	0	Encoder, inter mode, loop filter off
1	1	1	1	Encoder, inter mode, loop filter on
1	1	0	X	Encoder, intra mode
0	0	0	0	Decoder mode, parameters loaded from PDAT
				Special Modes
0	X	X	1	Reset mode
0	1	1	X	Test inter energy computation, not normally used
0	1	0	X	Test intra energy computation, not normally used

Reset mode is not normally used. If the device is reset for two cycles, all strobes (BSO, FSO, DSYNC, QSYNC and CFS) will not go HIGH until valid data arrives. If, however, the device is operated for 700 cycles after power up, the strobes will be valid without using the reset mode.

The two test modes are used to verify the internal measures of the energy computed for intra and inter modes. In addition, it is used when measuring the input transition levels.

The PDAT bus is used to communicate the quantization values and the status of the inter-intra and loop filter decisions between the L64760 and L64750 as specified in Table 2. In encoder mode (ENC HIGH), the L64760 will place this data on the PDAT bus in the cycle after address 5 (0101) is detected on the PADR bus. Otherwise, the PDAT bus will float. In decoder mode (ENC, FORCEII, MCI LOW), the L64760 will latch the parameters on the PDAT bus whenever address 5 is detected on the PADR bus. These parameters will take effect at the next macroblock boundary.

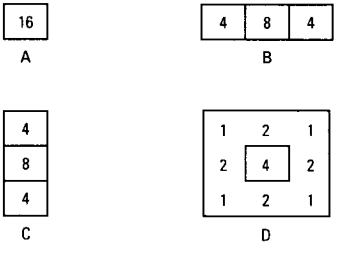
Table 2. Values on PDAT Bus

PDAT.6	PDAT.5	PDAT.4	PDAT.3	PDAT.2	PDAT.1	PDAT.0
Q.4	Q.3	Q.2	Q.1	Q.0	INTER	FILT_ON

Loop Filter

The loop filter is active for macroblocks in which motion compensation has been performed. The signal MCI indicates that the macroblock should be filtered in encoder mode and the parameter, FILT ON, from the decoder indicates that the loop filter is active in decode mode.

The loop filter operation is a separable operation. The filter is block oriented and different filter coefficients are used for different positions within the 8 x 8 data block. Figure 1 shows the nine sets of coefficients at the left. The position within the 8 x 8 data block where each set of filter coefficients is used is shown in the right half of the figure. Note that each coefficient is multiplied by the scale factor 1/16 and that the results are rounded to 8 bits.



A	B	B	B	B	B	B	A
C	D	D	D	D	D	D	C
C	D	D	D	D	D	D	C
C	D	D	D	D	D	D	C
C	D	D	D	D	D	D	C
C	D	D	D	D	D	D	C
C	D	D	D	D	D	D	C
A	B	B	B	B	B	B	A

Figure 1. Coefficients for Loop Filter

Inter-Intra Decision

In encoder mode, the decision to code the macroblock using interframe or intraframe techniques will be made automatically. The system can, however, override the automatic decision (via FORCEII and INTER). In decoder mode, the decision is simply transmitted by the encoder to the decoder.

Normally, it will be desirable to code the macroblock using interframe (temporal and spatial) prediction when the temporal correlation is high. The device measures the energy of the temporal prediction error and compares this to the variance of the original signal. Each is computed for the 16 x 16 luminance blocks and are defined as follows:

O(k,l) is the original macroblock

S(k,l) is the motion compensated macroblock.

VAROR (VARiance of the ORiginal) =

$$\frac{\sum_{K=1}^{16}\sum_{l=1}^{16} O(k,l)^2}{256} - \left[\frac{\sum_{K=1}^{16}\sum_{l=1}^{16} O(k,l)}{256}\right]^2$$

VAR (VARiance of the temporal prediction) =

$$\frac{\sum_{K=1}^{16}\sum_{l=1}^{16} \left[S(k,l)-O(k,l)\right]^2}{256}$$

The choice between inter and intra mode is made as shown in Figure 2. Note that inter mode includes the solid line.

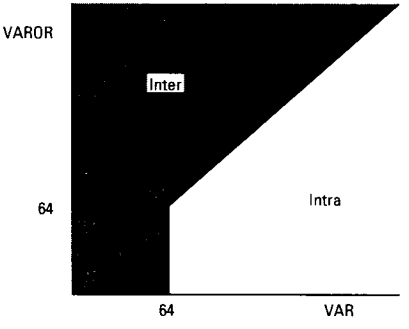


Figure 2. Inter-Intra Mode Decision

Functional Waveforms

Encoder Mode

Operation of the device in encoder mode is illustrated in Figure 3. The previous and current frame data is scanned into the device one macroblock at a time. The macroblocks consist of four luminance blocks (Y0-Y3) and two chrominance blocks (C0,C1). The macroblocks are separated by any number of header blocks (H). Each block is input over 64 cycles in a raster scan fashion. The data input during the header block time is ignored. FSI goes HIGH for the first pixel of the frame while BSI goes HIGH for the first pixel of each active block. Note that BSI does not go HIGH during the header blocks. All strobes in the diagram go HIGH for a single cycle.

The signals, FORCEII, INTER and MCI are sampled during the first cycle of each macroblock. In the example shown, the inter-intra decision is made internally (FORCEII LOW) in the first and fourth macroblocks and is made externally (FORCEII HIGH) in the second and third macroblocks. The second and fourth macroblocks have been motion compensated (MCI HIGH).

The prediction error to be processed by the DCT and the block start strobe (DYSNC) are output 273 cycles after and in the same format as the input.

The signals for the quantizer appear 371 cycles after the corresponding input data to account for the delay of the L64760 (273 cycles) and L64730 (98 cycles). QSYNC indicates the beginning of valid blocks at the quantizer input and QINTER indicates the type quantization to use.

CFS indicates the beginning of the frame at the variable length coder input.

The reconstructed pixel data, generated by the inverse quantizer and IDCT, is input on the RPIXI bus, 610 cycles after the corresponding input data and in the order output by the L64730.

Finally, previous frame update information is output on the PFO, BSO and FSO signals delayed by 677 cycles but in the same format as it was input on the PFI, BSI and FSI pins.

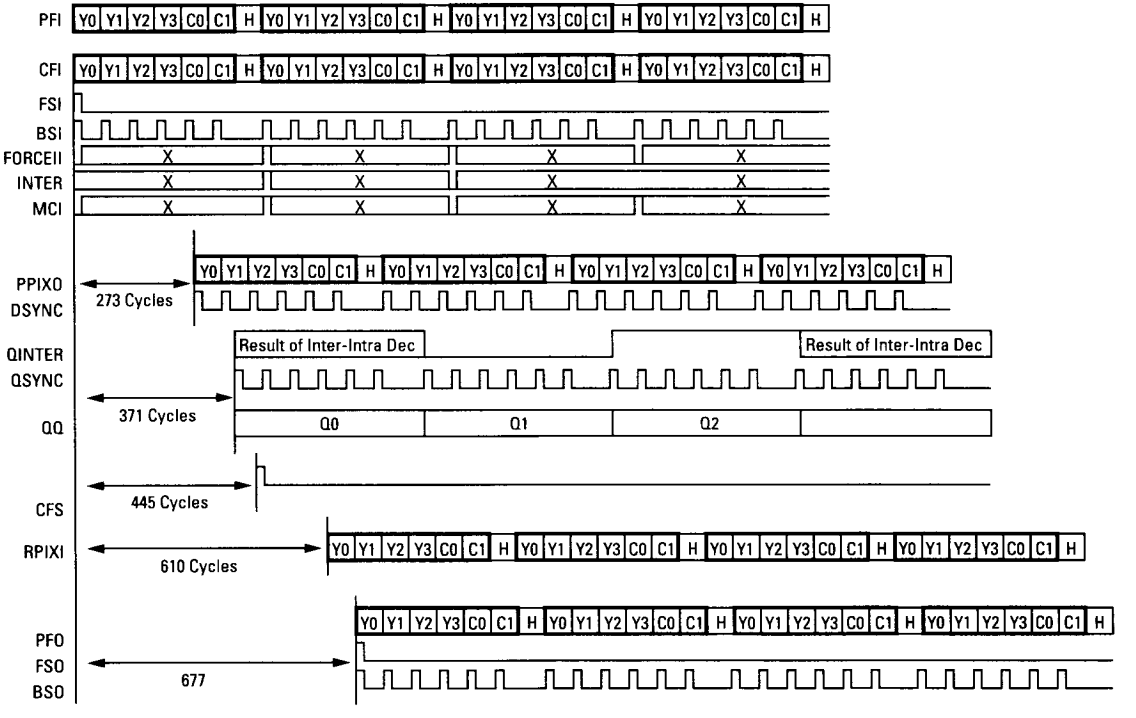


Figure 3. Encoder Mode Functional Waveforms

Functional Waveforms

Decoder Mode

Operation of the device in decoder mode is similar to that in encoder mode except that many functions are not used. The previous frame (PFI) data is scanned into the device as in encoder mode. The strobes, BSI and FSI, are also generated as before.

The QUANT value on the QQ bus is sent to the quantizer immediately to keep it aligned with the decoded DCT coefficients arriving from the CVLC. The reconstructed pixels are input on the RPIXI bus 98 cycles after the corresponding PFI data, and the previous frame update information and strobes are output 165 cycles later.

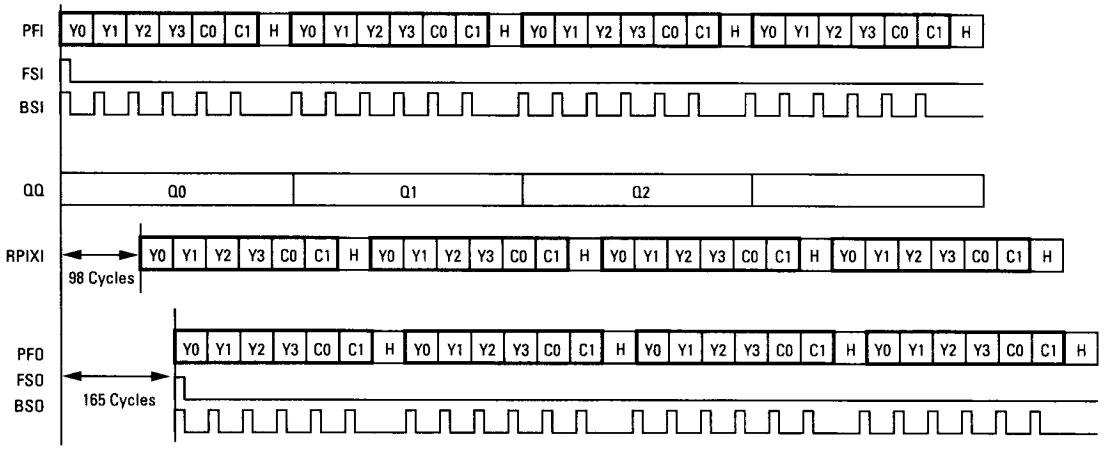
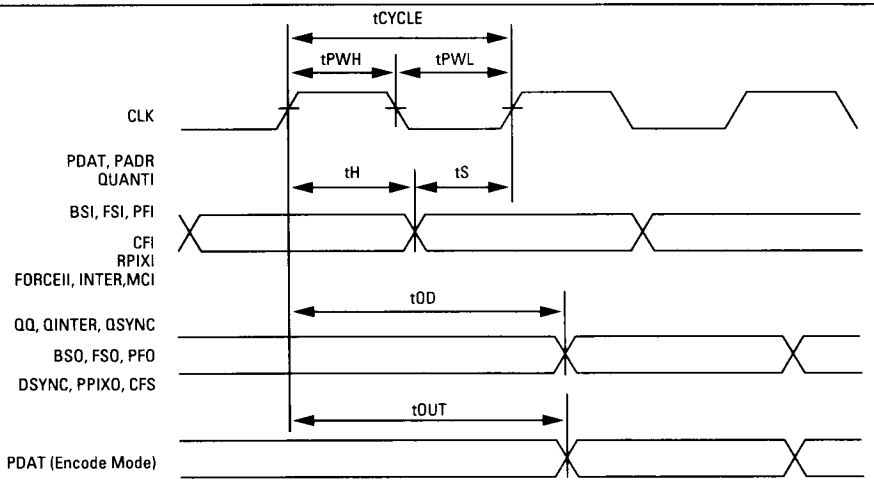


Figure 4. Decoder Mode Functional Waveforms

AC Timing Waveforms



AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

		L64760-30		L64760-20	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**
tCYCLE	CLK cycle time	33		50	
tPWH	Min CLK pulse width, HIGH	15		18	
tPWL	Min CLK pulse width, LOW	15		18	
tS	Input setup time to CLK	8		10	
tH	Input hold time CLK	1		1	
tOD	Output Delay from CLK		22*		25*
tOUT	PDAT Output Delay from CLK		22*		25*

Notes:
1. All times are in ns.
2. *output loading = 50 pF.

Package Pin Information (100-Pin PQFP, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
55	BSI	26	FSO	59	PFI.2	34	PPIXO.2	88	QUANTI.2	4	VDD
25	BSO	82	INTER	60	PFI.3	35	PPIXO.3	89	QUANTI.3	42	VDD
68	CFI.0	83	MCI	61	PFI.4	36	PPIXO.4	90	QUANTI.4	54	VDD
69	CFI.1	10	PADR.0	62	PFI.5	37	PPIXO.5	43	RPIXI.0	64	VDD
70	CFI.2	11	PADR.1	63	PFI.6	38	PPIXO.6	44	RPIXI.1	79	VDD
71	CFI.3	12	PADR.2	67	PFI.7	39	PPIXO.7	45	RPIXI.2	91	VDD
72	CFI.4	13	PADR.3	17	PFO.0	40	PPIXO.8	46	RPIXI.3	16	VSS
73	CFI.5	100	PDAT.0	18	PFO.1	98	QUINTER	47	PRIXI.4	30	VSS
74	CFI.6	1	PDAT.1	19	PFO.2	93	QQ.0	48	PRIXI.5	41	VSS
75	CFI.7	2	PDAT.2	20	PFO.3	94	QQ.1	49	RPIXI.6	5	VSS
14	CFS	6	PDAT.3	21	PFO.4	95	QQ.2	50	RPIXI.7	52	VSS
65	CLK	7	PDAT.4	22	PFO.5	96	QQ.3	51	RPIXI.8	66	VSS
31	DSYNC	8	PDAT.5	23	PFO.6	97	QQ.4	84	TESTO	76	VSS
85	ENC	9	PDAT.6	24	PFO.7	99	QSYNC	15	VDD	92	VSS
81	FORCEII	57	PFI.0	32	PPIXO.0	86	QUANTI.0	27	VDD		
56	FSI	58	PFI.1	33	PPIXO.1	87	QUANTI.1	29	VDD		

Package Pin Information (100-Pin PQFP, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	PDAT.1	18	PFO.1	35	PPXIO.3	51	RPIXI.8	68	CFI.0	87	QUANTI.1
2	PADT.2	19	PFO.2	36	PPIXO.4	52	VSS	69	CFI.1	88	QUANTI.2
4	VDD	20	PFO.3	37	PPIXO.5	54	VDD	70	CFI.2	89	QUANTI.3
5	VSS	21	PFO.4	38	PPIXO.6	55	BSI	71	CFI.3	90	QUANTI.4
6	PDAT.3	22	PFO.5	39	PPIXO.7	56	FSI	72	CFI.4	91	VDD
7	PDAT.4	23	PFO.6	40	PPIXO.8	57	PFI.0	73	CFI.5	92	VSS
8	PDAT.5	24	PFO.7	41	VSS	58	PFI.1	74	CFI.6	93	QQ.0
9	PDAT.6	25	BSO	42	VDD	59	PFI.2	75	CFI.7	94	QQ.1
10	PADR.0	26	FSO	43	RPIXI.0	60	PFI.3	76	VSS	95	QQ.2
11	PADR.1	27	VDD	44	RPIXI.1	61	PFI.4	79	VDD	96	QQ.3
12	PADR.2	29	VDD	45	RPIXI.2	62	PFI.5	81	FORCEII	97	QQ.4
13	PADR.3	30	VSS	46	RPIXI.3	63	PFI.6	82	INTER	98	QINTER
14	CFS	31	DSYNC	47	RPIXI.4	64	VDD	83	MCI	99	QSYNC
15	VDD	32	PPIXO.0	48	RPIXI.5	65	CLK	84	TESTO	100	PDAT.0
16	VSS	33	PPIXO.1	49	RPIXI.6	66	VSS	85	ENC		
17	PFO.0	34	PPIXO.2	50	RPIXI.7	67	PFI.7	86	QUANTI.0		

Package Pin Information (100-Pin PGA, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
M13	BSI	M1	FSO	K13	PFI.2	N4	PPIXO.2	B8	QUANTI.2	B2	VDD
L1	BSO	A11	INTER	J12	PFI.3	M5	PPIXO.3	A8	QUANTI.3	C7	VDD
F13	CFI.0	B10	MCI	J13	PFI.4	N5	PPIXO.4	B7	QUANTI.4	G2	VDD
F12	CFI.1	E2	PADR.0	H11	PFI.5	L6	PPIXO.5	N8	RPIXI.0	H13	VDD
F11	CFI.2	E1	PADR.1	H12	PFI.6	M6	PPIXO.6	M8	RPIXI.1	L2	VDD
E13	CFI.3	F3	PADR.2	G13	PFI.7	N6	PPIXO.7	L8	RPIXI.2	M12	VDD
E12	CFI.4	F2	PADR.3	G1	PFO.0	M7	PPIXO.8	N9	RPIXI.3	M2	VDD
D13	CFI.5	A3	PDAT.0	H1	PFO.1	A4	QINTER	M9	RPIXI.4	N7	VDD
D12	CFI.6	A2	PDAT.1	H2	PFO.2	A6	QQ.0	N10	RPIXI.5	A7	VSS
C13	CFI.7	B3	PDAT.2	H3	PFO.3	B6	QQ.1	M10	RPIXI.6	B1	VSS
F1	CFS	C2	PDAT.3	J1	PFO.4	C6	QQ.2	N11	RPIXI.7	B13	VSS
G12	CLK	C1	PDAT.4	J2	PFO.5	A5	QQ.3	N12	RPIXI.8	G11	VSS
M3	DSYNC	D2	PDAT.5	K1	PFO.6	B5	QQ.4	A10	TESTO	G3	VSS
B9	ENC	D1	PDAT.6	K2	PFO.7	B4	QSYNC	A1	VDD	L7	VSS
B11	FORCEII	L13	PFI.0	N3	PPIXO.0	A9	QUANTI.0	A13	VDD	M11	VSS
L12	FSI	K12	PFI.1	M4	PPIXO.1	C8	QUANTI.1	B12	VDD	N2	VSS

Package Pin Information (100-Pin PGA, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	VDD	B5	QQ.4	D2	PDAT.5	G11	VSS	K13	PFI.2	M9	RPIXI.4
A2	PDAT.1	B6	QQ.1	D12	CFI.6	G12	CLK	L1	BSO	M10	RPIXI.6
A3	PDAT.0	B7	QUANTI.4	D13	CFI.5	G13	PFI.7	L2	VDD	M11	VSS
A4	QINTER	B8	QUANTI.2	E1	PADR.1	H1	PFO.1	L6	PPIXO.5	M12	VDD
A5	QQ.3	B9	ENC	E2	PADR.0	H2	PFO.2	L7	VSS	M13	BSI
A6	QQ.0	B10	MCI	E12	CFI.4	H3	PFO.3	L8	RPIXI.2	N2	VSS
A7	VSS	B11	FORCEII	E13	CFI.3	H11	PFI.5	L12	FSI	N3	PPIXO.0
A8	QUANTI.3	B12	VDD	F1	CFS	H12	PFI.6	L13	PFI.0	N4	PPIXO.2
A9	QUANTI.0	B13	VSS	F2	PADR.3	H13	VDD	M1	FSO	N5	PPIXO.4
A10	TESTO	C1	PDAT.4	F3	PADR.2	J1	PFO.4	M2	VDD	N6	PPIXO.7
A11	INTER	C2	PDAT.3	F11	CFI.2	J2	PFO.5	M3	DSYNC	N7	VDD
A13	VDD	C6	QQ.2	F12	CFI.1	J12	PFI.3	M4	PPIXO.1	N8	RPIXI.0
B1	VSS	C7	VDD	F13	CFI.0	J13	PFI.4	M5	PPIXO.3	N9	RPIXI.3
B2	VDD	C8	QUANTI.1	G1	PFO.0	K1	PFO.6	M6	PPIXO.6	N10	RPIXI.5
B3	PDAT.2	C13	CFI.7	G2	VDD	K2	PFO.7	M7	PPIXO.8	N11	RPIXI.7
B4	QSYNC	D1	PDAT.6	G3	VSS	K12	PFI.1	M8	RPIXI.1	N12	RPIXI.8

Note: Pins A12, N1 and N13 are no connects.

Packaging

100-Pin Plastic Pin Grid Array: See NG Package in Package Selector Guide
100-Pin Ceramic Pin Grid Array: See FG Package in Package Selector Guide
100-Pin Plastic Quad Flat Pack: See PB Package in Package Selector Guide

Ordering Information