L64260/L64261 High-Speed Versatile FIR Filter (VFIR)

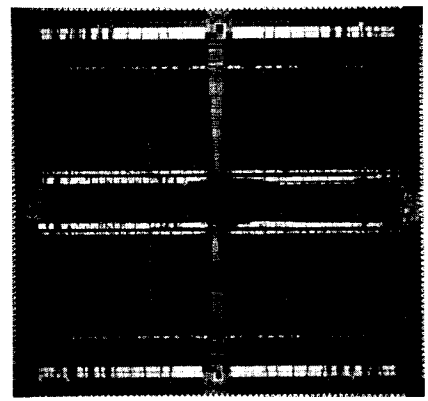
LSI LOGIC

Description

The L64260/61 compute inner products in many different forms. FIR filters to perform decimation, interpolation, adaptive filtering and 2D filtering can be implemented. In addition, matrix-matrix and matrix-vector multiplication can both be performed. Each processor contains four high-speed MACs each with four data and four coefficient registers. An on-chip sequencer is used to control the chip when repetitive operations are performed.

There are two versions of the processor. The L64260 comes in a 223-pin Ceramic Pin Grid Array with eight 16-bit data inputs bonded out.

The L64261 comes in a 144-pin Ceramic Pin Grid Array that does not provide the use of all I/O pins. The L64261 has two 16-bit data inputs, three 12-bit data inputs and three 12-bit data inputs that are shared with the buses needed to cascade parts. In applications not requiring both the additional data input buses and the ability to cascade parts, the L64261 can be used. The L64260 is useful in applications in which either very high I/O bandwidth is required (e.g., general inner products) or the extra data precision is needed. The L64261 is aimed primarily at filtering and matrix multiplication applications. In these applications, not all of the data input buses are necessary.



L64260 Chip

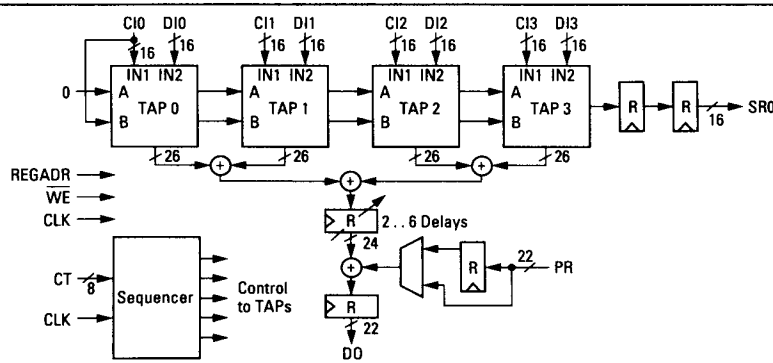
Features

- Four 16-bit MACs
- On-chip control functions reduce system size
- Multiple chips can be used to increase performance
- Flexible architecture with 16 coefficient and data registers
- High I/O bandwidth for:
  - Adaptive filtering
  - Matrix-matrix or matrix-vector multiplication
  - General inner products
- Variable input and output data rates for decimation and interpolation
- Can perform one-chip 4 x 4 convolution
- High data rates

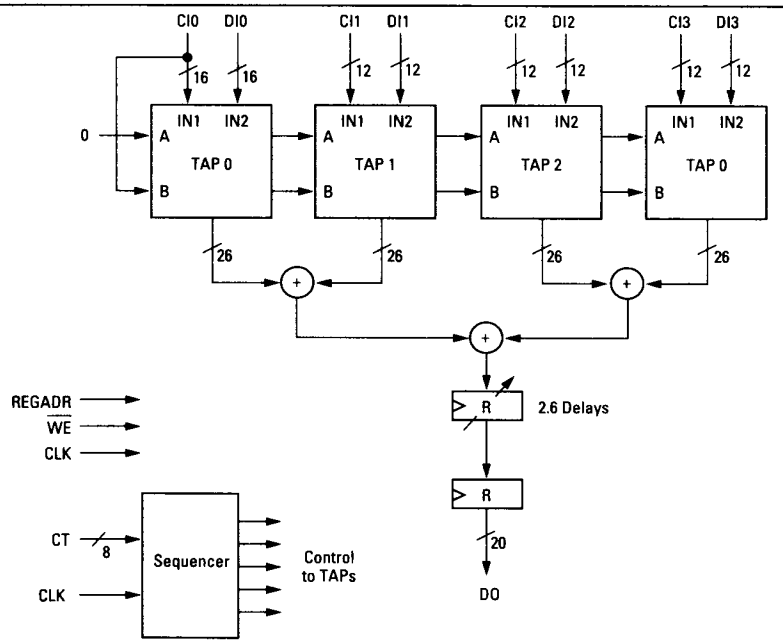
Commercial	Military
40 MHz	30 MHz
30 MHz	25 MHz

- Available in 223-pin CPGA (Ceramic Pin Grid Array) (L64260) and 144-pin CPGA (Ceramic Pin Grid Array) (L64261) packages

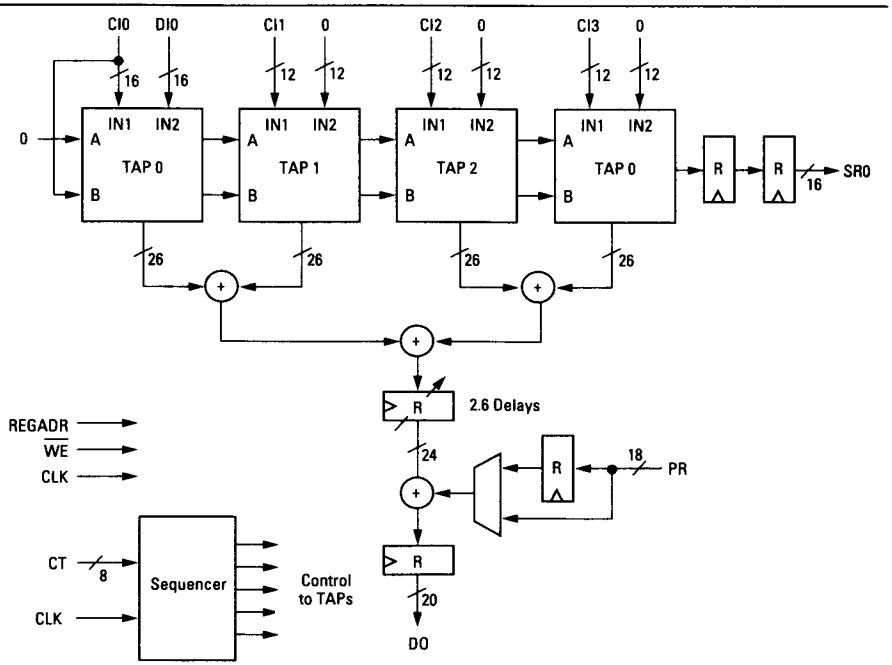
L64260 Block Diagram



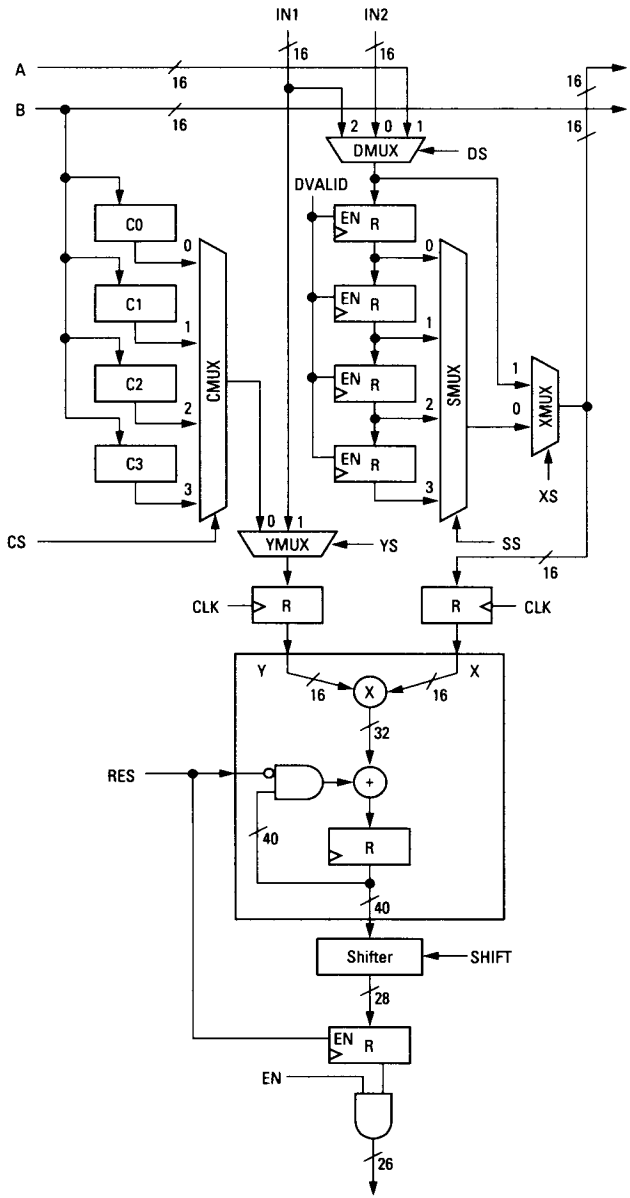
L64261 Block Diagram (MP LOW)



L64261 Block Diagram (MP HIGH)



TAP Block Diagram (L64260/L64261)



L64260 Pin Listing and Description

DI0
16-bit TAP 0 data input.

DI1
16-bit TAP 1 data input.

DI2
16-bit TAP 2 data input.

DI3
16-bit TAP 3 data input.

CI0
16-bit TAP 0 coefficient/data input. Also used during processor initialization to load any fixed coefficients.

CI1
16-bit TAP 1 coefficient/data input.

CI2
16-bit TAP 2 coefficient/data input.

CI3/CT
16-bit TAP 3 coefficient/data input. Data to be loaded into the internal control registers is also placed on the CI3 bus during initialization. For systems utilizing all of the eight counter control bits, the CI3 bus is not used for data or coefficients but for the two most significant bits of the count instead.

SR0
16-bit shift register output. Used in multiprocessor systems operating on 1 D data to pass the delayed input data to the next processor in the system.

PR
22-bit partial result input. Used in multiprocessor systems to accept the output of another processor to sum with the output of the current processor.

D0
22-bit filter data output. The sum of the result from the current processor and the data on the partial result bus.

CLK
System clock. Controls the positive edge triggered data latches and pipeline registers. The filter state registers only latch data when CLK goes from LOW to HIGH and the internal signal DVALID is HIGH.

$\overline{WE}$
Write enable for internal control and coefficient latches. When LOW, the data on the CI3 bus will be latched into the control register specified by the address on the REGADR.0– REGADR.4 pins when REGADR.5 is LOW. If REGADR.5 is HIGH, the coefficient data on the CI0 bus is loaded into the coefficient latch specified by the REGADR.0– REGADR.4 pins.

REGADR/CT
Register address of internal coefficients and control signals during processor initialization. REGADR.5 HIGH indicates that a coefficient on the CI0 is to be loaded. When REGADR.5 is LOW, a control word on the CI3 bus will be loaded. After initialization this bus is used for the controller count input.

L64260 Pin Description Summary

Pin	No. of Pins	I/O	Description
DI0.0–DI0.15	16	I	TAP 0 data input
DI1.0–DI1.15	16	I	TAP 1 data input
DI2.0–DI2.15	16	I	TAP 2 data input
DI3.0–DI3.15	16	I	TAP 3 data input
CI0.0–CI0.15	16	I	TAP 0 coefficient input
CI1.0–CI1.15	16	I	TAP 1 coefficient input
CI2.0–CI2.15	16	I	TAP 2 coefficient input
CI3.0–CI3.15 CT.6–CT.7	16	I I I	TAP 3 coefficient input shared with data to be loaded into configuration registers and program count input
SR.0–SR0.15	16	O	Shift register output
PR.0–PR.21	22	I	Partial result input
DO.0–DO.21	22	O	Filter output
CLK	1	I	System clock Clock registers at LOW to HIGH transition
$\overline{WE}$	1	I	Write enable for internal configuration registers active LOW
REGADR.0–REGADR.5 CT.0–CT.5	6	I	Internal configuration/coefficient register address program count input

Note: X.0 is always the LSB of bus X

L64261 Pin Listing Description

DI0
16-bit TAP 0 data input.

DI1/PR
12-bit TAP 1 data input shared with 10 partial result input pins. For single processor systems (MP LOW), the partial result inputs are not used and this bus can be used as an additional 12-bit data bus for TAP 1. In a multiprocessor system (MP HIGH), this bus is used to accept the output of another processor in the system to be summed with the result from the current processor.

DI2/PR (8), SR0 (4)
12-bit TAP 2 data input shared with 4-bits of the SR0 (shift register output) and 8-bits of the PR bus. For single processor systems (MP LOW), this bus can be used as an additional 12-bit data bus for TAP 2. In multiprocessor systems (MP HIGH), 8-bits of this bus are used to form the rest of the 20-bit PR bus and 4-bits of the SR0 bus. The SR0 bus is used to pass the delayed data input to another processor in a 1D processing system.

DI3/SR0 (12)
12-bit TAP 3 data input shared with the other 12-bits of the SR0 bus. This bus is used as an additional 12-bit data input bus for TAP 3 when MP is LOW and as 12-bits of the delayed input bus when MP is HIGH.

CI0
16-bit TAP 0 coefficient/data input. Also used during initialization to load any fixed coefficients.

CI1
12-bit TAP 1 coefficient/data input.

CI2
12-bit TAP 2 coefficient/data input.

C13/CT(2)
12-bit TAP 3 coefficient/data input. Data to be loaded into the internal control registers is also placed on the CI3 bus during initialization. For systems utilizing all of the eight counter control bits, the CI3 bus is not used for data or coefficients but for the two most significant bits of the count instead.

DO
20-bit filter data output. The sum of the result from the current processor and the data on the partial result bus.

CLK
System clock. Controls the positive edge triggered data latches and pipeline registers. The filter state registers only latch data when CLK goes from LOW to HIGH and the internal signal DVALID is HIGH.

$\overline{WE}$
Write enable for internal control and coefficient latches. When LOW, the data on the CI3 bus will be latched into the control register specified by the address on the REGADR.0–REGADR.4 pins when REGADR.5 is LOW. If REGADR.5 is HIGH, the coefficient data on the CI0 bus is loaded into the coefficient latch specified by the REGADR.0–REGADR.4 pins.

REGADR/CT
Register address of internal coefficients and control signals for use during processor initialization. REGADR.5 HIGH indicates that a coefficient on the CI0 bus is to be loaded. When REGADR.5 is LOW, a control word on the CI3 bus will be loaded. After initialization this bus is used for the controller count input.

MP
Multiprocessor mode pin. When HIGH, the device will operate in the multiprocessor mode. In this mode, the DI1, D12 and DI3 buses are unavailable. The SR0 and PR buses can be used instead. When MP is LOW, SR0 and PR are unavailable, but DI1, DI2 and DI3 are available.

L64261 Pin Description Summary

Pin	No. of Pins	I/O	Description
DI0.0–DI0.15	16	I	TAP 0 data input
DI1.4–DI1.15 PR.12–PR.21	12	I I	TAP 1 data input shared with: 10 partial result bits
DI2.4–DI2.15 PR.4–PR.11 SR0.0–SR0.3	12	I I O	TAP 2 data input shared with: 8 bits of partial result 4 bits of shift register output
DI3.4–DI3.15 SR0.4–SR0.15	12	I O	TAP 3 data input shared with: 12 bits of shift register output
CI–CI.15	16	I	TAP 0 coefficient input
CI1.4–CI1.15	12	I	TAP 1 coefficient input
CI2.4–CI2.15	12	I	TAP 2 coefficient input
CI3.4–CI3.15 CT6.–CT.7	12	I	TAP 3 coefficient input shared with data to be loaded into configuration registers and program count input
DO.0–DO.21	20	O	Filter output
CLK	1	I	System clock Clock registers at LOW to HIGH transition
$\overline{WE}$	1	I	Write enable for internal configuration registers active LOW
REGADR.0–REGADR.5 CT.0–CT.5	6	I	Internal configuration/coefficient register address program count input
MP	1	I	When HIGH sets L64261 in multiprocessor mode When LOW sets L64261 in single processor mode

Note: X.0 is always the LSB of bus X

Architecture

There are three basic architectures that the user can choose from. The L64260 has one configuration, with eight input buses of 16-bits each and the input and output buses required for multiprocessor operation. The L64261 can be electrically reconfigured between a cascadable architecture with only five input buses (two 16-bits wide, three 12-bits wide) and a non-cascadable architecture with eight input buses (two 16-bits wide, six 12-bits wide). The MSB of all 12-bit buses have the same significance as the MSB of 16-bit buses; i.e., the four LSBs have been replaced by zero. A single pin (MP) selects the desired architecture.

The only difference between these three architectures is the availability of I/O pins; the core of the circuit is the same for all three. Each contains four TAP cells, the adders to sum the results of the TAPs and a variable delay element.

The TAP Cell

To ease the requirements for off chip storage of coefficients and data values, 16 data registers and 16 coefficient latches are included on-chip. There are four of each type of register in each TAP cell. This makes it possible to implement, without external data or coefficient storage, fixed coefficient filters with up to 16 taps (with input or output rates of 10 MHz) and a 4 x 4 matrix-vector or matrix-matrix multiplication in which one of the matrices is fixed.

The inputs to the multipliers can come from several sources. The X input data is chosen from the internal state registers, the CI data pins or the DI data pins by the DMUX, XMUX and SMUX multiplexers. The Y input data can be derived from either the CI data pins or the coefficient latches by the CMUX and YMUX multiplexers. These options make it possible to perform a wide range of operations with the same basic hardware and to use the I/O pins effectively for each application. Application examples are given later to illustrate these points.

The reset signal (RES) for each TAP latches the last accumulated result in a register and resets the accumulator to zero. If the enable signal (EN) in any TAP is brought LOW, the output for that TAP is forced to zero. These two signals give the user the flexibility of summing the outputs of two or more TAPs or multiplexing the outputs.

Architecture
(Continued)

The state register shift control (DVALID), RES, EN, state register select (SS) and coefficient latch select (CS) signals are generated at the system clock rate by the sequencer. The RES and EN signals are unique for each TAP while the DVALID, CS and SS signals are the same for all four TAPs. The shift value (SHIFT) and the control signals (DS, XS, YS) for the DMUX, XMUX and YMUX are controlled statically via mode latches. DS is unique for each TAP (DS0.0, DS0.1, control the DMUX for TAP 0, and so on), but XS, YS and SHIFT are the same for all four TAPs.

The value of each multiplexer control signal that is required to select a particular input signal is shown at that input to the multiplexer in the TAP Block Diagram. For example, to select IN2 as the MAC X input, DS is set to 0 and XS is set to 1 (see TAP Block Diagram).

MAC Flexibility

The data path has been designed to give the user as much flexibility as possible in using the processor. Each MAC can compute an independent inner product or the MACs can be used as multipliers with all products being summed to produce a single inner product. The outputs of each MAC can be accessed independently by enabling them one at a time onto the common output bus. In addition, results accumulated in different MACs can be summed together. Each approach has some advantages and disadvantages. Because each MAC has a 40-bit accumulator, performing a complete inner product in a single MAC will result in minimum truncation error. For fixed coefficient filters, this is a viable approach. However, if all of the elements of the two vectors are valid during the same cycle, it may be preferable to have all of the MACs computing one part of a single result. One example of this would be a matrix-matrix multiplication in which the columns of one matrix are fed into the X inputs and the rows of the other matrix are fed into the Y inputs. For large inner products, the partial result input is used to sum the outputs from processors computing other parts of the result.

Data Formats

Throughout this data sheet, the highest numbered bit of a bus (i.e., BUS.max) has the greatest significance and the lowest numbered bit (i.e., BUS.0) has the least significance.

The MACs can operate with any combination of two's-complement and unsigned data (X input) and coefficients (Y input). The internal control bit TCD sets the MACs to operate on two's-complement data when HIGH and unsigned data when LOW. The internal control bit TCC sets the MACs to operate on two's-complement coefficients when LOW and unsigned coefficients when HIGH. The partial result input (PR) and data output (DO) are always two's-complement format.

The barrel shifter can be used to scale the results. The internal control signals (SHIFT.0–SHIFT.1) set the relative significance of the multiplier output with respect to the partial result input and the data output. PR.21 and DO.21 always have the same significance. However, the relative significance of the MSB of the 32-bit multiplier product can be adjusted with respect to the significance of the MSBs of the PR and DO (see Table 1). Note that the L64260 and L64261 are slightly different in this respect.

The primary function of the shifter is to prevent overflow when the sum of a large number of products is computed while maintaining sufficient precision when few products are summed. If each MAC is operated as a multiplier, then SHIFT.0 and SHIFT.1 can be held HIGH (L64260). With SHIFT.0 and SHIFT.1 LOW, the sum of 256 products can be computed without overflow (L64260).

Table 1. Effect of SHIFT Controls

		L64260		L64261	
SHIFT.0	SHIFT.1	Position of MSB of Multiplier Product	Max Number of Products	Position of MSB of Multiplier Product	Max Number of Products
0	0	DO.12,PR.12	256	DO.14,PR.14	64
1	0	DO.14,PR.14	64	DO.16,PR.16	16
0	1	DO.16,PR.16	16	DO.18,PR.18	4
1	1	DO.18,PR.18	4	DO.20,DO.20	1

Architecture
(Continued)

If an integer format (binary point to the right of the LSB) is used for data and coefficients, then the binary point of the multiplier is always to the right of the LSB. However, when working with fractional formats, the binary point of the multiplier product is to the left of the MSB for unsigned data and coefficients, to the right of the second most significant bit for two's-complement data and coefficients and to the right of the MSB if one of the inputs is two's-complement and the other is unsigned.

Table 2. Summary of Multiplier Output Formats for Fractional Data Inputs

Coefficient Format	Data Format	Position of Multiplier Output Binary Point
unsigned	unsigned	left of MSB
signed	unsigned	right of MSB
unsigned	signed	right of MSB
signed	signed	right of 2nd most significant bit

Example Data Formats
Consider an example utilizing the L64260 in which the data and coefficients are both two's-complement fractional numbers. If SHIFT.0 and SHIFT.1 are HIGH, PR=0 and 1.000000000000000 (-1) is multiplied by 1.000000000000000 (-1), then the result on the L64260 DO.21–DO.0 pins will be 00001.000000000000000000 (+1). The MSB of the multiplier product is at DO.18 and the binary point is to the right of DO.17. For the same multiplication with SHIFT.0 and SHIFT.1 LOW, the result on the L64260 DO.21–DO.0 pins will be: 00000000001.00000000000 (+1). All numbers in this example are with the MSB to the left.

The L64261 produces somewhat different results. Suppose SHIFT.0 and SHIFT.1 are HIGH, PR=0 and both data and coefficients are unsigned. If .1000000000000000 (0.5) is multiplied by .1000000000000000 (0.5), then the result on the L64261 DO.21–DO.2 pins will be 0.0100000000000000000 (0.25). The MSB of the multiplier product is at DO.20 and the binary point is to the left of DO.20. For the same multiplication with SHIFT.0 and SHIFT.1 LOW, the result on the L64261 DO.21–DO.2 pins will be: 0000000.0100000000000 (0.25). These examples were for 16-bit input buses (DI0 or CI0). When 12-bit fractional data values are used, the results are the same (i.e., .100000000000 times .100000000000 is 0.010000000000000000, as expected).

Data Precision
The 32-bit multiplier products must be truncated in order to generate an output of only 22 bits (or 20 bits for the L64261). The bit widths of the signals in the L64260/L64261 are shown in the block diagrams. Whenever a bus width is reduced, the LSBs are simply truncated.

Latency
The latency (delay from input to output in cycles) depends on the actual configuration of the chip and the setting of the variable delay element. If the state registers are used and the variable delay is set to two, then the total latency is seven cycles: the first state reg, the MAC X input reg, the MAC ACC, the shifter output reg, two in the variable delay element and the output reg. The minimum latency is six cycles when the state registers are bypassed.

Architecture
(Continued)

Cascading Multiple Chips

The SRO output and the PR input are provided for cascading multiple chips to create filters with larger windows. The SRO output can be connected to the DI input of another chip in a 1D system to effectively increase the shift register and hence the filter window length. The PR bus is used to sum the output from another chip in the system. The PR input path is pipelined if the internal control signal ENREG is HIGH and is unpipelined when ENREG is LOW. For systems with high data rates it is necessary to pipeline the PR input path.

The variable delay element before the partial result adder is used to cancel the pipeline delays in the partial result path. For 1D filters, the two delays at the SRO output cancel both the PR input pipeline register and the output register delays. Hence, filters of arbitrary window length can be constructed without external components. For 2D filters, the SRO output is not used and the variable output delay must be used instead. It can cancel the delays accumulated in a five chip system (if PR pipeline register is bypassed) or a three chip system (if the PR pipeline register is enabled).

The two registers at the SRO pins effectively delay the inputs to the next processor in a cascaded 1D filter system by two cycles. Care should be taken to ensure that CT is similarly delayed.

The number of delays provided by the variable delay element is determined by the internal control signal, DEL.0–DEL.2 as shown in Table 3.

Table 3. Effect DEL.0–DEL.2 Controls

DEL.0	DEL.1	DEL.2	Number Delays
0	0	0	2
1	0	0	3
0	1	0	4
1	1	0	5
0	0	1	6
1	0	1	UNDEF
0	1	1	UNDEF
1	1	1	UNDEF

Architecture
(Continued)

Loading the Control Parameters and Coefficients

Before normal filter operation can commence, all of the filter coefficients (if they are to be stored in the internal coefficient storage) and operating parameters must be loaded into the processor. The pins, REGADR.0–REGADR.5 specify which coefficient or control register is being loaded. When $\overline{WE}$ is pulled LOW data is latched. Coefficient data is loaded on the CI0 bus and control parameters are loaded on the CI3 bus. The way in which the coefficient, control and mode latches are addressed is shown in Tables 4, 5 and 6.

When coefficients or control parameters are being loaded into the processor, the output (DO) will be undefined for a number of cycles not greater than the sequencer period +40 cycles. The SRO output will be undefined for a period of less than 20 cycles in which DVALID is true.

Table 4. Addressing for Control Latches

REGADR	CI3
0	$\overline{\text{DVALIDM}}$ – DVALID $\overline{\text{MASK}}$
1	$\overline{\text{DVALIDI}}$ – DVALID $\overline{\text{INVERT}}$
2	$\overline{\text{EN0M}}$ – TAP 0, EN $\overline{\text{MASK}}$
3	$\overline{\text{EN0I}}$ – TAP 0, EN $\overline{\text{INVERT}}$
4	$\overline{\text{EN1M}}$ – TAP 1, EN $\overline{\text{MASK}}$
5	$\overline{\text{EN1I}}$ – TAP 1, $\overline{\text{INVERT}}$
6	$\overline{\text{EN2M}}$ – TAP 2, EN $\overline{\text{MASK}}$
7	$\overline{\text{EN2I}}$ – TAP 2, EN $\overline{\text{INVERT}}$
8	$\overline{\text{EN3M}}$ – TAP 3, EN $\overline{\text{MASK}}$
9	$\overline{\text{EN3I}}$ – TAP 3, EN $\overline{\text{INVERT}}$
10	$\overline{\text{RES0M}}$ – TAP 0, RES $\overline{\text{MASK}}$
11	$\overline{\text{RES0I}}$ – TAP 0, RES $\overline{\text{INVERT}}$
12	$\overline{\text{RES1M}}$ – TAP 1, RES $\overline{\text{MASK}}$
13	$\overline{\text{RES1I}}$ – TAP 1, RES $\overline{\text{INVERT}}$
14	$\overline{\text{RES2M}}$ – TAP 2, RES $\overline{\text{MASK}}$
15	$\overline{\text{RES2I}}$ – TAP 2, RES $\overline{\text{INVERT}}$
16	$\overline{\text{RES3M}}$ – TAP 3, RES $\overline{\text{MASK}}$
17	$\overline{\text{RES3I}}$ – TAP 3, RES $\overline{\text{INVERT}}$

For $0 \leq$ REGADR ≤ 17, the seventh bit (MSB) of each control word is loaded on the CI3.15 pin and the LSB is loaded on the CI3.8 pin.

Table 5. Addressing for Mode Latches

REGADR	CI3.15	CI3.14	CI3.13	CI3.12	CI3.11	CI3.10	CI3.9	CI3.8
18	DS3.1	DS3.0	DS2.1	DS2.0	DS1.1	DS1.0	DS0.1	DS0.0
19	$\overline{\text{CSM.1}}$	$\overline{\text{CSM.0}}$	$\overline{\text{SSM.1}}$	$\overline{\text{SSM.0}}$	SSI.1	SSI.0	XS	YS
20	TCD	$\overline{\text{TCC}}$	SHIFT.1	SHIFT.0	DEL.2	DEL.1	DEL.0	ENREG

Architecture
(Continued)

Table 6. Addressing for Coefficient Latches

REGADR	CI0.0–CI0.15
32	TAP 0 C0
33	TAP 0 C1
34	TAP 0 C2
35	TAP 0 C3
36	TAP 1 C0
37	TAP 1 C1
38	TAP 1 C2
39	TAP 1 C3
40	TAP 2 C0
41	TAP 2 C1
42	TAP 2 C2
43	TAP 2 C3
44	TAP 3 C0
45	TAP 3 C1
46	TAP 3 C2
47	TAP 3 C3

The Sequencer

Some decoding hardware is included to make it possible to program the processor to perform many repetitive operations including all of those listed in the Applications section. The only off chip hardware required is a single counter (applied via the CT pins). The counter was left external to the processor to give the user more flexibility in the sequencing of operations and the synchronization of several processor chips. The repetition rate of the program can be adjusted by adjusting the modulus of the counter. In addition, the RES, EN, CS and SS signals for each multiplier can be programmed as a function of the control counter (the type of function supported is a single minterm). The RES and EN signals can be separately programmed for each multiplier. The CS and SS signals are the same for all four multipliers. The clocking of the data registers is controlled by the sequencer which makes operation with different system and data clock rates straightforward.

There are three different types of circuits in the sequencer. There is one which generates SS, one which generates CS and one which generates the four RES, four EN signals and DVALID. Note that the mask and invert signals are different for each control signal and are loaded by the user and stored in latches in the processor. Also note that the SS and CS circuits are less general than the others and only consider the low two bits of the count value.

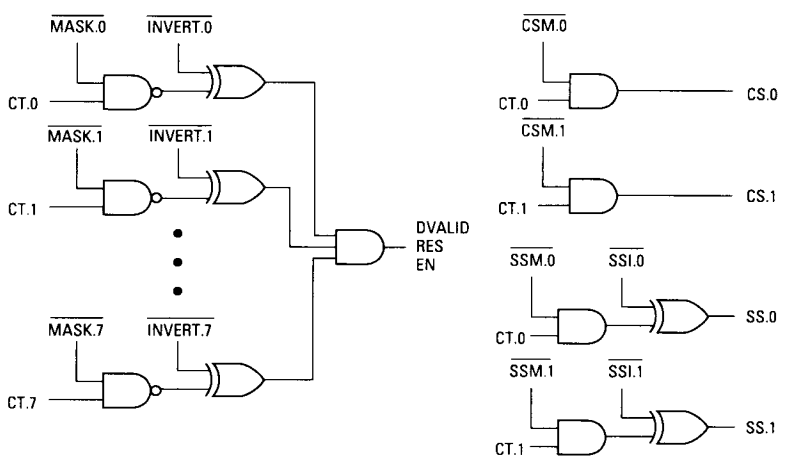


Figure 1. The Sequencer

Architecture (Continued)

Programming the Sequencer

The sequencer has been designed to be easily programmed. There are no real instructions; the user simply specifies which minterm of CT will cause each internal control signal to be valid. This is done by latching the MASK and INVERT signals for each control output. The user then supplies the appropriate CT values (normally from a counter) to manipulate the control signals.

To cancel the internal data path pipeline stages as effectively as possible, the control signals are similarly pipelined. DVALID has one delay from the CT pins, CS and SS are delayed two cycles, RES is delayed three cycles and EN is delayed four cycles. For filtering operations, this delay is inconsequential. However, for matrix operations in which the data has a definite beginning and end, the delay must be accounted for. When using the internal state or coefficient registers when computing matrix operations, the count value input on the CT bus should be advanced by one cycle. If the internal state registers are bypassed during matrix operations, the count value should be advanced by two cycles relative to the data inputs.

The values of the control signals needed to perform many common applications are given in the next section. Programming the processor for these cases is really quite simple; all four TAPs have identical RES and EN (EN is always true) signals and, at most, a two-bit counter is required. For filters with large differences in system and data clock rates, the control of the processor is more complex.

Application Examples

To illustrate the versatility and power of the processor, several applications are shown in the following sections. Table 7 is a list of some possible operations which can be performed with one or more processors. All of the data rates listed in the table are for an L64260A or L64261A operating at a 40 MHz clock rate. For processors operating at lower clock rates, the data rates should be scaled accordingly.

Table 7. Partial List of Possible Operations (N=Number of Chips)

Operation	fINPUT	fOUTPUT	Window Length	On Chip Coeff/Data Storage	DVALID M/I	RES M/I	SS M/I	CS M
1D Filter	40	40	4N	Y/Y	0/0	0/0	0/0	0
Fixed	40	20	8N	Y/Y	0/0	1/0	0/1	1
Coeff	40	10	16N	Y/Y	0/0	3/0	0/3	3
	20	20	8N	Y/Y	1/0	1/0	1/0	1
	10	10	16N	Y/Y	3/0	3/0	3/0	3
	20	40	8N	Y/Y	1/0	0/0	0/0	1
	10	40	16N	Y/Y	3/0	0/0	0/0	3
	40	f < 10	$\frac{160N}{f}$	N/NA				
2D Filter	40	40	4N x 1 . . 1 x 4N	Y/Y	0/0	0/0	0/0	0
Fixed	40	20	4N x 2 . . 1 x 8N	Y/Y	0/0	1/0	0/1	1
Coeff	40	10	4N x 4 . . 1 x 16N	Y/Y	0/0	3/0	0/3	3
	20	20	4N x 2 . . 1 x 8N	Y/Y	1/0	1/0	1/0	1
	10	10	4N x 4 . . 1 x 16N	Y/Y	3/0	3/0	3/0	3
	40	f < 10	$4N \times \frac{40}{f}$ . . $1 \times \frac{160N}{f}$	N/N				
1D Filter	40	40	4N	N/Y	0/0	0/0	0/0	NA
Adaptive	40	20	8N	N/Y	0/0	1/0	0/1	NA
Coeff	40	10	16N	N/Y	0/0	3/0	0/3	NA
	20	20	8N	N/Y	1/0	1/0	1/0	NA
	10	10	16N	N/Y	3/0	3/0	3/0	NA
	40	f < 10		N/NA				

Operation	Matrix Size	Cycles
Matrix-Vector Mult	K x L	$\frac{KL}{4N}$
Matrix-Matrix Mult	K x L	$K^2 \frac{L}{4N}$
Operation	**Vector Size**	**Cycles**
Inner Product	K	$\frac{K}{4N}$

Application Examples (Continued)

Decimation Filter

For filtering requirements with large decimation rates

$$(D = \frac{fIN}{fOUT} > 4),$$

Figure 2 is used. In this configuration, there are four coefficient inputs connected to CI0–CI3 and a single data input connected to DI0. The decimation ratio,

$$D = \frac{L}{4N},$$

where L is the length of the filter impulse response and N is the number of chips used. The maximum data output rate is

$$\frac{40\ MHz}{D}$$

The coefficients are supplied from an offchip RAM or ROM. The offchip counter counts from 0 to L–1 and the sequencer is programmed to reset each of the MACs every L cycles with an offset of D cycles from each other. It is also possible to configure the processor as 4N independent filters (different input data but the same impulse response) each with an impulse response length and decimation ratio of L.

For this application, the L64260 can support 16-bit data and coefficients with cascaded processors. The L64261 can support 16-bit data but only 12-bit coefficients with cascaded processors.

All control values for this application are given in Table 8 in which L = 64 and D = 16. A 6-bit counter output is connected to CT. It can be seen that DVALID is always true (latching data at a 40 MHz rate). Each MAC is reset 17 cycles from the adjacent MAC. Normally, for a decimation ratio of 16, each MAC would be reset 16 cycles after the adjacent MAC. However, to maintain a 40 MHz input data rate, the input data is passed through the data shift register, causing an extra delay of one cycle in the data of each TAP with respect to the data of the preceding TAP. Each TAP output is enabled for non-overlapping periods of 16 of the 64 cycles so that they are effectively multiplexed over the output bus, DO.

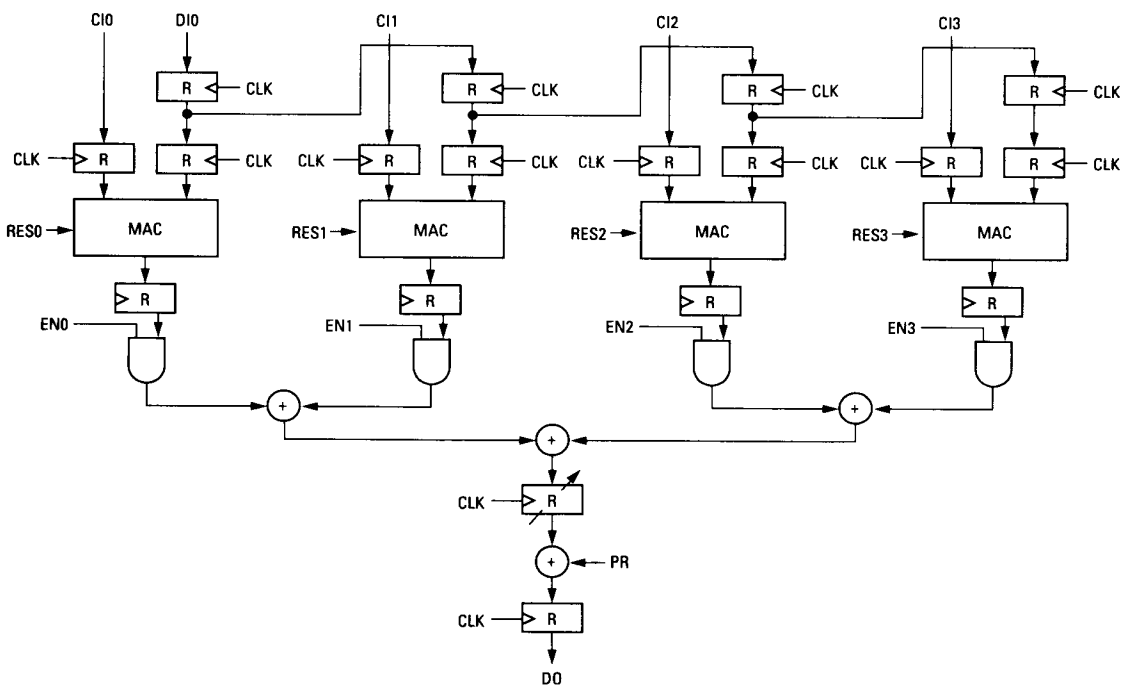


Figure 2. Decimination Filter

Application Examples (Continued)

Table 8. Configuration Data for Decimation Filter with a Decimation Ratio of 16

Address	Function	Bit 7-Bit 0	DEC
0	DVALIDM	00000000	0
1	DVALIDI	00000000	0
2	ENOM	00110000	48
3	ENOI	00010000	16
4	EN1M	00110000	48
5	EN1I	00100000	32
6	EN2M	00110000	48
7	EN2I	00110000	48
8	EN3M	00110000	48
9	EN3I	00000000	0
10	RESOM	00111111	63
11	RESOI	00000000	0
12	RES1M	00111111	63
13	RES1I	00010001	17
14	RES2M	00111111	63
15	RES2I	00100010	34
16	RES3M	00111111	63
17	RES3I	00110011	51
18	DMUX	01010100	84
19	MUX	00000001	1
20	MISC	00000000	0

TAP 0: DI bus is selected as data input.
TAP 1: Cascade bus (TAP A bus) is selected as data input.
TAP 2: Cascade bus (TAP A bus) is selected as data input.
TAP 3: Cascade bus (TAP A bus) is selected as data input.
State registers are selected in each TAP as data input (X) of the MAC.
CI bus is selected in each TAP as coefficient input (Y) of the MAC.
SHIFT is set to set the significance of the MSB of each multiplication to be the same as DO.12.
Data (MAC X input) is unsigned and coefficients (MAC Y input) are signed.
The variable delay is set to be two.
The partial result bypasses the input register.

16-TAP 10 MHz Fixed Coefficient Filter

Figure 3 is used to implement 16-TAP 10 MHz (input and output sample rates) fixed-coefficient filter. In this case, there is a single data input connected to DI0 and a single coefficient input connected to CI0 that is used to load the coefficient into on chip storage latches. Each MAC performs four multiplications per sample. The leftmost MAC computes the first four TAPs of the filter and so on. To increase the filter impulse response length, multiple processors can be connected in a cascade configuration. The cascade and data outputs are connected to the data and partial result inputs of adjacent processors in a cascaded system. If the partial-result input pipeline-register is enabled, filters of unlimited length can be implemented without use of the variable delay element.

To implement a 20 MHz or 40 MHz filter (input and output rates), the number of data registers accessed by each MAC can be reduced to 2 or 1, respectively. Of course, the impulse response length drops to 8 TAPs with 20 MHz sample rates and 4 TAPs with 40 MHz sample rates. This is simply a matter of reconfiguring the chip and reprogramming the sequencer.

It is also possible to configure the processor to perform decimation filtering with a 40 MHz input sample rate and 20 MHz (8-TAP filter) or 10 MHz (16-TAP filter) output sample rates without using off-chip storage (as shown in the previous example). For these cases, the sequencer is simply reprogrammed.

For this application, both the L64260 and L64261 support 16-bit data and coefficients with cascadability. Both are fully cascadable.

Application Examples
(Continued)

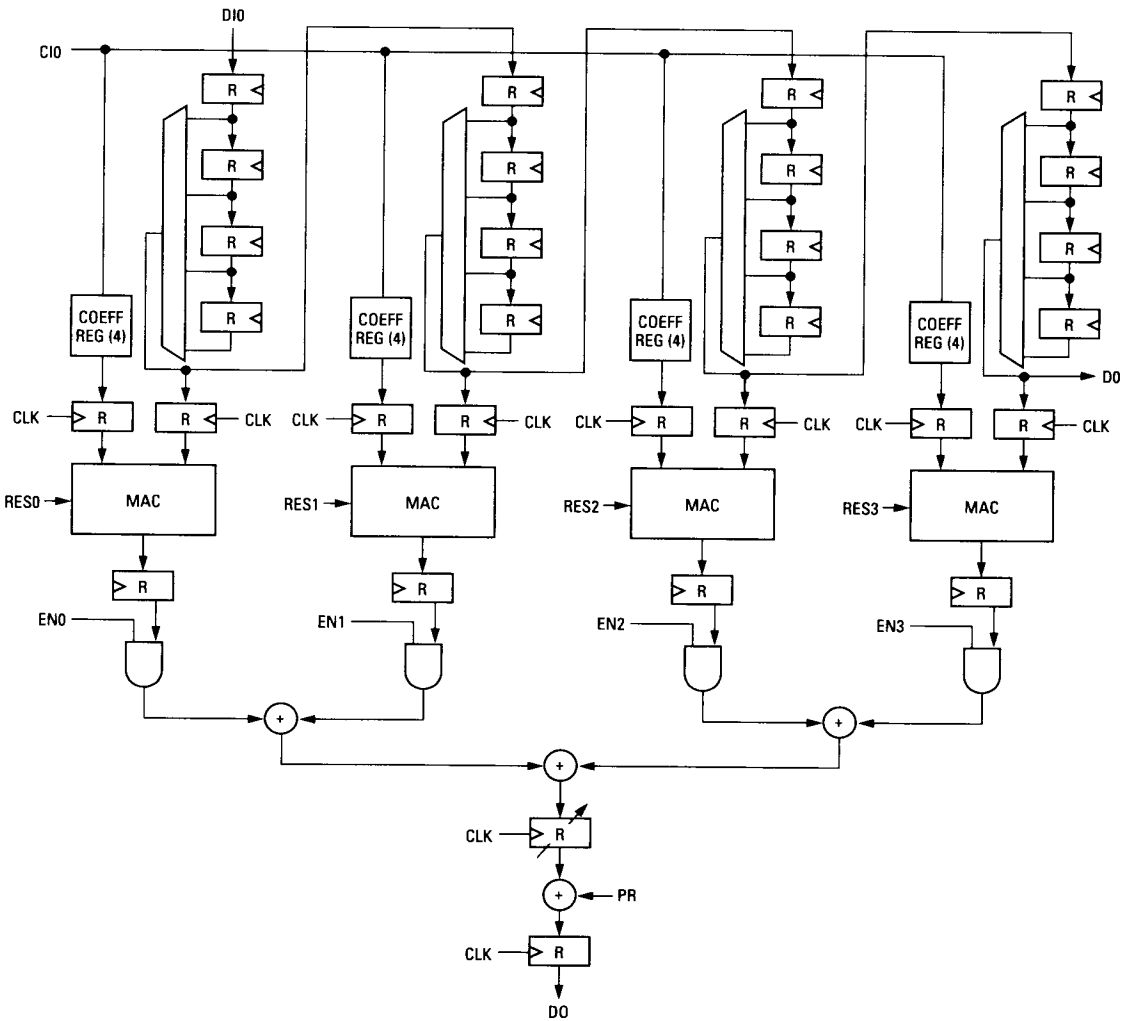


Figure 3. 16-Tap 10 MHz Fixed Coefficient Filter

Application Examples (Continued)

4 x 4 10 MHz Fixed Coefficient Filter

If the shift register chain shown in the previous example is broken and data from different lines of the input signal are inserted at the breaks, 2-dimensional filtering can be accomplished. One case is shown in Figure 4. Here the 16 TAPs are organized into a 4 x 4 configuration to perform a 10 MHz input/output rate filter. Similar to the previous example, it is possible to reduce the number of TAPs as the sample rates increase.

As with the decimation example shown, the L64260 supports full 16-bit data and coefficients while the L64261 can only support 12-bit data and 16-bit coefficients.

The control words required to implement this function are shown in Table 9. A 2-bit counter is connected to CT. In this case, DVALID is true only every fourth cycle when CT = 0. The RES signal for all MACs is also true every fourth cycle. All MACs are always enabled and all four MAC outputs are summed to produce a single output.

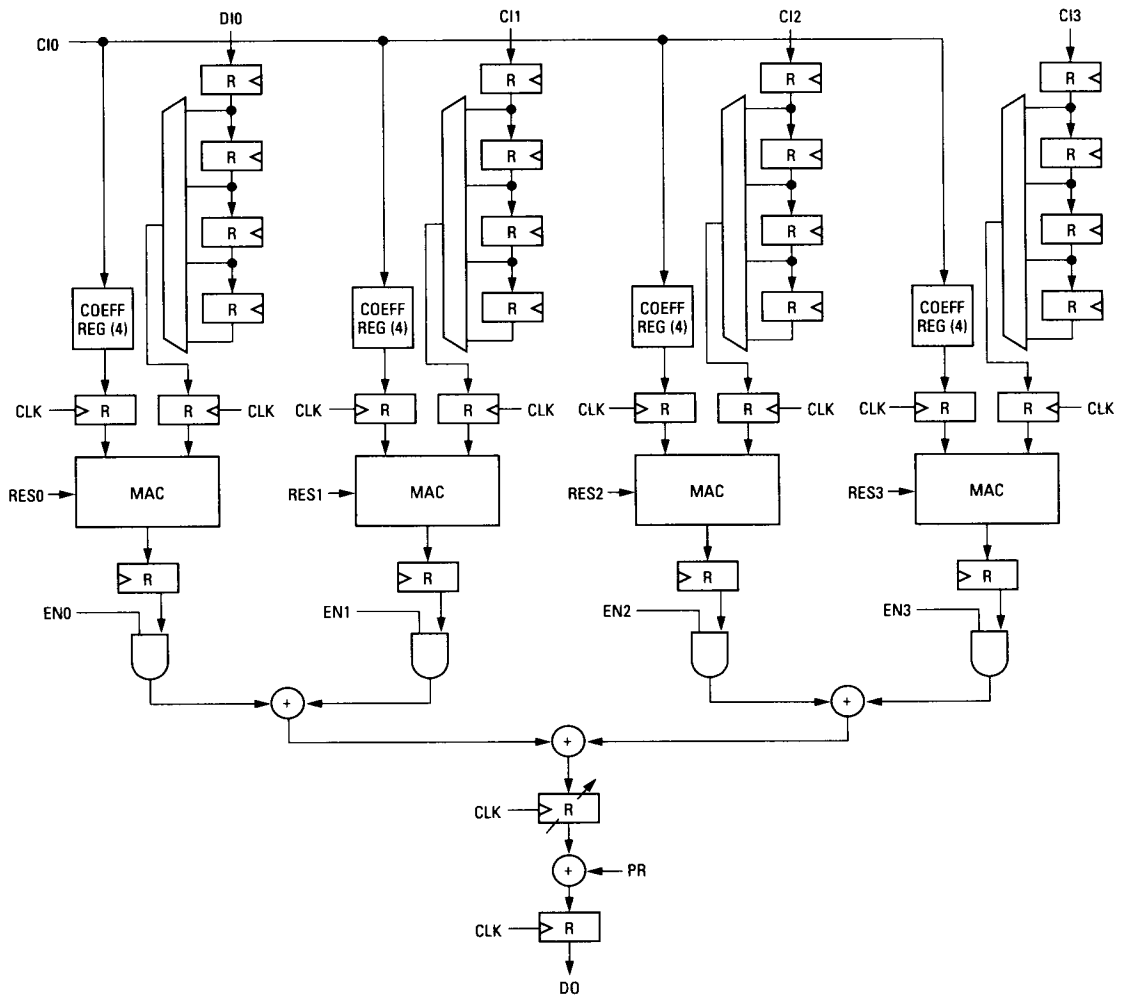


Figure 4. 4 x 4 10 MHz Fixed Coefficient Filter

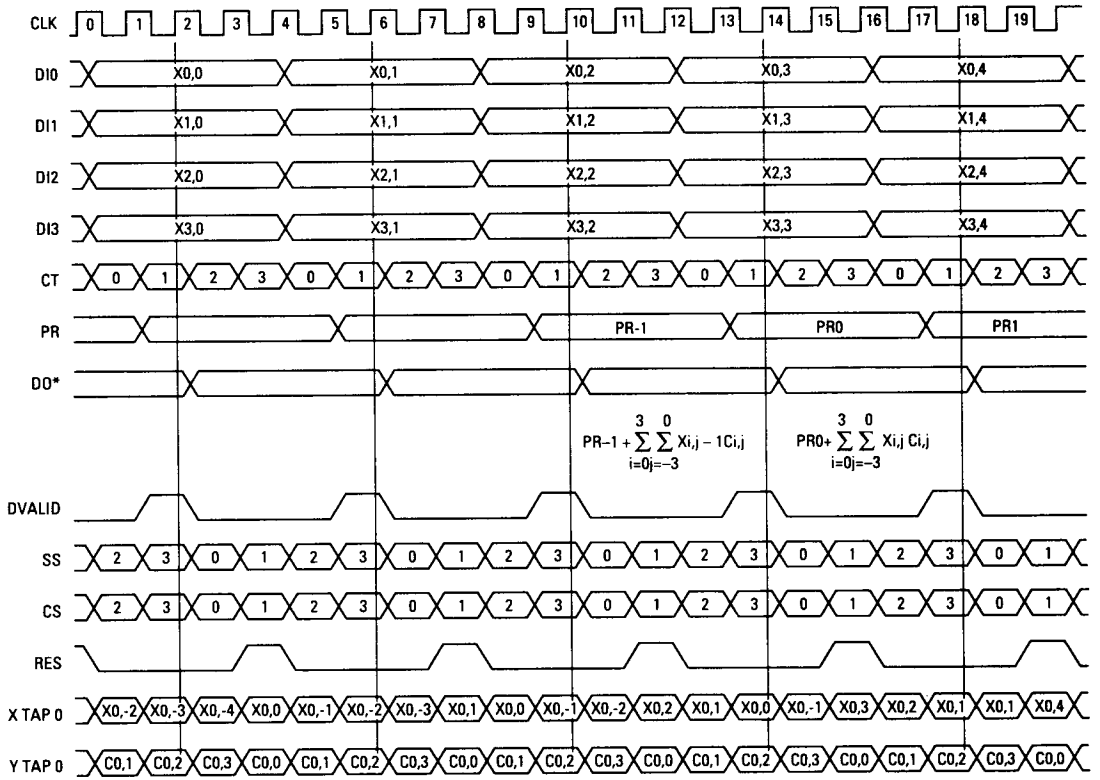
Application Examples
(Continued)

Table 9. Configuration Data for 10 MHz Fixed Coefficient 2-D Filter

Address	Function	Bit 7-Bit 0	DEC
0	DVALIDM	00000011	3
1	DVALIDI	00000000	0
2	ENOM	00000000	0
3	ENOI	00000000	0
4	EN1M	00000000	0
5	EN1I	00000000	0
6	EN2M	00000000	0
7	EN2I	00000000	0
8	EN3M	00000000	0
9	EN3I	00000000	0
10	RESOM	00000011	3
11	RESOI	00000000	0
12	RES1M	00000011	3
13	RES1I	00000000	0
14	RES2M	00000011	3
15	RES2I	00000000	0
16	RES3M	00000011	3
17	RES3I	00000000	0
18	DMUX	10101000	168
19	MUX	11110000	240
20	MISC	11110110	246

Tap 0: DI bus is selected as data input.
Tap 1: CI bus is selected as data input.
Tap 2: CI bus is selected as data input.
Tap 3: CI bus is selected as data input.
State registers are selected in each TAP as data input of the MAC.
Coefficient registers are selected in each TAP as Y input of the MAC.
Data (MAC X input) is signed and coefficients (MAC Y input) are unsigned.
SHIFT is set to set the significance of the MSB of each multiplication to be the same as DO.18.
The variable delay is set to be five.
The partial result bypasses the input register.
The I/O signal waveforms for this application are shown in Figure 5. Note that the only 40 MHz signals required are the CLK and CT signals and that the input data is latched at the vertical dashed lines. Some internal signals are shown at the bottom of the diagram to illustrate the detailed internal operation.

Application Examples
(Continued)



*The variable delay is set to five.

Figure 5. I/O and Selected Internal Signal Waveforms for the 4 X 4 10 MHz Filter

Application Examples (Continued)

16-TAP 10 MHz Adaptive Coefficient Filter

For applications requiring the coefficients to change at the same rate as the input data, Figure 6 is used. Instead of fetching the coefficients from the on-chip register files, the coefficients are brought in on the four coefficient buses connected to CI0–CI3. Otherwise the operation in this configuration is very similar to that for fixed coefficient 1D filters.

The L64260 supports full 16-bit data and coefficients while the L64261 can only support 16-bit data and 12-bit coefficients. Both versions are fully cascadable.

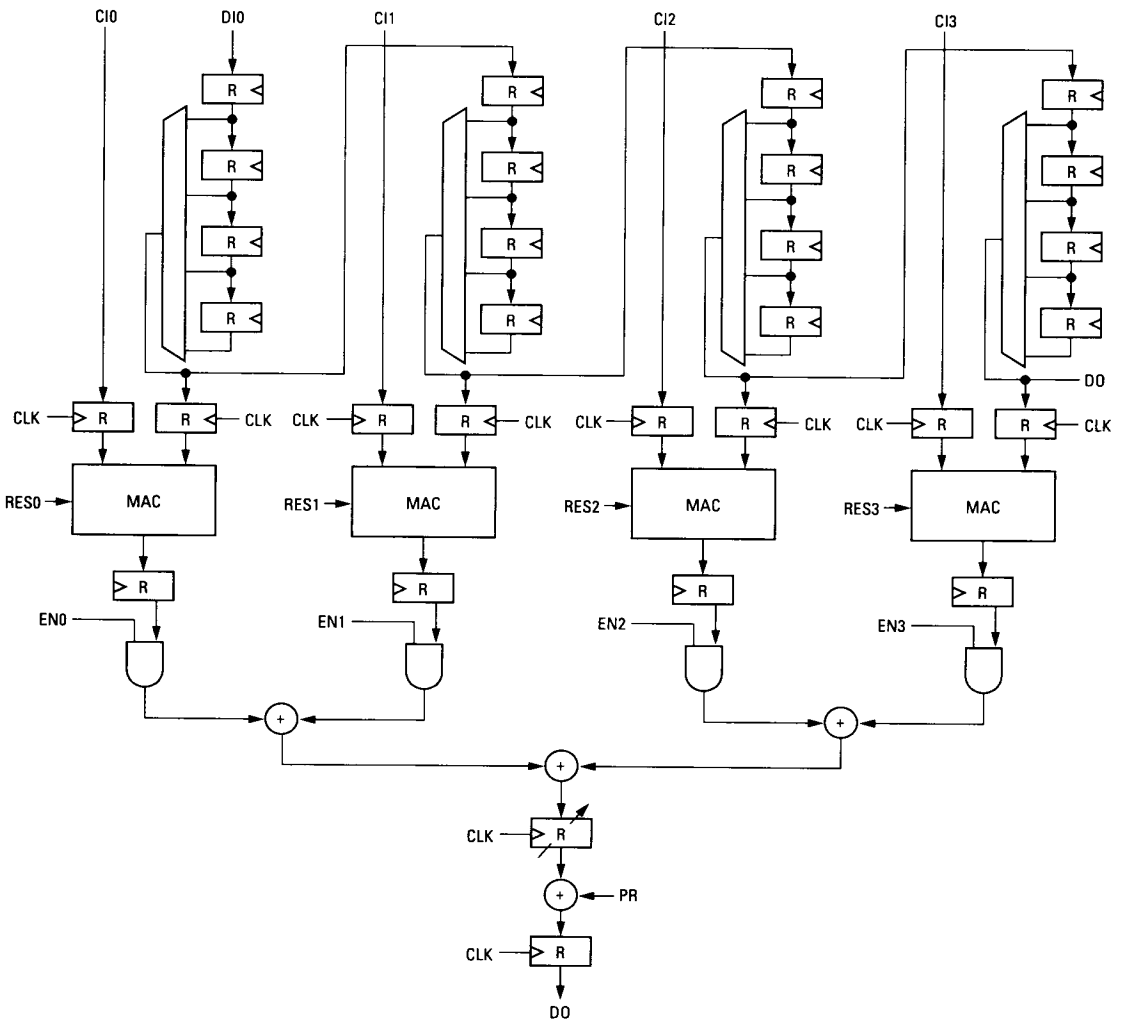


Figure 6. 16-TAP 10 MHz Adaptive Coefficient Filter

Application Examples
(Continued)

Inner Product Processor

To compute arbitrary inner products in which both multiplier inputs must change every cycle, Figure 7 is used. The length of the inner product can be expanded by connecting the outputs of each chip to the partial result of the next chip in the chain.

In this case, the L64260 supports 16-bit data and is fully cascadable. The L64261 is not cascadable and only 12-bit is supported.

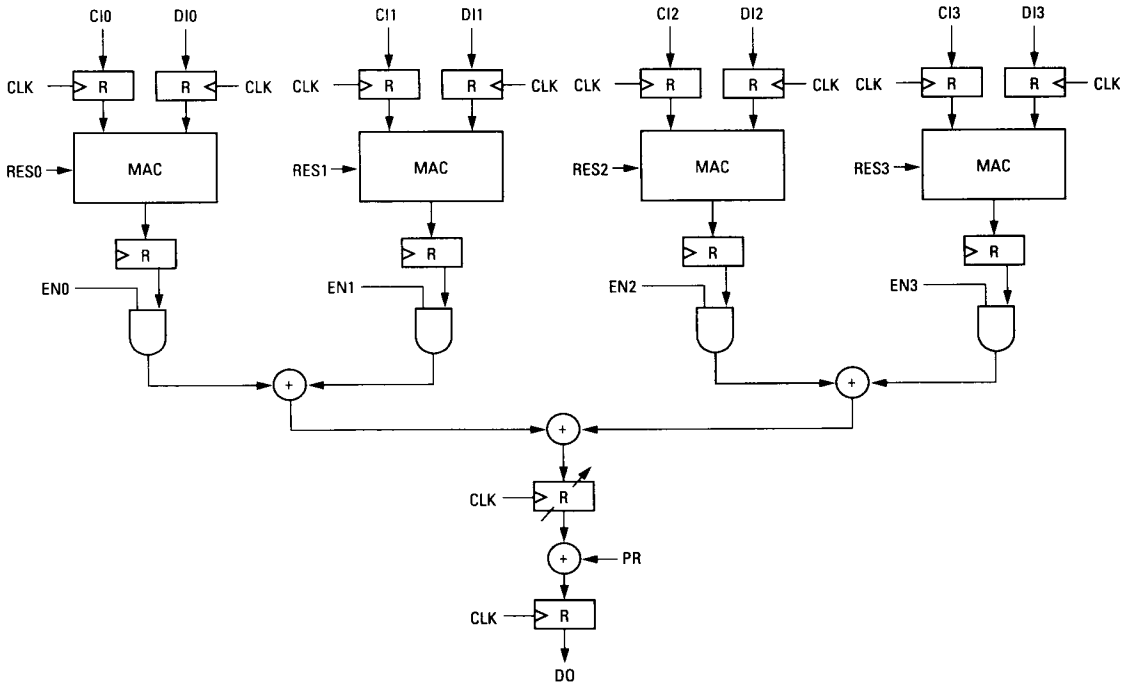


Figure 7. Inner Product Processor

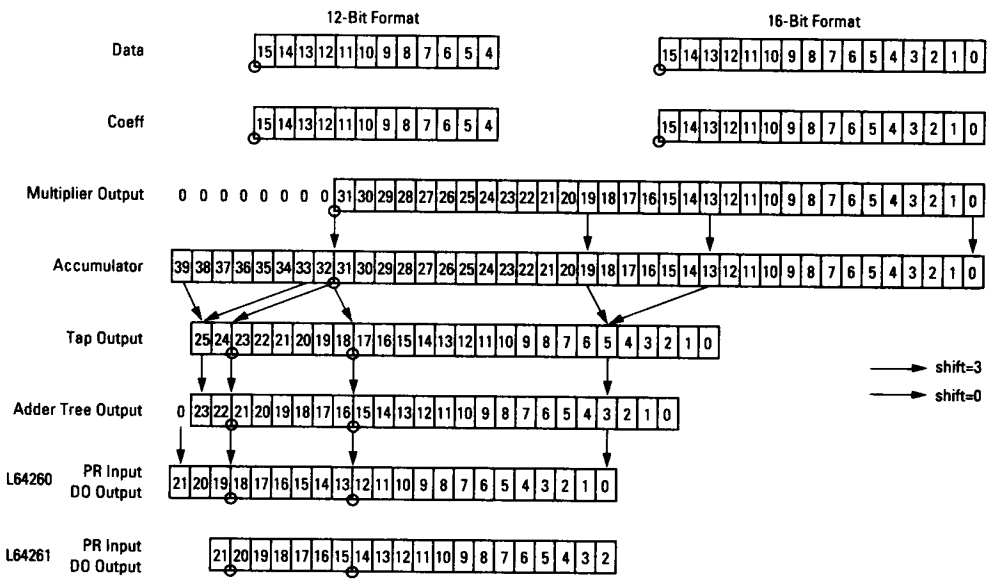
Fractional Data Formats and the L64260/L64261

Any combination of fractional signed and unsigned data and coefficients can be handled by the L64260/61. A fractional number is one in which the magnitude is always strictly less than one. The following diagrams show the flow of the data within the VFIR for different combinations of signed and unsigned data and coefficients. The binary point, indicated by the dark circle, is shown for shift values of 0 and 3.

The results are shown for both the L64260 and L64261 each operating with either 12- or 16-bit data and coefficients. 12-bit (or any other number of bits less than 16) operation is the same as 16-bit operation with the LSBs set to zero. For fractional data formats, the position of the binary point at each stage of the computation is unaffected by the number of significant bits.

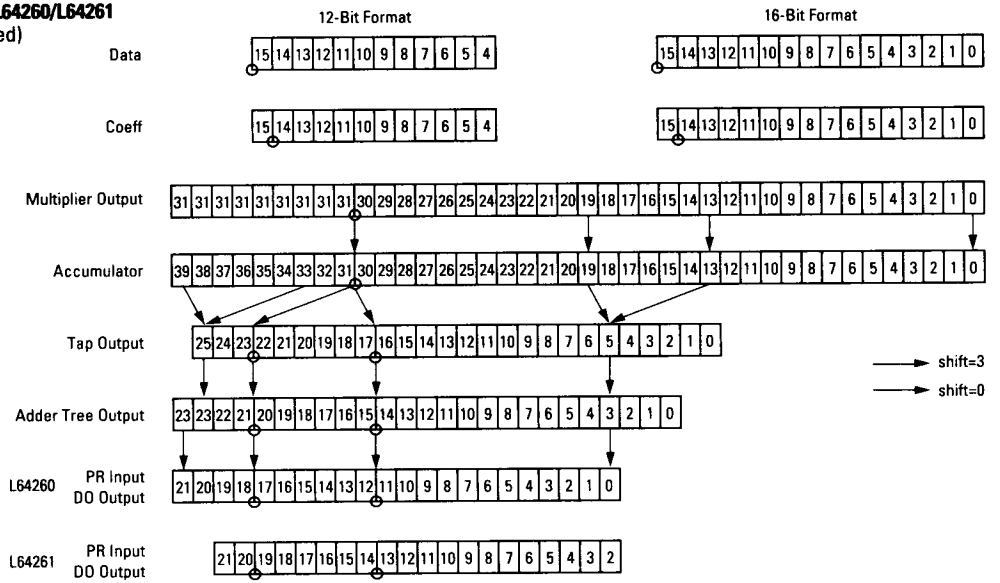
When the number of bits is reduced, simple truncation is performed. Because the accumulator is 40 bits wide, the dynamic range of the computations will be greatest if each result is computed within a single multiplier-accumulator. In this case, the result will be truncated at the end of the computation rather than at an intermediate stage.

Data Flow for Unsigned Data and Coefficients

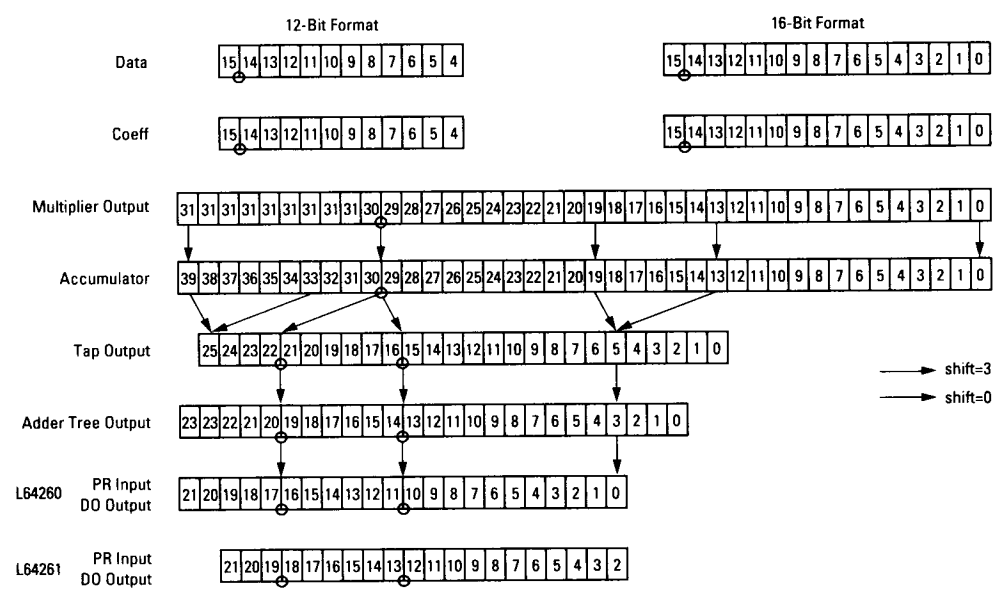


Fractional Data Formats and the L64260/L64261 (Continued)

Data Flow for Unsigned Data and Signed Coefficients (Data and Coefficients can be swapped)



Data Flow for Signed Data and Coefficients



Fractional Data Formats and the L64260/L64261 (Continued)

The number of products which can be summed without the possibility of overflow (in a single device) is a function of the data formats and the shift value and is tabulated below. With appropriate constraints on the data or coefficients, a sum of a greater number of products can be formed without overflow.

Data Format	Coeff Format	Shift Value	No. of Products	
			L64260	L64261
Signed	Signed	0	512	256
		1	128	64
		2	32	16
		3	8	4
Unsigned	Signed	0	256	128
		1	64	32
Signed	Unsigned	2	16	8
		3	4	2
Unsigned	Unsigned	0	256	64
		1	64	16
		2	16	4
		3	4	1

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 over the specified temperature and voltage ranges [1].

Symbol	Parameter	Condition			Min	Typ	Max	Units
VIL	Low level input voltage						0.8	V
VIH	High level input voltage							
	Commercial temperature range				2.0			V
	Military temperature range				2.25			V
IIN	Input current	VIN = VDD			-150		200	µA
VOH	High level output voltage		Comm	Mil				
		IOH =	-4 mA	-3.2 mA	2.4	4.5		V
VOL	Low level output voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOS	Output short circuit current [2]	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = 0V			-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					10	mA
IDD	Operating supply current	tCYCLE = 25 ns				300		mA
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

Notes:
1. Military temperature range is -55°C to +125°C, ±10% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

AC Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V).

Symbol	Parameter	L64260/L64261A		L64260/L64261	
		Min	Typ	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	25		33	
t PWH	Minimum clock (CLK) pulse width, HIGH	8		11	
tPWL	Minimum clock (CLK) pulse width, LOW	8		11	
tPIS	PR setup time [2]	6		8	
tPIS	PR setup time [3]	20		24	
tPIH	PR hold time	4		6	
tDIS	DI0–DI3, CI0–CI3, CT setup time	6		8	
tDIH	DI0–DI3, CI0–CI3, CT hold time	4		6	
tOD	Output delay (D0,SR0) from CLK [4]		18		22
tRS	REGADR setup time with respect to $\overline{WE}\downarrow$	5		7	
tRH	REGADR hold time with respect to $\overline{WE}\uparrow$	5		7	
tCS	CI0, CI3 setup time with respect to $\overline{WE}\downarrow$	8		11	
tCH	CI0, CI3 hold time with respect to $\overline{WE}\uparrow$	10		14	
tWW	Minimum $\overline{WE}$ pulse width, LOW	8		11	
tWC	Minimum $\overline{WE}$ cycle time	25		33	

Notes:
1. All times are in ns.
2. When ENREG is HIGH
3. When ENREG is LOW
4. CLOAD = 55 pF

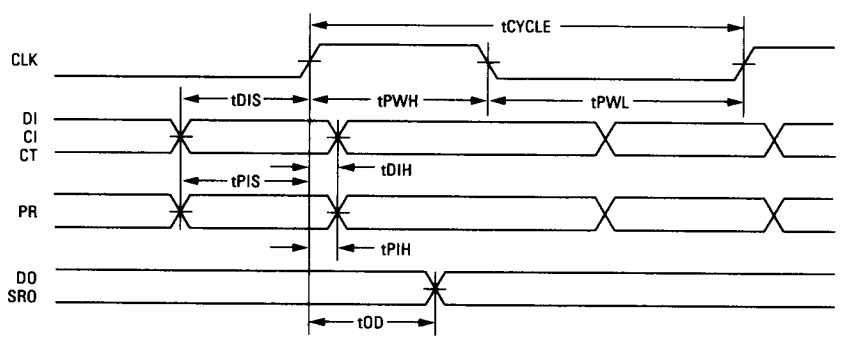
AC Characteristics: Military (TA = -55°C to 125°C, VDD = 4.5 V to 5.5 V).

Symbol	Parameter	L64260/L64261A		L64260/L64261	
		Min	Typ	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	33		40	
t PWH	Minimum clock (CLK) pulse width, HIGH	11		15	
tPWL	Minimum clock (CLK) pulse width, LOW	11		15	
tPIS	PR setup time [2]	8		10	
tPIS	PR setup time [3]	27		32	
tPIH	PR hold time	6		8	
tDIS	DI0–DI3, CI0–CI3, CT setup time	6		8	
tDIH	DI0–DI3, CI0–CI3, CT hold time	4		6	
tOD	Output delay (DO,SR0) from CLK [4]		24		28
tRS	REGADR setup time with respect to $\overline{WE}$ Ø	7		9	
tRH	REGADR hold time with respect to $\overline{WE}$ ≠	7		9	
tCS	CI0, CI3 setup time with respect to $\overline{WE}$ Ø	11		15	
tCH	CI0, CI3 hold time with respect to $\overline{WE}$ ≠	13		19	
tWW	Minimum $\overline{WE}$ pulse width, LOW	11		15	
tWC	Minimum $\overline{WE}$ cycle time	33		40	

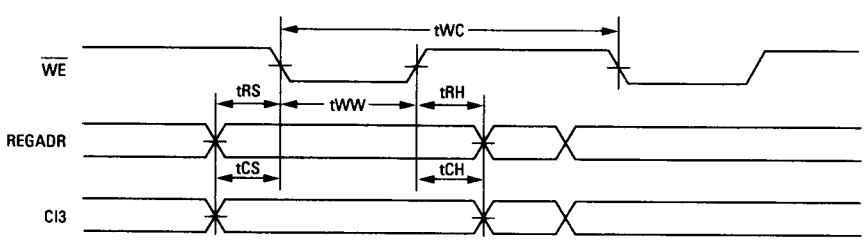
Notes:
1. All times are in ns.
2. When ENREG is HIGH
3. When ENREG is LOW
4. CLOAD = 55 pF

AC Timing Waveforms

Timing for Normal Filter Operation



Timing for Normal Filter Operation



L64260 Package Pin Information (223-Pin PGA, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	VDD	C4	DO.20	E16	CI3.10	K4	CI0.6	R2	CI1.11	U4	PR.20
A3	DI0.8	C5	DI0.12	E17	CI3.11	K15	DO.3	R3	DI1.10	U5	PR.18
A4	DI0.11	C6	DI0.14	E18	CI2.0	K16	DO.5	R4	CI1.6	U6	DI1.13
A5	DI3.14	C7	DO.10	F1	CI0.11	K17	DI2.0	R5	CI1.4	U7	DI1.15
A6	DI3.12	C8	DO.12	F2	CI1.0	K18	VSS	R6	PR.16	U8	PR.0
A7	DO.13	C9	DI3.9	F3	CI1.1	L1	$\overline{WE}$	R7	PR.14	U9	DI2.15
A8	VSS	C10	DI3.8	F4	DI0.0	L2	DI1.5	R8	SR0.0	U10	SR0.3
A9	VDD	C11	DI3.6	F15	CI3.9	L3	DI1.6	R9	SR0.2	U11	DI2.14
A10	VSS	C12	SR0.13	F16	CI3.2	L4	CI0.3	R10	DI2.12	U12	PR.9
A11	DO.17	C13	SR0.11	F17	CI2.3	L15	DO.1	R11	DI2.10	U13	PR.7
A12	DO.19	C14	DI3.2	F18	CI3.14	L16	DO.2	R12	DI2.8	U14	PR.5
A13	DI3.5	C15	SR0.6	G1	CI0.9	L17	DI2.1	R13	PR.3	U15	CT.5
A14	DI3.3	C16	CI3.4	G2	CI0.10	L18	VDD	R14	CT.3	U16	CT.1
A15	DI3.1	C17	CI3.5	G3	CI0.12	M1	CI0.5	R15	CI2.4	U17	VDD
A16	SR0.5	C18	CI3.6/CT.6	G4	CI0.13	M2	CI0.4	R16	CI2.6	U18	VSS
A17	VDD	D1	DI0.1	G15	CI3.3	M3	CI0.1	R17	CI2.8	V1	VSS
A18	VSS	D2	DI0.2	G16	C13.12	M4	CI0.0	R18	DI2.5	V2	VDD
B1	VDD	D3	CI1.3	G17	DO.9	M15	CI2.14	T1	CI1.9	V3	CI1.5
B2	VSS	D4	DI0.6	G18	DO.7	M16	DI2.2	T2	CI1.8	V4	DI1.12
B3	DO.21	D5	DI0.9	H1	VSS	M17	CI2.15	T3	CI1.7	V5	PR.17
B4	DI0.10	D6	DI3.15	H2	CI0.8	M18	DO.0	T4	PR.21	V6	DI1.14
B5	DI0.13	D7	DI0.15	H3	DI1.1	N1	CI0.2	T5	PR.19	V7	PR.1
B6	DI3.13	D8	DO.11	H4	DI1.0	N2	DI1.7	T6	PR.15	V8	VSS
B7	DI3.11	D9	DI3.10	H15	CI3.13	N3	CI1.15	T7	PR.13	V9	VDD
B8	DO.14	D10	DI3.7	H16	CI3.15	N4	CI1.13	T8	SR0.1	V10	VSS
B9	DO.15	D11	SR0.14	H17	DO.6	N15	CI2.11	T9	PR.12	V11	PR.11
B10	DO.16	D12	SR0.12	H18	CI2.1	N16	DI2.3	T10	DI2.13	V13	PR.10
B11	DO.18	D13	SR0.9	J1	VDD	N17	CI2.12	T11	DI2.11	V13	PR.8
B12	SR0.15	D14	SR0.7	J2	DI1.4	N18	CI2.13	T12	DI2.9	V14	PR.6
B13	DI3.4	D15	DI3.0	J3	DI1.3	P1	DI1.8	T13	DI2.7	V15	PR.2
B14	SR0.10	D16	CI3.0	J4	DI1.2	P2	CI1.14	T14	PR.4	V16	CT.2
B15	SR0.8	D17	CI3.8	J15	CI2.2	P3	CI1.12	T15	CT.4	V17	VSS
B16	SR0.4	D18	CI3.1	J16	DO.8	P4	CI1.10	T16	CT.0	V18	VDD
B17	VSS	E1	CI0.14	J17	DO.4	P15	CI2.7	T17	DI2.6		
B18	VDD	E2	CI0.15	J18	VDD	P16	CI2.9	T18	CI2.5		
C1	DI0.4	E3	CI1.2	K1	VSS	P17	CI2.10	U1	VDD		
C2	DI0.5	E4	DI0.3	K2	CI0.7	P18	DI2.4	U2	VSS		
C3	DI0.7	E15	CI3.7/CT.7	K3	CLK	R1	DI1.9	U3	DI1.11		

L64260 Package Pin Information (223-Pin PGA, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
M4	CI0.0	R16	CI2.6	C2	DI0.5	T11	DI2.11	A11	D0.17	C13	SR0.11
M3	CI0.1	P15	CI2.7	D4	DI0.6	R10	DI2.12	B11	D0.18	D12	SR0.12
N1	CI0.2	R17	CI2.8	C3	DI0.7	T10	DI2.13	A12	D0.19	C12	SR0.13
L4	CI0.3	P16	CI2.9	A3	DI0.8	U11	DI2.14	C4	D0.20	D11	SR0.14
M2	CI0.4	P17	CI2.10	D5	DI0.9	U9	DI2.15	B3	D0.21	B12	SR0.15
M1	CI0.5	N15	CI2.11	B4	DI0.10	D15	DI3.0	U8	PR.0	A17	VDD
K4	CI0.6	N17	CI2.12	A4	DI0.11	A15	DI3.1	V7	PR.1	A2	VDD
K2	CI0.7	N18	CI2.13	C5	DI0.12	C14	DI3.2	V15	PR.2	A9	VDD
H2	CI0.8	M15	CI2.14	B5	DI0.13	A14	DI3.3	R13	PR.3	B1	VDD
G1	CI0.9	M17	CI2.15	C6	DI0.14	B13	DI3.4	T14	PR.4	B18	VDD
G2	CI0.10	D16	CI3.0	D7	DI0.15	A13	DI3.5	U14	PR.5	J1	VDD
F1	CI0.11	D18	CI3.1	H4	DI1.0	C11	DI3.6	V14	PR.6	J18	VDD
G3	CI0.12	F16	CI3.2	H3	DI1.1	D10	DI3.7	U13	PR.7	L18	VDD
G4	CI0.13	G15	CI3.3	J4	DI1.2	C10	DI3.8	V13	PR.8	U1	VDD
E1	CI0.14	C16	CI3.4	J3	DI1.3	C9	DI3.9	U12	PR.9	U17	VDD
E2	CI0.15	C17	CI3.5	J2	DI1.4	D9	DI3.10	V12	PR.10	V18	VDD
F2	CI1.0	C18	CI3.6/CT.6	L2	DI1.5	B7	DI3.11	V11	PR.11	V2	VDD
F3	CI1.1	E15	CI3.7/CT.7	L3	DI1.6	A6	DI3.12	T9	PR.12	V9	VDD
E3	CI1.2	D17	CI3.8	N2	DI1.7	B6	DI3.13	T7	PR.13	A10	VSS
D3	CI1.3	F15	CI3.9	P1	DI1.8	A5	DI3.14	R7	PR.14	A18	VSS
R5	CI1.4	E16	CI3.10	R1	DI1.9	D6	DI3.15	T6	PR.15	A8	VSS
V3	CI1.5	E17	CI3.11	R3	DI1.10	M18	D0.0	R6	PR.16	B17	VSS
R4	CI1.6	G16	CI3.12	U3	DI1.11	L15	D0.1	V5	PR.17	B2	VSS
T3	CI1.7	H15	CI3.13	V4	DI1.12	L16	D0.2	U5	PR.18	H1	VSS
T2	CI1.8	F18	CI3.14	U6	DI1.13	K15	D0.3	T5	PR.19	K1	VSS
T1	CI1.9	H16	CI3.15	V6	DI1.14	J17	D0.4	U4	PR.20	K18	VSS
P4	CI1.10	K3	CLK	U7	DI1.15	K16	D0.5	T4	PR.21	U18	VSS
R2	CI1.11	T16	CT.0	K17	DI2.0	H17	D0.6	R8	SR0.0	U2	VSS
P3	CI1.12	U16	CT.1	L17	DI2.1	G18	D0.7	T8	SR0.1	V1	VSS
N4	CI1.13	V16	CT.2	M16	DI2.2	J16	D0.8	R9	SR0.2	V10	VSS
P2	CI1.14	R14	CT.3	N16	DI2.3	G17	D0.9	U10	SR0.3	V17	VSS
N3	CI1.15	T15	CT.4	P18	DI2.4	C7	D0.10	B16	SR0.4	V8	VSS
E18	CI2.0	U15	CT.5	R18	DI2.5	D8	D0.11	A16	SR0.5	L1	$\overline{WE}$
H18	CI2.1	F4	DI0.0	T17	DI2.6	C8	D0.12	C15	SR0.6		
J15	CI2.2	D1	DI0.1	T13	DI2.7	A7	D0.13	D14	SR0.7		
F17	CI2.3	D2	DI0.2	R12	DI2.8	B8	D0.14	B15	SR0.8		
R15	CI2.4	E4	DI0.3	T12	DI2.9	B9	D0.15	D13	SR0.9		
T18	CI2.5	C1	DI0.4	R11	DI2.10	B10	D0.16	B14	SR0.10		

L64261 Package Pin Information (144-Pin PGA, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	DI0.5	B10	CI1.15	D13	DI1.14	H13	VSS	M13	CI2.4	P7	CI3.15
A2	DI0.1	B11	CI1.12	D14	PR.18/DI1.10	H14	PR.12/DI1.4	M14	CT.2	P8	DO.9
A3	CI0.13	B12	CI1.9	D15	PR.16/DI1.8	H15	MP	M15	PR.4/DI12.8	P9	DO.5
A4	CI0.12	B13	CI1.7	E1	DI0.15	J1	DO.18	N1	SR0.I1/DI3.I1	P10	DO.4
A5	CI0.10	B14	CI1.4	E2	DI0.11	J2	DO.20	N2	SR0.I8/DI3.I8	P11	CI2.15
A6	VSS	B15	PR.21/DI1.13	E3	DI0.9	J3	VSS	N3	SR0.5/DI3.5	P12	CI2.12
A7	VDD	C1	DI0.10	E13	PR.19/DI1.11	J13	PR.9/DI2.13	N4	CI3.4	P13	CI2.10
A8	CI0.6	C2	DI0.6	E14	PR.15/DI1.7	J14	PR.8/DI2.12	N5	VSS	P14	CI2.6
A9	CI0.4	C3	DI0.3	E15	SR0.0/DI2.4	J15	PR.11/DI2.15	N6	CI3.11	P15	CT.1
A10	CI0.3	C4	DI0.2	F1	DO.14	K1	DO.19	N7	CI3.14	R1	VDD
A11	CI0.0	C5	CI0.15	F2	DI0.14	K2	DO.21	N8	VSS	R2	CI3.6/CT.6
A12	CI1.13	C6	CI0.9	F3	DI0.13	K3	SR0.15/DI3.15	N9	VDD	R3	CI3.8
A13	CI1.11	C7	WE	F13	SR0.1/DI2.5	K13	PR.5/DI2.9	N10	DO.3	R4	CI3.10
A14	CI1.8	C8	CLK	F14	SR0.2/DI2.6	K14	PR.6/DI2.10	N11	CI2.11	R5	CI3.13
A15	CI1.5	C9	CI0.2	F15	PR.14/DI1.6	K15	PR.10/DI2.14	N12	CI2.8	R6	DO.11
B1	DI0.7	C10	CI1.14	G1	DO.15	L1	SR0.14/DI3.13	N13	CI2.7	R7	DO.10
B2	DI0.4	C11	CI1.10	G2	DO.12	L2	SR0.13/DI3.13	N14	CT.0	R8	DO.8
B3	DI0.0	C12	CI1.6	G3	DO.13	L3	SR0.9/DI3.9	N15	CT.4	R9	DO.7
B4	CI0.14	C13	DI1.15	G13	VDD	L13	CT.3	P1	SR0.7/DI3.7	R10	DO.6
B5	CI0.11	C14	PR.20/DI1.12	G14	SR0.3/DI2.7	L14	CT.5	P2	SR0.4/DI3.4	R11	DO.2
B6	CI0.8	C15	PR.17/DI1.9	G15	PR.13/DI1.5	L15	PR.7/DI2.11	P3	CI3.5	R12	CI2.14
B7	CI0.7	D1	DI0.12	H1	DO.17	M1	SR0.12/DI3.12	P4	CI3.7/CT.7	R13	CI2.13
B8	CI0.5	D2	DI0.8	H2	DO.16	M2	SR0.10/DI3.10	P5	CI3.9	R14	CI2.9
B9	CI0.1	D3	VDD	H3	VDD	M3	SR0.6/DI3.6	P6	CI3.12	R15	CI2.5

L64261 Package Pin Information (144-Pin PGA, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A11	CI0.0	B11	CI1.12	P6	CI3.12	F3	DI0.13	K2	D0.21	P2	SR0.4/DI3.4
B9	CI0.1	A12	CI1.13	R5	CI3.13	F2	DI0.14	H15	MP	N3	SR0.5/DI3.5
C9	CI0.2	C10	CI1.14	N7	CI3.14	E1	DI0.15	M15	PR.4/DI2.8	M3	SR0.6/DI3.6
A10	CI0.3	B10	CI1.15	P7	CI3.15	D13	DI1.14	K13	PR.5/DI2.9	P1	SR0.7/DI3.7
A9	CI0.4	M13	CI2.4	C8	CLK	C13	DI1.15	K14	PR.6/DI2.10	N2	SR0.8/DI3.8
B8	CI0.5	R15	CI2.5	N14	CT.0	R11	D0.2	L15	PR.7/DI2.11	L3	SR0.9/DI3.9
A8	CI0.6	P14	C12.6	P15	CT.1	N10	D0.3	J14	PR.8/DI2.12	M2	SR0.10/DI3.10
B7	CI0.7	N13	CI2.7	M14	CT.2	P10	D0.4	J13	PR.9/DI2.13	N1	SR0.11/DI3.11
B6	CI0.8	N12	CI2.8	L13	CT.3	P9	D0.5	K15	PR.10/DI2.14	M1	SR0.12/DI3.12
C6	CI0.9	R14	CI2.9	N15	CT.4	R10	D0.6	J15	PR.11/DI2.15	L2	SR0.13/DI3.13
A5	CI0.10	P13	CI2.10	L14	CT.5	R9	D0.7	H14	PR.12/DI1.4	L1	SR0.14/DI3.14
B5	CI0.11	N11	CI2.11	B3	DI0.0	R8	D0.8	G15	PR.13/DI1.5	K3	SR0.15/DI13.15
A4	CI0.12	P12	CI2.12	A2	DI0.1	P8	D0.9	F15	PR.14/DI1.6	A7	VDD
A3	CI0.13	R13	CI2.13	C4	DI0.2	R7	D0.10	E14	PR.15/DI1.7	D3	VDD
B4	CI0.14	R12	CI2.14	C3	DI0.3	R6	D0.11	D15	PR.16/DI1.8	G13	VDD
C5	CI0.15	P11	CI2.15	B2	DI0.4	G2	D0.12	C15	PR.17/DI1.9	H3	VDD
B14	CI1.4	N4	CI3.4	A1	DI0.5	G3	D0.13	D14	PR.18/DI1.10	N9	VDD
A15	CI1.5	P3	CI3.5	C2	DI0.6	F1	D0.14	E13	PR.19/DI1.11	R1	VDD
C12	CI1.6	R2	CI3.6/CT.6	B1	DI0.7	G1	D0.15	C14	PR.20/DI1.12	A6	VSS
B13	CI1.7	P4	CI3.7/CT.7	D2	DI0.8	H2	D0.16	B15	PR.21/DI1.13	H13	VSS
A14	CI1.8	R3	CI3.8	E3	DI0.9	H1	D0.17	E15	SR0.0/DI2.4	J3	VSS
B12	CI1.9	P5	CI3.9	C1	DI0.10	J1	D0.18	F13	SR0.1/DI2.5	N5	VSS
C11	CI1.10	R4	CI3.10	E2	DI0.11	K1	D0.19	F14	SR0.2/DI2.6	N8	VSS
A13	CI1.11	N6	CI3.11	D1	DI0.12	J2	D0.20	G14	SR0.3/DI2.7	C7	$\overline{WE}$

Packaging

223-Pin Ceramic Pin Grid Array (Cavity Down): See FS Package in Package Selector Guide
144-Pin Ceramic Pin Grid Array: See FE Package in Package Selector Guide

L64260 Ordering Information

L64260 G C -XX

- -XX: Speed in MHz
- C: Temperature Range/Flow Option
  C = Commericial (0°C to 70°C)
  M = Military (-55°C to + 125°C), Processed to MIL-STD-883C Level B
- G: Package Code
  G = 223-Pin Ceramic Pin Grid Array
- L64260: Device Type
  Versatile FIR Filter

L64261 Ordering Information

L64261 G M -XX

- -XX: Speed in MHz
- M: Temperature Range/Flow Option
  C = Commericial (0°C to 70°C)
  M = Military (-55°C to + 125°C), Processed to MIL-STD-883C Level B
- G: Package Code
  G = 144-Pin Ceramic Pin Grid Array
- L64261: Device Type
  Versatile FIR Filter