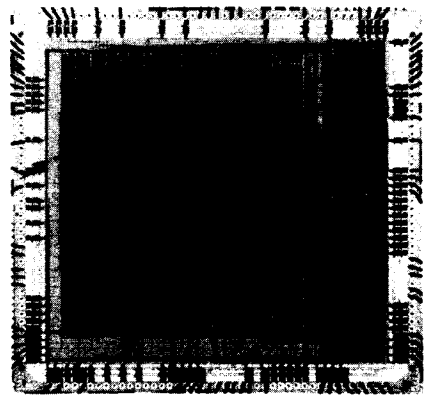
L64210/L64211 Variable-Length Video Shift Registers

Description

The L64210 and L64211 are two high-speed Variable-Length Video Shift Registers. These devices can be used individually or as video line delays for the L64200 series filter processors.

The L64210 provides four individual 8-bit shift registers, each with a length of up to 1032, and is packaged in a 68-pin Plastic Leaded Chip Carrier or Ceramic Pin Grid Array.

The L64211 provides eight individual 8-bit shift registers, each with a length adjustable to 516 and is packaged in a 120-pin Plastic or Ceramic Pin Grid Array.



L64210 Chip

Features

- Variable-length video shift register
- Acts as a variable-length line delay, reformatting serial (raster-scanned video) data into a 2-D video signal for image processing
- Can work individually or with any of the LSI Logic L64200 series filter processors
- L64210 contains four separate 8-bit shift registers whose length can be varied from 24 to 1032
- L64211 contains eight separate 8-bit shift registers whose length can be varied from 12 to 516
- High data rates

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Control available to blank (force to zero) data outputs during horizontal video blanking intervals
- Control available to blank (force to zero) data inputs, which could be used to ignore invalid data during vertical video blanking intervals
- Input data can be sent to all eight internal shift registers simultaneously
- L64210 is available in a 68-pin PLDCC (Plastic Leaded Chip Carrier) or CPGA (Ceramic Pin Grid Array) package
- L64211 is available in a 120-pin PPGA or CPGA (Plastic or Ceramic Pin Grid Array) package

Architecture

The L64211 contains eight individual 8-bit variable-length shift registers which can be used as video line delays. The L64210 has every other shift register output connected to external package pins and effectively has four individual 8-bit shift registers. The length of the shift registers is controlled by the value residing in the level-triggered LENGTH latch register controlled by an active LOW $\overline{WE}$ input. The length of each of the eight shift registers of the L64211 can be varied from 12 to 516 bits by loading the LENGTH register according to:

Number of Shifts = (4 • LENGTH) + 8.

where 0 is an illegal input. Since the L64210 internally cascades two shift registers together, each of the resulting four registers can be varied from 24 to 1032 bits long, and its length is determined by the equation:

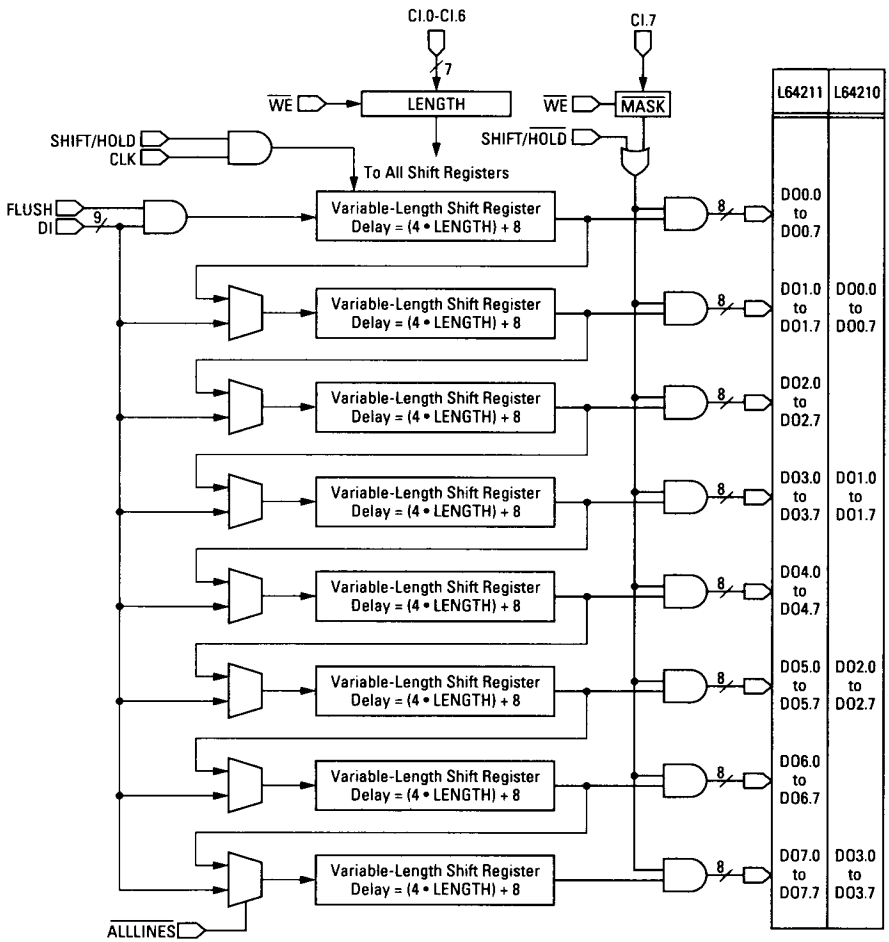
Number of Shifts = (8 • LENGTH) + 16.

Architecture (Continued)

In a video or image-processing system, the length of each shift register is normally set to the number of pixels per video line. When used in this fashion (as a video line delay or as a front end to any of the LSI Logic real-time image-processing chips), the line delay ouputs the pixels vertically adjacent to (in the same column as) the input pixel. In the case of the L64211, the outputs of the eight line delays will be eight pixels in a vertical line.

To accommodate the horizontal and vertical blanking periods of a video signal, provision is made to disable the shift register. The SHIFT/$\overline{\text{HOLD}}$ input causes the system clock to be disabled - ie data is not shifted. The $\overline{\text{MASK}}$ and $\overline{\text{FLUSH}}$ controls allow the outputs and inputs respectively of the device to be forced to zero.

Block Diagram



Pin Listing and Description

DI
Eight-bit input data bus. Data inputs are loaded into the first stage of the shift register at the rising edge of CLK while SHIFT/$\overline{\text{HOLD}}$ is HIGH.

CLK
System clock. Active at the rising edge.

$\overline{\text{FLUSH}}$
When $\overline{\text{FLUSH}}$ is LOW, zeros are forced into the shift register. This action overrides the data on DI bus. If $\overline{\text{FLUSH}}$ is connected to the vertical blanking signal in a video system, the input will be blank during the blanking period.

CI.0 to CI.7
Control input bus. This bus is common to all L64200 series devices. On the L64210/11, the bus feeds into two control registers, LENGTH and $\overline{\text{MASK}}$.

$\overline{\text{WE}}$
Active-LOW Write Enable for the CI (LENGTH and $\overline{\text{MASK}}$ control) inputs. When $\overline{\text{WE}}$ is LOW, new data is written into the LENGTH and $\overline{\text{MASK}}$ registers. LENGTH becomes active at the next rising edge of CLK.

SHIFT/$\overline{\text{HOLD}}$
Disables the action of the CLK input and forces the shift register outputs LOW when $\overline{\text{MASK}}$ is LOW. When SHIFT/$\overline{\text{HOLD}}$ is connected to the horizontal blanking signal in a video system, data will not be loaded during the horizontal blanking period.

DOX.Y
Data output buses where X and Y represent the output bus number and bit numbers, respectively. The L64210 has 4 8-bit output buses, while the L64211 has 8 8-bit output buses.

$\overline{\text{ALLLINES}}$
When $\overline{\text{ALLLINES}}$ is LOW, data from DI bus (overridden by $\overline{\text{FLUSH}}$) is fed into all eight shift registers simultaneously. $\overline{\text{ALLLINES}}$ is intended as a test function; in normal operation it should be held HIGH.

$\overline{\text{TEST}}$
Internal LSI Logic test input. Should be held HIGH or left unconnected by user.

Loading of Control Words

The L64210 and L64211 are configured by writing an 8-bit control word to the LENGTH and $\overline{\text{MASK}}$ registers. The LENGTH register, accessed through CI.0 - CI.6 is a number between 0 and 127 which controls the length of the individual shift registers.

For the L64210 each of the four shift registers will be of length (8 • LENGTH) + 16. For the L64211 the length of each of the eight shift registers will be (4 • LENGTH) + 8.

The value written into LENGTH becomes active on the next rising edge of the clock after it has been written. The value in this register must be greater than zero for correct operation.

The $\overline{\text{MASK}}$ register, which is accessed through CI.7, controls the masking of the outputs. If a zero is written into $\overline{\text{MASK}}$ then the effect of the SHIFT/$\overline{\text{HOLD}}$ input will be to force all data outputs to zero. If a one is written into $\overline{\text{MASK}}$ then the effect of the SHIFT/$\overline{\text{HOLD}}$ input will be to freeze the current value on the outputs.

Both the $\overline{\text{MASK}}$ and LENGTH registers are loaded when $\overline{\text{WE}}$ is LOW.

Blanking Periods

Typically the horizontal blanking signal of a video system will be tied to the SHIFT/$\overline{\text{HOLD}}$ input. This disables the clock and hence disables data input to the device, during the blanking period. If $\overline{\text{MASK}}$ has been set LOW then this will also have the effect of setting to zero – ie blanking – the data outputs.

If $\overline{\text{MASK}}$ is LOW and SHIFT/$\overline{\text{HOLD}}$ is taken LOW then the delay from SHIFT/$\overline{\text{HOLD}}$ going LOW to the data outputs being valid (ie zero) is 20 ns.

When SHIFT/$\overline{\text{HOLD}}$ is taken HIGH again, the delay to data outputs being valid is 15 ns. The vertical blanking signal might be connected to the $\overline{\text{FLUSH}}$ input, causing zeros to be input into the device during this period. This means that any spurious data during vertical blanking will be ignored, leaving only zero data values between frames.

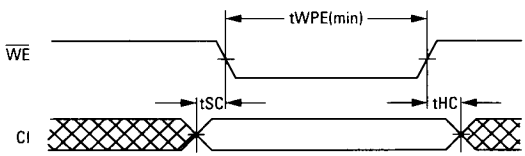
For operation as a standard shift register, both $\overline{\text{FLUSH}}$ and $\overline{\text{MASK}}$ should be held high.

Data Retention

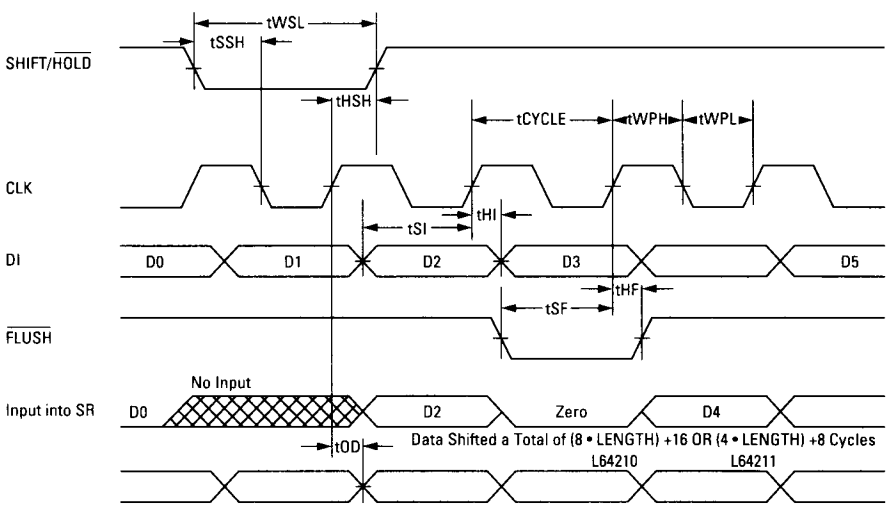
The shift registers in the L64210 and L64211 are constructed from DRAM cells. These DRAM cells are refreshed only when a new data value is written into that location. In the worst case, ie with the shift registers set to their maximum length, there will be 512 cycles, plus any time when SHIFT/$\overline{\text{HOLD}}$ is held LOW, between successive writes to a location. The DRAM used will retain data for 200 usecs. Care must be taken to ensure that the cumulative time between accesses does not exceed this limit. The maximum values given in the AC Switching Characteristics for tCYCLE and tWSL are an example of meeting this requirement: the total time elapsed between successive writes to the same memory location is given by (512 • 200) + 100,000 = 200,400 ns. In practice, the designer may trade off the parameters of LENGTH, tCYCLE and tWSL as long as this 200 usec limit is observed.

AC Timing

Coefficient/Control Section



Input Timing



AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64210-20 L64211-20		L64210-15 L64211-15	
tCYCLE	Clock cycle time	50	400*	65	400*
tPWH(min)	Min clock pulse width HIGH	20		30	
tPWL(min)	Min clock pulse width LOW	20		30	
tSI	Input data set-up time	15		20	
tHI	Input data hold time	5		10	
tWPE	WE pulse width	20		30	
tSC	CI input set-up time	10		15	
tHC	CI input hold time	10		15	
tSF	FLUSH input set-up time	15		20	
tHF	Flush input hold time	5		10	
tOD	Output delay time		33		40
tSSH	SHIFT/HOLD set-up time	2		3	
tHSH	SHIFT/HOLD hold time	0		0	
tWSL	SHIFT/HOLD width LOW		200,000*		200,000

AC Switching Characteristics: Military (TA = 55°C to 125°C, VDD = 4.5 V to 5.5 V)

Symbol	Parameter	L64210-16 L64211-16		L64210-12 L64211-12	
tCYCLE	Clock cycle time	60	400*	75	400*
tPWH(min)	Min clock pulse width HIGH	25		35	
tPWL(min)	Min clock pulse width LOW	25		35	
tSI	Input data set-up time	20		25	
tHI	Input data hold time	10		15	
tWPE	WE pulse width	30		35	
tSC	CI input set-up time	15		20	
tHC	CI input hold time	15		20	
tSF	FLUSH input set-up time	20		25	
tHF	Flush input hold time	10		15	
tOD	Output delay time		35		55
tSSH	SHIFT/HOLD set-up time	3		4	
tHSH	SHIFT/HOLD hold time	0		0	
tWSL	SHIFT/HOLD width LOW		200,000*		200,000

All units are in ns, output loading = 50 pF.
* Assuming SHIFT/HOLD always HIGH, LENGTH = 127.
** Assuming LENGTH = 1 (see text for further information).

Ordering Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to + 150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range	TA	- 55 to + 125	°C
Military			
Commercial	TA	0 to + 70	°C

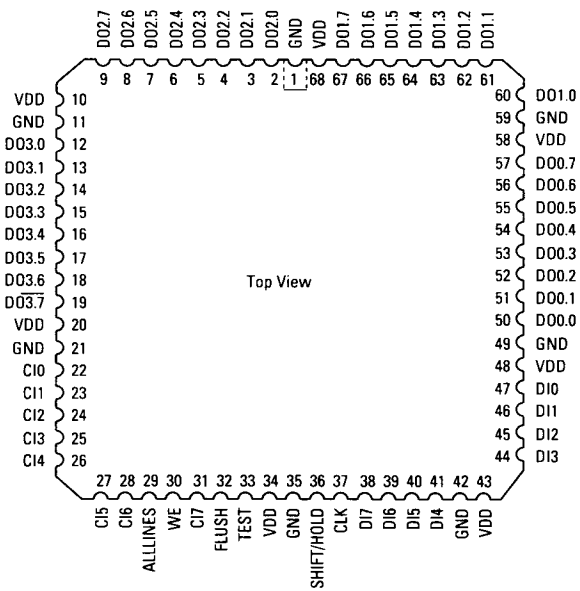
DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges[1]

Symbol	Parameter	Condition			Min	Typ	Max	Units
VIL	Low level input voltage						0.8	V
VIH	High level input voltage Commercial temperature range Military temperature range				2.0 2.25			V V
IIN	Input current	VIN = VDD			-150		200	µA
VOH	High level output voltage		Comm	Mil				
		IOH =	–4 mA	–3.2 mA	2.4	4.5		V
VOL	Low level output voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOS	Output short circuit current[2]	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = OV			–5		–100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					10	mA
IDD	Operating supply current	tCYCLE = 50 ns				300		mA
CIN	Input capacitance	Any Input				5		pF
COUT	Output capacitance	Any Output				10		pF

Notes:
1. Military temperature range is -55°C to + 125°C, ± 10% power supply; commercial temperature range is 0°C to 70°C, ± 5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

L64210 Pinout Diagram

68-Pin Plastic Leaded Chip Carrier (PLCC)



68-Pin Grid Array (PGA)

	1	2	3	4	5	6	7	8	9	10	11
A		DO2.7	DO2.6	DO2.4	DO2.2	DO2.0	VDD	DO1.6	DO1.4	DO1.2	
B	GND	VDD	DO2.5	DO2.3	DO2.1	GND	DO1.7	DO1.5	DO1.3	DO1.1	DO1.0
C	DO3.1	DO3.0	X	← Extra Pin						VDD	GND
D	DO3.3	DO3.2								DO0.6	DO0.7
E	DO3.5	DO3.4								DO0.4	DO0.5
F	DO3.7	DO3.6			Top View					DO0.2	DO0.3
G	GND	VDD								DO0.0	DO0.1
H	CI1	CI0								VDD	GND
J	CI3	CI2								DI1	DI0
K	CI4	CI5	$\overline{\text{ALL LINES}}$	CI7	$\overline{\text{TEST}}$	GND	CLK	DI6	DI4	DI3	DI2
L		CI6	$\overline{\text{WE}}$	$\overline{\text{FLUSH}}$	VDD	SHIFT/$\overline{\text{HOLD}}$	DI7	DI5	GND	VDD	

LSI LOGIC

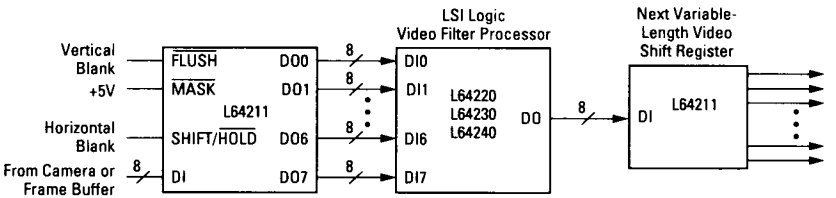
L64211 Pinout Diagram

120-Pin Ceramic Pin Grid Array (CPGA)

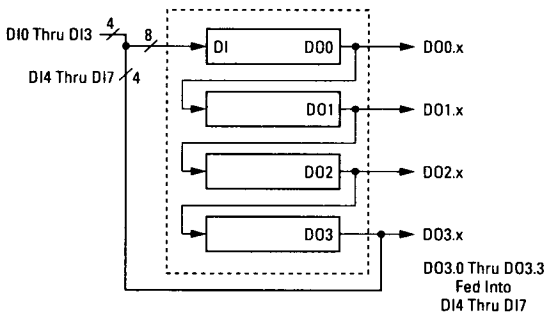
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	DO5.6	DO5.5	DO5.3	NC	DO5.0	NC	VDD	NC	NC	DO3.4	DO3.1	DO3.0
B	VDD	NC	DO5.7	DO5.4	DO5.2	NC	NC	NC	NC	DO3.5	DO3.3	NC	VDD
C	DO7.1	DO7.0	NC	NC	NC	DO5.1	GND	DO3.7	NC	DO3.2	NC	NC	DO1.7
D	DO7.4	DO7.2	GND	X	Extra Pin						GND	DO1.6	DO1.4
E	DO7.6	DO7.5	DO7.3								DO1.5	DO1.3	DO1.2
F	NC	NC	DO7.7								DO1.1	DO1.0	DO0.0
G	DO6.6	NC	DO6.7				Top View				DO0.2	DO1.0	DO0.1
H	DO6.5	DO6.4	VDD								DO0.6	DO0.5	DO0.4
J	GND	DO6.3	DO6.1								DO2.0	GND	DO0.7
K	DO6.2	DO6.0	CI2								DI0	DO2.1	VDD
L	CI0	CI3	CI5	DO4.6	DO4.3	WE	VDD	DO2.7	TOUT	DI4	DI3	DO2.3	DO2.2
M	CI1	CI6	$\overline{\text{ALL LINES}}$	DO4.4	DO4.1	CI7	$\overline{\text{TEST}}$	CLK	DO2.5	DI7	GND	DI2	DI1
N	CI4	DO4.7	DO4.5	DO4.2	DO4.0	$\overline{\text{FLUSH}}$	GND	SHIFT/$\overline{\text{HOLD}}$	DO2.6	DO2.4	DI6	DI5	VDD

Application Examples

Recommended Application in a Video System



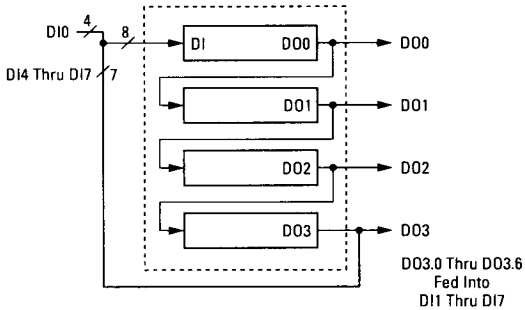
Example No. 1: L64210 Configured for 4-Bit Operation Eight Individual 1 K x 4 Shift Registers



Output of Shift Register	Data Output Pins
0	DO0.0...DO0.3
1	DO1.0...DO1.3
2	DO2.0...DO2.3
3	DO3.0...DO3.3
4	DO0.4...DO0.7
5	DO1.4...DO1.7
6	DO2.4...DO2.7
7	DO3.4...DO3.7

Application Examples
(Continued)

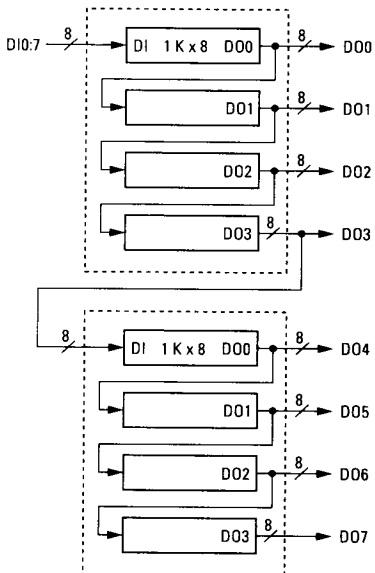
Example No. 2: L64210 Set-Up for Binary Operation
32 Individual 1 K x 1 Shift Registers



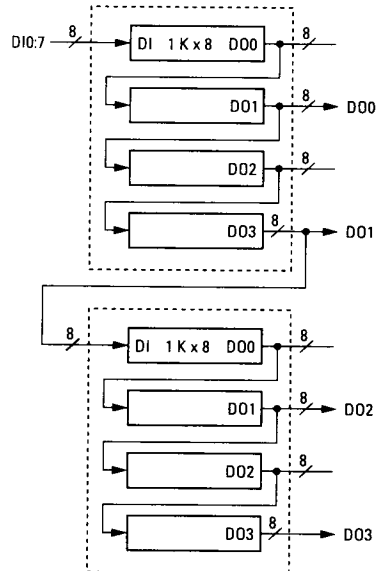
Output of Shift Register	Data Output Pins
0	DO0.0
1	DO1.0
2	DO2.0
3	DO3.0
4	DO0.1
*	*
*	*
*	*
29	DO1.7
30	DO2.7
31	DO3.7

Application Examples
(Continued)

Example No. 3: Expansion to Larger Shift Registers. Eight 1 K x 8 Shift Registers Using Two L64210s

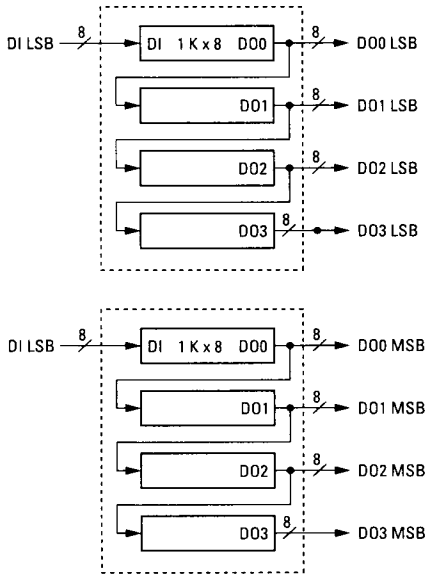


Example No. 4: Expansion to Larger Shift Registers. Four 2 K x 8 Shift Registers Using Two L64210s



Application Examples
(Continued)

Example No. 5: Expansion to Larger Shift Registers.
Four 1 K x 16 Shift Registers Using Two L64210s



Packaging

68-pin Plastic Leaded Chip Carrier: See MC Package in Package Selector Guide
68-pin Ceramic Pin Grid Array: See FB Package in Package Selector Guide
120-pin Ceramic Pin Grid Array: See FD Package in Package Selector Guide
120-pin Plastic Pin Grid Array: See ND Package in Package Selector Guide

Ordering Information

L64210
L64211 G M -XX

- -XX: Speed in MHz
- M: Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to +125°C), Processed to MIL-STD-883C Level B
- G: Package Code
  - G = Ceramic Pin Grid Array
  - N = Plastic Pin Grid Array
  - J = Plastic Leaded Chip Carrier
- L64210/L64211: Device Type
  - Video Shift Register