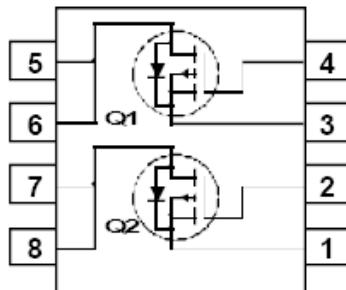
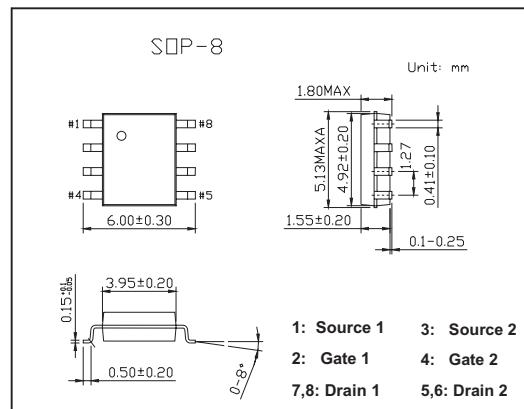


Dual 30V P-Channel PowerTrench MOSFET

KDS4953

■ Features

- -5 A, -30 V, $R_{DS(ON)} = 55\text{m}\Omega$ @ $V_{GS} = -10\text{V}$
 $R_{DS(ON)} = 95\text{m}\Omega$ @ $V_{GS} = -4.5\text{V}$
- Low gate charge(6nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Fast switching speed



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

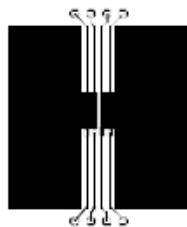
Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-30	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current Continuous (Note 1a)	I_D	-5	A
Drain Current Pulsed		-20	A
Power Dissipation for Single Operation (Note 1a)	P_D	2	W
Power Dissipation for Single Operation (Note 1b)		1.6	
Power Dissipation for Single Operation (Note 1c)		1	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40	$^\circ\text{C}/\text{W}$

KDS4953■ Electrical Characteristics $T_a = 25^\circ\text{C}$

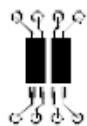
Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{BDSS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta V_{BDSS}}{\Delta T_J}$	$I_D = -250 \mu\text{A}$, Referenced to 25°C		-23		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$		-1		μA
Gate-Body Leakage, Forward	I_{GSSF}	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$		100		nA
Gate-Body Leakage, Reverse	I_{GSSR}	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$		-100		nA
Gate Threshold Voltage(Not 2)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1	-1.7	-3	V
Gate Threshold Voltage Temperature Coefficient(Not 2)	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	$I_D = -250 \mu\text{A}$, Referenced to 25°C		4.5		$\text{mV}/^\circ\text{C}$
Static Drain-Source On-Resistance(Not 2)	$R_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$	46	55		$\text{m}\Omega$
		$V_{GS} = -4.5 \text{ V}, I_D = -3.3 \text{ A}$	70	95		
		$V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}, T_J = 125^\circ\text{C}$	63	85		
On-State Drain Current	$I_{D(on)}$	$V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$	-20			A
Forward Transconductance	g_{FS}	$V_{DS} = -5 \text{ V}, I_D = -5 \text{ A}$		10		S
Input Capacitance	C_{iss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$		528		pF
Output Capacitance	C_{oss}			132		pF
Reverse Transfer Capacitance	C_{rss}			70		pF
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 \text{ V}, I_D = -1 \text{ A}, V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$ (Note 2)		7	14	ns
Turn-On Rise Time	t_r			13	24	ns
Turn-Off Delay Time	$t_{d(off)}$			14	25	ns
Turn-Off Fall Time	t_f			9	17	ns
Total Gate Charge	Q_g	$V_{DS} = -15 \text{ V}, I_D = -5 \text{ A}, V_{GS} = -5 \text{ V}$ (Note 2)		6	9	nC
Gate-Source Charge	Q_{gs}			2.2		nC
Gate-Drain Charge	Q_{gd}			2		nC
Maximum Continuous Drain-Source Diode Forward Current	I_s				-1.3	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}, I_s=-1.3\text{A}$ (Note 2)		-0.8	-1.2	V

Notes:

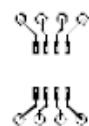
1. R_{eJK} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{eQJ} is guaranteed by design while R_{eQA} is determined by the user's board design.



a) $78^\circ\text{C}/\text{W}$ when mounted on a 0.5in^2 pad of 2 oz copper



b) $125^\circ\text{C}/\text{W}$ when mounted on a 0.02 in^2 pad of 2 oz copper



c) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%