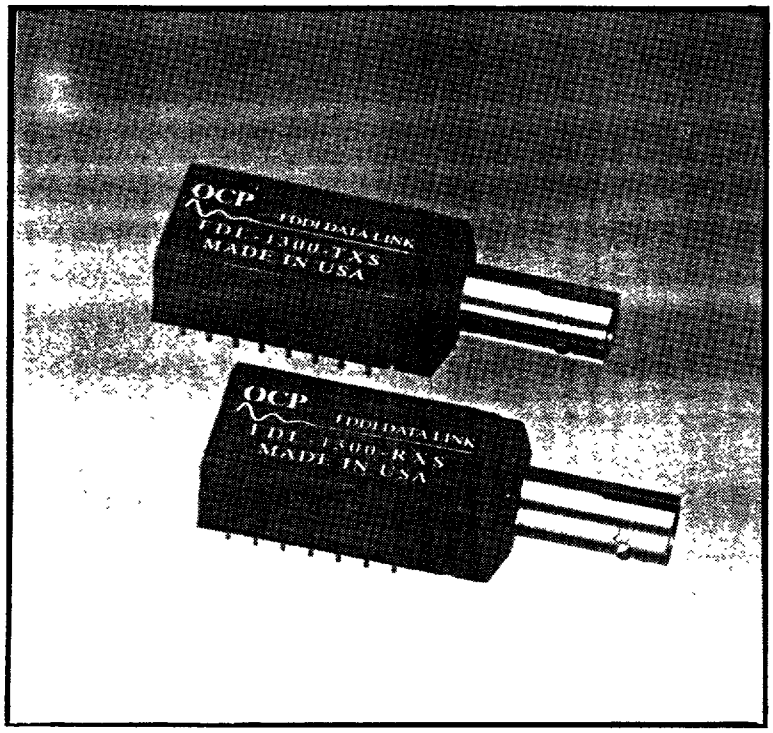
OCP

T-41-91

FDL-1300-S and FDL-1300-SA

Data Link Modules for FDDI



Features

- ☐ *Full FDDI Compliance*
- ☐ *Integral ST™ Optical Connector*
- ☐ *Single Supply Voltage (+5 V or -5.2 V)*
- ☐ *Standard 16 Pin Footprint*
- ☐ *Model FDL-1300-S is Pinout Compatible with DTL-1300*
- ☐ *Model FDL-1300-SA is Pinout Compatible with AT&T ODL-125*
- ☐ *Dual-in-Line Conductive Plastic Package*
- ☐ *0°C to +70°C Operating Temperature Range*

FDDI Applications

The FDL-1300 Fiber Optic Transmitter and Receiver Data Link Set is designed to meet or exceed all the requirements of the Physical Layer Medium Dependent (PMD) specification for the Fiber Distributed Data Interface (FDDI). Highly reliable 1300 nm surface-emitting LEDs selected for proper rise/fall time, center wavelength and spectral width are utilized in the transmitters. The receivers incorporate an InGaAs/InP PIN photodiode and a high speed transimpedance amplifier to meet the sensitivity and dynamic range requirements of FDDI. The receiver post- amplifier features the specified Signal Detect function and differential emitter coupled logic (ECL) outputs. Both the FDL-1300-S and FDL-1300-SA transmitters and receivers are housed in a cost-effective 16-pin dual-in-line conductive plastic package with integral ST™ connector and operate on standard +5 volt or -5.2 volt power supply.

The FDL-1300-S transmitter and receiver are pin compatible with the DTL-1300 and LDL-1300 Data Link Modules from Optical Communication Products, Inc.The FDL-1300-SA transmitter and receiver are pin compatible with the ODL-125 Data Link Modules from AT&T.

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Transmitter Operation

The transmitter behaves logically as a differential input gate which controls a 1300 nm light emitting diode. When the DATA input voltage is greater than the $\overline{DATA}$ input voltage, the LED is ON. When the $\overline{DATA}$ signal is greater than the DATA input voltage, the LED is OFF. In a single-ended application, the unused input pin should be connected to reference voltage V_{BB} or biased to V_{CC} - 1.29 volts.

Receiver Operation

The receiver converts optical energy to a photocurrent using a high performance PIN photodiode. The photocurrent is converted to a proportional analog voltage by a transimpedance amplifier. This low level analog signal is amplified by additional gain stages and processed through a shaping filter and a comparator to generate the differential ECL output signals. Both outputs (DATA and $\overline{DATA}$) are open emitters requiring termination to V_{CC} -2 volts with 50 ohms or to V_{EE} with 510 ohms. For optimum performance both outputs should be terminated identically, even if only one output is used.

The Signal Detect circuit monitors the level of incoming optical signal and outputs a logic LOW signal when insufficient photocurrent is produced to ensure proper operation. The Signal Detect can be used to control an external squelch circuit to gate off spurious outputs generated by the receiver when no optical input is available. The outputs are open emitter ECL requiring termination (510 ohms to V_{EE} is recommended).

Data Encoding

The receiver circuit utilizes capacitive interstage coupling which limits the permissible duty cycle variations in the serial data. A DC balanced optical signal generated by a scrambling or encoding circuit is optimal for this type of data link. Unrestricted NRZ or bursty transmissions require special precautions.

PCB Layout Considerations

The differential inputs to the transmitter and the differential outputs from the receiver are high speed emitter coupled logic signals. Printed circuit board interconnections should be configured in accordance with ECL design rules. The *MECL System Design Handbook* from Motorola, Inc. is an excellent reference. Board layouts created by CAD autorouting techniques should be reviewed carefully. Special care should be taken with the receiver, since it is a very sensitive analog device. If the receiver outputs drive long traces or multiple loads, the use of an ECL buffer gate to isolate the receiver from transmission line reflections is recommended. A solid ground plane and low impedance power supply traces are highly recommended.

EMI Susceptibility

The transmitter power supply leads should be bypassed with RF quality capacitors (0.1microfarad) close to the package. Recommended power supply filtering circuits for the receiver are shown elsewhere in this document.

The receiver circuit contains sensitive analog circuitry and is housed in a conductive plastic package. While shielding is provided , it is recommended that the receiver be located away from strong sources of radiated EMI.

Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+100	°C
Operating Temperature	-40	+85	°C
Supply Voltage	0	+6.0	V
Input Voltage	0	+6.0	V
Lead Soldering	-	240 °C, 10 sec	-

Electrical Performance Characteristics (Over Temperature Range 0°C to +70°C)

Transmitter Electrical Interface

Parameter		Symbol	Minimum	Typical	Maximum	Units
Supply Voltage[1]	+5 V	V_{CC}	4.75	5.0	5.25	V
	-5.2 V	V_{EE}	-5.25	-5.0	-4.75	V
Supply Current		I	-	110	135	mA
Power Dissipation		P	-	550	700	mW
Input HIGH Voltage (Data/$\overline{\text{Data}}$)		V_{IHS}	V_{CC} -1.15	-	V_{CC} -0.73	V
Input LOW Voltage (Data/$\overline{\text{Data}}$)		V_{ILS}	V_{CC} -1.87	-	V_{CC} -1.45	V
Differential Input Voltage		V_{DIF}	0.3	-	1.1	V
Input Common Mode Voltage [2]		V_{ICM}	-	-	1.0	V
Reference Voltage		V_{BB}	V_{CC} -1.39	V_{CC} -1.29	V_{CC} -1.17	V

[1] These modules are designed for FDDI compliance with $|V_{CC} - V_{EE}|$ = 5.0 *volts* ±5% .These modules will operate with an ECL -5.2 volt ±10% power supply, but minor deviations from FDDI requirements may occur.
[2] Permissible ± V_{ICM} with respect to V_{BB}.

Receiver Electrical Interface

Parameter		Symbol	Minimum	Typical	Maximum	Units
Supply Voltage[1]	+5 V	V_{CC}	4.75	5.0	5.25	V
	-5.2 V	V_{EE}	-5.25	-5.0	-4.75	V
Supply Current		I	-	55	65	mA
Power Dissipation		P	-	275	350	mW
Output HIGH Voltage		V_{OH}	V_{CC} -1.035	-	V_{CC} -0.88	V
Output LOW Voltage		V_{OL}	V_{CC} -1.83	-	V_{CC} -1.62	V

[1] These modules are designed for FDDI compliance with $|V_{CC} - V_{EE}|$ = 5.0 *volts* ±5% .These modules will operate with an ECL -5.2 volt ±10% power supply, but minor deviations from FDDI requirements may occur.

Optical Performance Characteristics

Transmitter Performance (Over Operating Temperature Range 0°C to +70°C)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Rate	B	DC	125	130	Mb/s
Optical Output Power	$\overline{P}_o$	-19.0	-16.0	-14.0	dBm
Center Wavelength[1]	λ_c	1270	1320	1380	nm
Rise Time (10% to 90%)[1]	t_r	0.6	-	3.5	ns
Fall Time (90% to 10%)[1]	t_f	0.6	-	3.5	ns
Random Jitter (p-p)	RJ	0	-	0.70	ns
Duty Cycle Distortion (p-p)	DCD	0	-	0.6	ns
Data Dependent Jitter (p-p)	DDJ	0	-	0.6	ns
Extinction Ratio (P_{off}/P_{on}) x 100%	-	-	-	10	%
Transmit OFF Power	P_{off}	-	-	-45.0	dBm
Spectral Width[1]	$\Delta\lambda$	-	150	-	nm

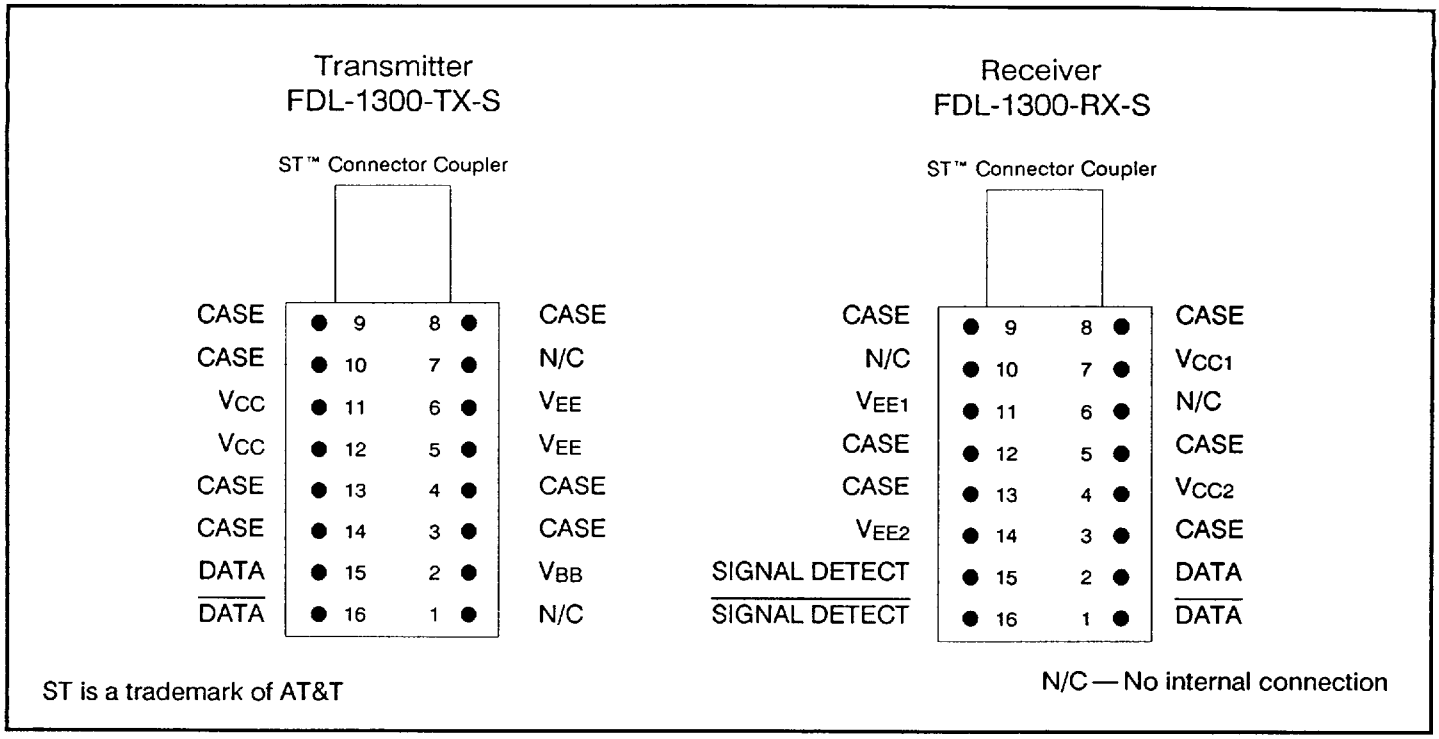
[1] Center wavelength, spectral width, and rise/fall time are compliant with Figure 5.1 of the FDDI PMD.

Receiver Performance (Over Operating Temperature Range 0°C to +70°C)

Parameter		Symbol	Minimum	Typical	Maximum	Units
Data Rate		B	1	125	130	Mb/s
Optical Input Power ($BER = 2.5 \times 10^{-10}$)	FDDI Test[1]	$\overline{P}_{in}$	-32.0	-33	-14.0	dBm
	Sensitivity[2]		-33.5	-34.5		
Signal Detect Thresholds	Assertion	P_{sd}	-	-	-31.0	dBm
	Deassertion		-45.0	-		
Signal Detect Hysteresis			1.5	-		dB
Signal Detect Timing	Assertion	T_{sd}	-	-	100	μs
	Deassertion		-	-	350	
Wavelength of Operation		λ	1100	1320	1600	nm
Output Duty Cycle Distortion (p-p)		DCD	-	-	0.4	ns

[1] FDDI Test Conditions.
[2] When tested with 2^7-1 PRBS with 50% duty cycle, optical rise/fall time of 2.5 nsec, and optimum sampling point at 125 Mbaud.

FDL-1300-S Pin Assignments (Top View)



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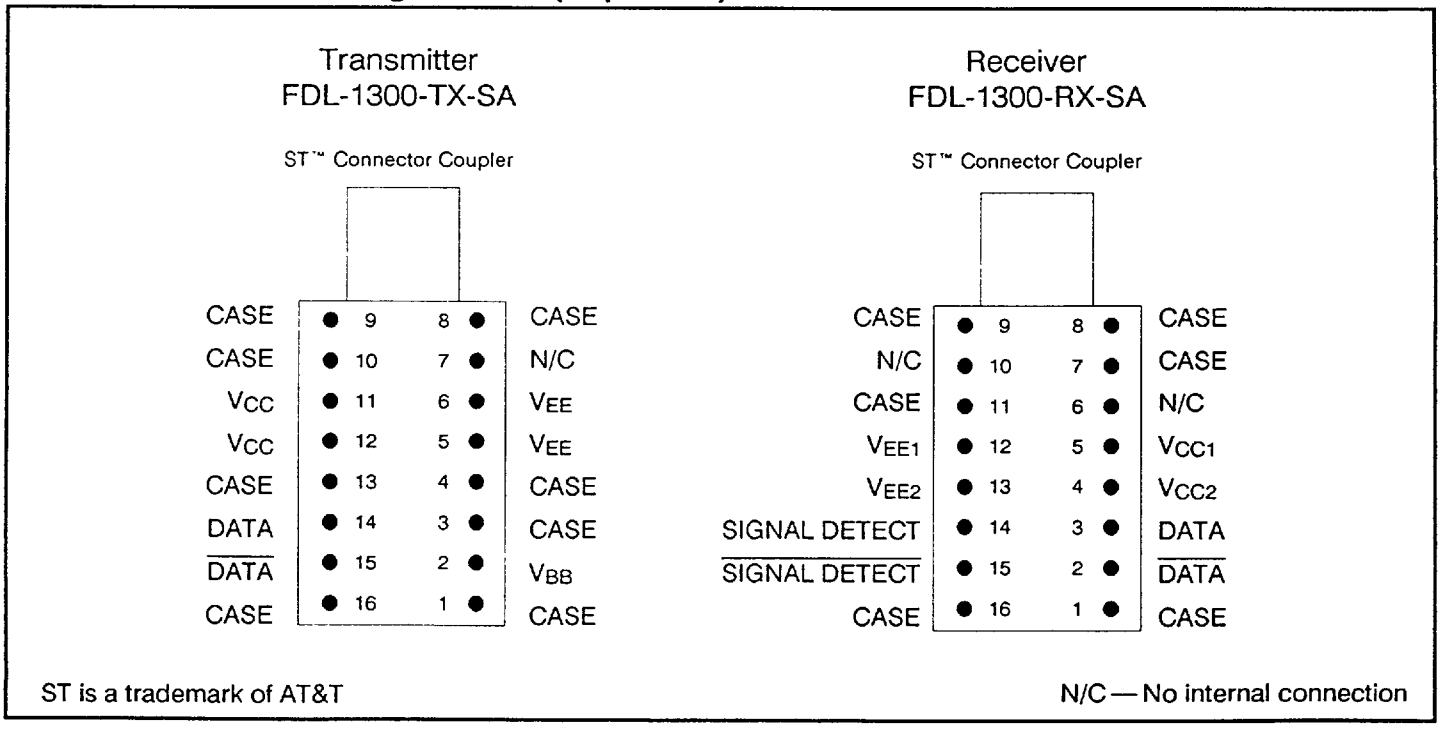
N/C — No internal connection

FDL-1300-SA Pin Assignments (Top View)



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N/C — No internal connection

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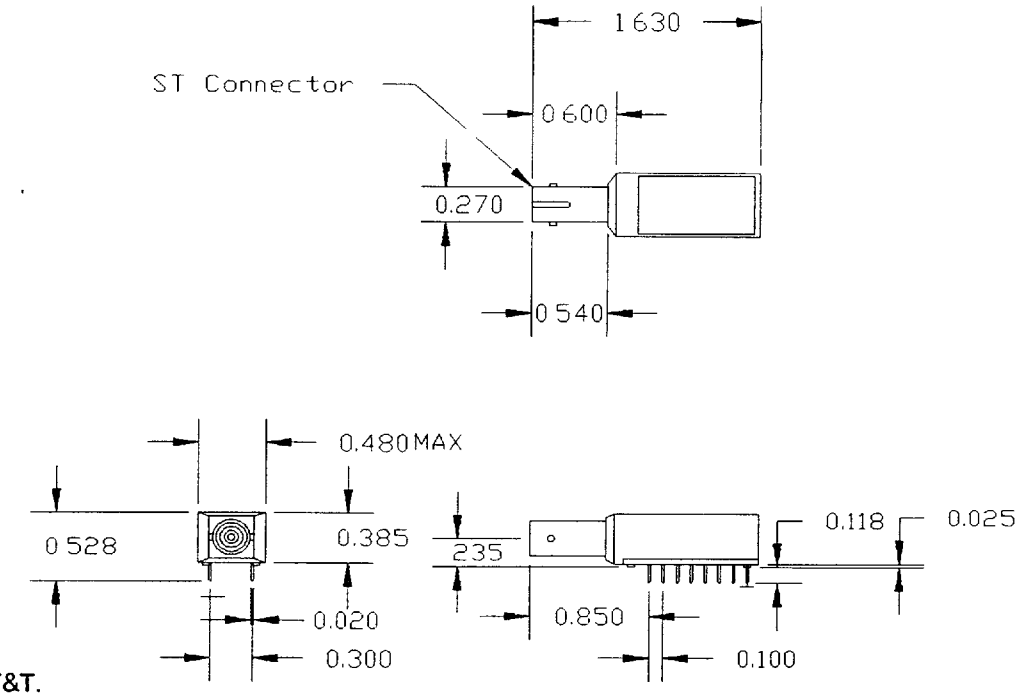
FDL-1300-S and FDL-1300-SA Outline Drawing



Dimensions in inches
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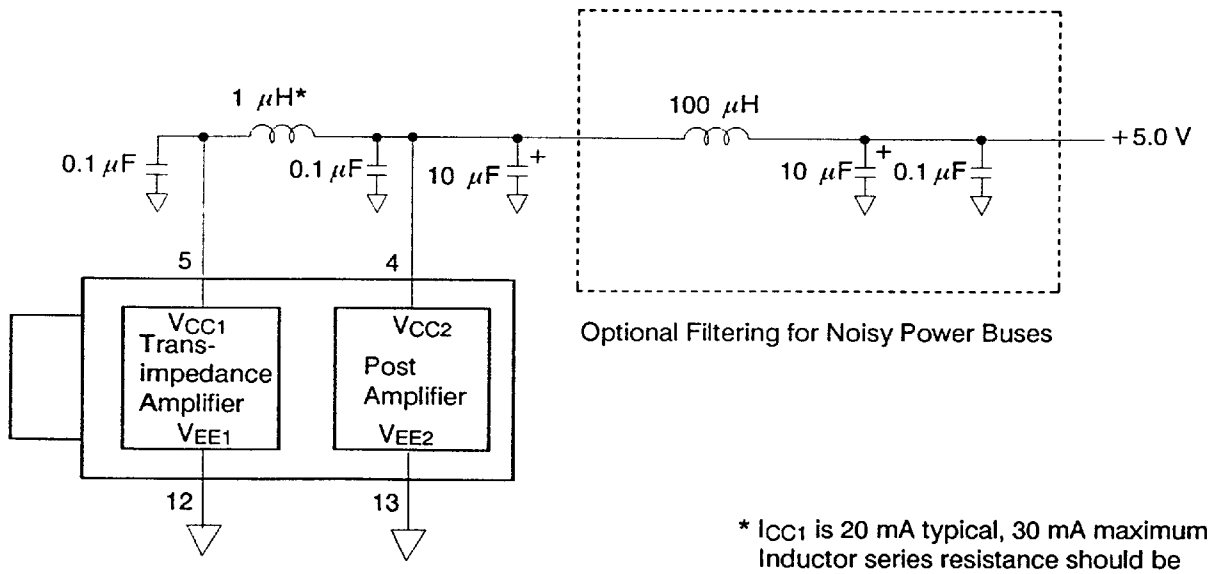
The package provides molded-in standoffs to allow for proper cleaning beneath the part after soldering. Parts are shipped with a protective cap to protect the optical interface during attachment to the printed circuit boards.

FDL-1300-RX-SA Recommended De-Coupling Circuit for +5 V Operation

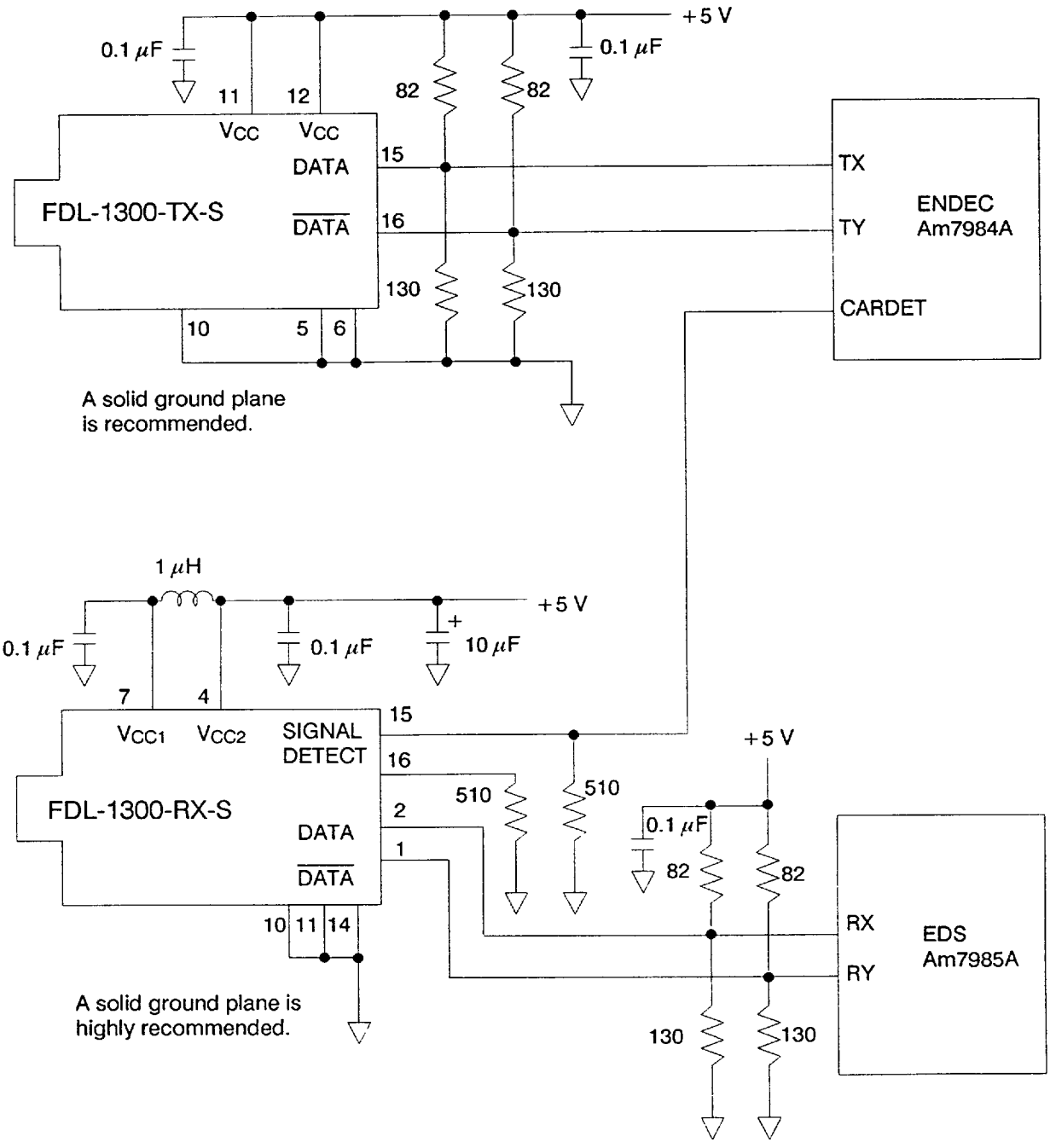


All case pins should be grounded.

* I_{CC1} is 20 mA typical, 30 mA maximum. Inductor series resistance should be 0.5 ohms or less.

Connections with AMD Supernet™ Chip Set

Transmitter and Receiver printed circuit board traces for DATA/$\overline{\text{DATA}}$ should conform to ECL design rules.



All case pins should be grounded.
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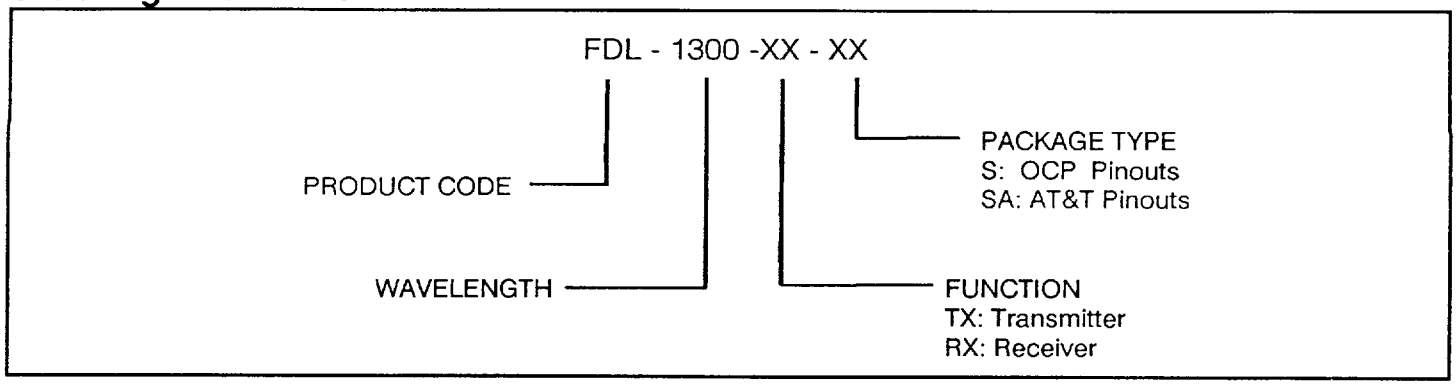
Ordering Information



HANDLING PRECAUTIONS

Normal handling precautions for electrostatic-sensitive devices should be taken.

PRELIMINARY DATA

This data sheet contains preliminary data. Supplementary data will be published at a later date. Optical Communication Products, Inc. reserves the right to make changes at any time without notice.

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