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RS data

High speed opto-isolators 6N137 and Dual 6N137

T-41-83

Stock numbers 304 – 273 and 302 – 104

The 6N137 consists of a Ga As P input diode optically coupled to a unique integrated detector comprising a photodiode, high gain linear amplifier and Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.
The internal isolator design provides maximum DC and AC circuit isolation between input and output whilst achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt V_{cc} applied to the detector. The isolation and coupling is achieved with a typical propagation delay of 45ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 25ns typical (single version only).
The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.
The Dual 6N137 is equivalent to the HCPL-2630.

Features

- LSTTL/TTL compatible: 5V supply
- Ultra high speed typically 10M bit/s (NRZ)
- Low input current required
- High common mode rejection
- Guaranteed performance over temperature range
- 3000 Vdc withstand test voltage
- Enable input available (single type only)

Absolute maximum ratings

(No derating required up to 70°C). Where two figures are given (e.g. 20/15) the first is for single version, the second for dual version.

Operating Voltage Range — 4.5 to 5.5V (7V 1 Minute Maximum)
Storage Temperature — −55°C to + 125°C
Operating Temperature — 0°C to + 70°C
Lead Solder Temperature — 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current — 40/30mA (≤ 1msec duration)
Average Forward Input Current — 20/15mA
Reverse Input Voltage — 5V
Enable Input Voltage — 5.5V (Not to exceed V_{cc} by more than 500mV)
Output Current — 50/16mA
Output Collector Power Dissipation — 85/60mW
Output Voltage — 7V

Electrical characteristics T_A = 0 to + 70°C, V_{cc} = 4.5 to 5.5V unless otherwise stated

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Note
Input Current, Low Level	I_{FL}		0	—	250	μA	
Input Current, High Level	I_{FH}		6.3	—	15	mA	5
High Level Output Current	I_{OH}	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA, V_E = 2.0V		50	250	μA	
Low Level Output Voltage	V_{OL}	V_{CC} = 5.5V, I_F = 5mA, V_{EH} = 2.0V, I_{OL}(Sinking) = 13mA		0.5	0.6	V	
High Level Enable Voltage	V_{EH}		2.0		V_{CC}	V	
High Level Enable Current	I_{EH}	V_{CC} = 5.5V, V_E = 2.0V		−1.0		mA	
Low Level Enable Voltage (Output High)	V_{EL}		0		0.8	V	
Low Level Enable Current	I_{EL}	V_{CC} = 5.5V, V_E = 0.5V		−1.6	−2.0	mA	
High Level Supply Current (per channel)	I_{CCH}	V_{CC} = 5.5V, I_F = 0, V_E = 0.5V		7	15	mA	
Low Level Supply Current (per channel)	I_{CCL}	V_{CC} = 5.5V, I_F = 10mA, V_E = 0.5V		13	18	mA	
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity = 45%, T_A = 25°C, t = 5s, V_{I-O} = 3000Vdc			1.0	μA	1
Resistance (Input-Output)	R_{I-O}	V_{I-O} = 500V, T_A = 25°C		10^{12}		Ω	1
Capacitance (Input-Output)	C_{I-O}	f = 1MHz, T_A = 25°C		0.6		pF	1
Input Forward Voltage	V_F	I_F = 10mA, T_A = 25°C		1.5	1.75	V	2
Input Reverse Breakdown Voltage	BV_R	I_R = 10μA, T_A = 25°C	5			V	
Input Capacitance	C_{IN}	V_F = 0, f = 1MHz		60		pF	
Current Transfer Ratio	CTR	I_F = 5.0mA, R_L = 100Ω		700		%	3
Fan Out (TTL Load)	N	V_{CC} = 5.5V			8		

**All typical values are at V_{cc} = 5V, T_A = 25°C

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Switching characteristics at $T_A = 25°C$, $V_{CC} = 5V$

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Note
Propagation Delay Time to High Output Level	t_{PLH}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$		45	75	ns	
Propagation Delay Time to Low Output Level	t_{PHL}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$		45	75	ns	
Output Rise-Fall Time (10-90%)	t_r, t_f	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$		25		ns	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$, $V_{EH} = 3.0V$, $V_{EL} = 0.5V$		25		ns	
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$, $V_{EH} = 3.0V$, $V_{EL} = 0.5V$		15		ns	
Common Mode Transient Immunity at Logic High Output Level	CM_H	$V_{CM} = 10V$, $R_L = 350\Omega$, V_O(min.) = 2V, $I_F = 0mA$,		50		V/μs	4
Common Mode Transient Immunity at Logic Low Output Level	CM_L	$V_{CM} = 10V$, $R_L = 350\Omega$, V_O(max.) = 0.8V, $I_F = 5mA$,		−150		V/μs	4

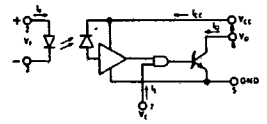
NOTES:

1. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5,6,7 and 8 shorted together.
2. At 10mA V_F decreases with increasing temperature at the rate of 1.6mV/°C.
3. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
4. Common mode transient immunity in Logic High Level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low Level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
5. 6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Figure 1
Pin connections

(a) 6N137 (b) Dual 6N137

Figure 2
Internal schematic



NOTE:
A 0.01 to 0.1uF bypass capacitor must be connected between pins 8 and 5.

TRUTH TABLE
(Positive Logic)

Input V_F	Enable V_E	Output V_O
H	H	L
L	H	H
H	L	H
L	L	H

Typical Characteristics

Figure 3
Opto-isolator Collector characteristics

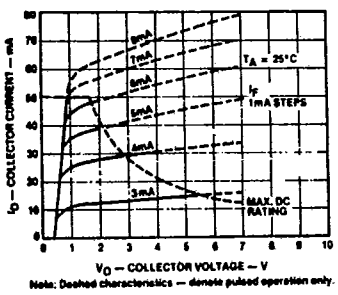


Figure 4
Input Diode Forward characteristics

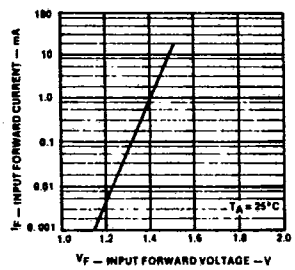


Figure 5
Output Current, I_{OH} vs. Temperature

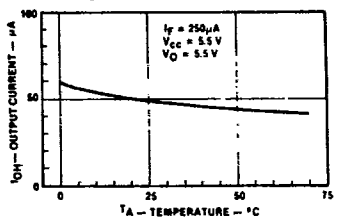


Figure 6 **Input-Output characteristics**

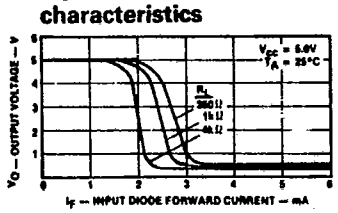


Figure 7 **Output Voltage, V_{OL} vs. Temperature and Fan-Out.**

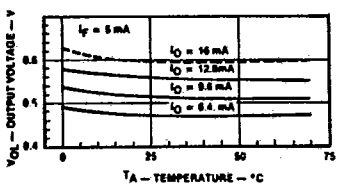
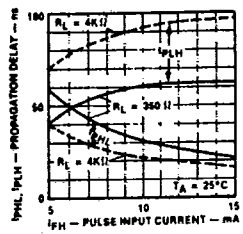


Figure 8 **Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.**



Definitions

Logic Convention. The 6N137 is defined in terms of positive logic.

Bypassing. A ceramic capacitor (.01 to 0.1μF) should be connected from pin 8 to pin 5 (Figure 15). Its purpose is to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20mm.

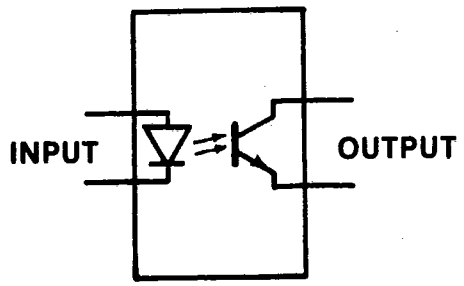
Polarities. All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Enable Input. No external pull-up required for a logic 1, i.e., can be open circuit.

Phototransistor vs Integrated Detector

A common type of optically coupled isolator (Figure 9) uses a phototransistor for a detector where the transistor provides the gain necessary to interface with logic circuits. The major problem with this phototransistor isolator is bandwidth. This is due to the fact that both the detection of the photons and the amplification of the resulting photo current occur in the same physical structure in the phototransistor. The large feedback capacitance between the collector and the base is what essentially limits the phototransistor bandwidth.

Figure 9 **Phototransistor isolator**



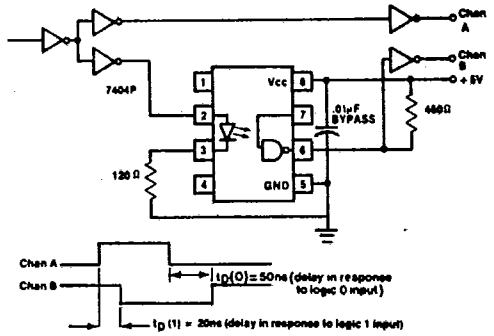
The 6N137 design greatly reduces this bandwidth limitation by proper optimization of the detector. The detector element is a monolithic structure, consisting of a photodiode, which collects the light; and a linear high speed amplifier (Fig. 2), which amplifies the resultant photo current. Functional separation of the photodiode from the amplifier reduces feedback capacitance to less than 1pF, thus making possible bandwidths up to 20MHz. The device, in detail, consists of a gallium arsenide phosphide input diode and a monolithically integrated detector at the output. The detector comprises a photodiode followed by a linear amplifier which drives a Schottky clamped output transistor. This output circuit is temperature, voltage, and current compensated to be truly compatible with standard TTL and DTL circuits. It also has a DTL/TTL compatible strobing input; with logic '0' at the strobe input, the output is held at logic '1', regardless of input conditions at the gallium arsenide phosphide diode. The basic features of the 6N137 are compared to phototransistor types in Table 1.

TABLE 1			
Isolator Types	**Bandwidth BW**	**Propagation Delay**	**Common Mode Rejection**
6N137 (IC Compatible Optical Isolated Gate)	20 MHz (Data Rate)	60ns	10V/10MHz
Phototransistor Types	100 kHz	6μs	3V/1MHz

TTL interfacing

The 6N137 is TTL (also DTL) compatible at both input and output requiring only 5mA input current to sink 13mA at the output — that is, it has 8-gate fan-out capability at 5mA input. The device interfacing with TTL inverters is demonstrated in Figure 10, the circuit for testing response delays. The inverting mode achieves the best speed performance, with typical delays of 20ns and 50ns. The current limiting resistor in series with the input diode is 120Ω, allowing approximately 10 mA of current to flow in on the 'on' state. The output load resistor is only 450Ω– due to the greater sinking capability of the output transistor.

Figure 10 **Response delay between TTL gates**



The input diode turn-on delay time of the 6N137 is a function of the input charging time. This delay time is most easily improved by simply adding a capacitor in parallel with the input current limiting resistor and operating from a low impedance source. In general, the capacitor should be a low inductance type with a value for a time constant of 15 to 30ns with the current limiting resistor. If the current limiting resistor is 100Ω, the capacitor should be 150 to 300pF.

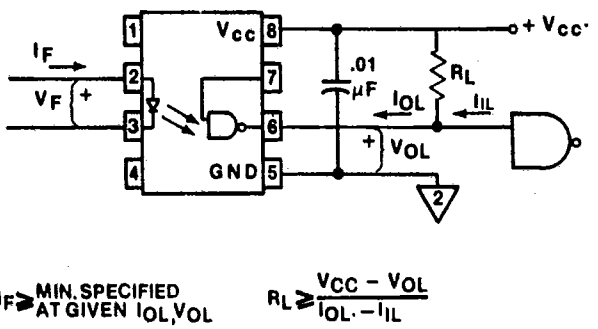
On the output side of the isolator, speed is enhanced by using the lowest possible value of pull-up resistance which is consistent with the current sinking capability of the isolator collector. The stray capacitance to ground should also be minimized. An output pull-up resistor is recommended to improve noise immunity and speed of response in moving to logic '1' output.

Line receivers

When digital data is transmitted over an appreciable length of transmission line (even less than a metre), there arises a possibility of ground shift, ground looping, etc. Opto-isolators can reduce the amount of ground loop current and the effects of the resulting common mode voltage. They are, therefore, very useful as line receivers.

Most line drivers are capable of sourcing a line voltage higher than the minimum ($\approx$ 1.5V) needed to turn "on" an opto-isolator. They usually also deliver a line current greater than the value of I_F as determined with reference to Figure 11. It is possible, of course, to design a line driver that will source the proper current and no more, but that is usually not good practice. Good practice is to drive the line with all the voltage and current available, then deal with the excess in the design of the termination of the line.

Figure 11 **Input and output considerations**



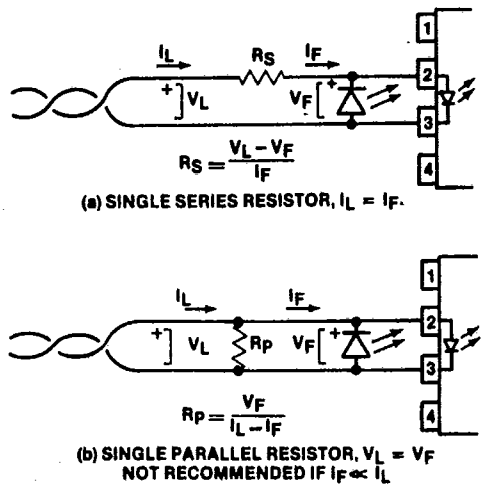
In the design of the termination, the "off" state is usually ignored unless pre-bias is used. There are usually three objectives in the design of the termination:

(A) proper "on" state I_F
(B) threshold level, I_{Fth} (to switch the output)
(C) reflections due to impedance mismatch.

Resistive Terminations

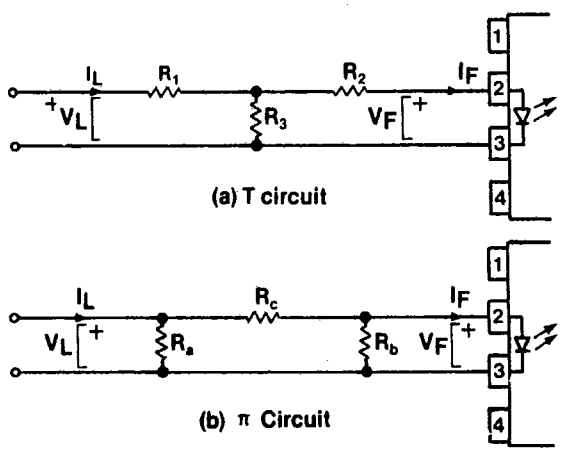
Objective (A) is mandatory; objectives (B) and (C) are discretionary. If discretion allows (B) and (C) to be neglected, the termination may be as simple as in Figure 12 requiring only a single resistor. In most cases, the series resistor termination of Figure 12 (a) would be used because it will accomodate a broader range of driver and line resistance variables. It is slower than the single parallel resistor termination of figure 12 (b) because the input diode is driven from a higher impedance. Slowness can be remedied with a peaking capacitor in parallel with R_S as previously explained; if peaking capacitance is applied, the anti-parallel diode should be used (even if the driver is polarity *non*-reversing) to allow the peaking capacitor to charge and discharge the maximum amount.

Figure 12 **Single–resistor terminations using opto-isolators as line receivers**



When, in addition to proper I_F, consideration must be given to either threshold current. I_{Fth}, or to line reflections, an additional resistor provides one additional degree of freedom. A two-resistor termination can accommodate the additional objective of either setting the I_{Fth} level or of approximate impedance matching but not both. To satisfy all three of the design objectives requires a three resistor termination in either "π" or "T" configuration.

Figure 13 **T and π circuits**

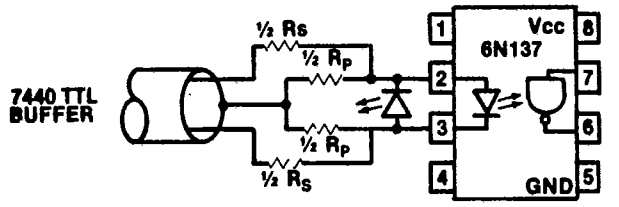


The 6N137 may be used as line receivers in either single-ended or balanced line applications. The turn-on voltage of the input diode establishes a threshold for the flow of current, thereby making the noise immunity higher than it would be for a linear line receiver. In many applications, this noise immunity is high enough that only a single-ended transmission line is required. For transmission over long distances or in very noisy environments, a balanced system should be used.

Figure 14 – demonstrates the use of the 6N137 as a balanced line receiver, using 7440 line driver. The resistor values are chosen in each case to match the line driver to the isolator line receiver. The line driver should be designed to supply more current

than the isolator input diode requires; this permits the use of a shunt resistor at the receiving end for better impedance matching and improved noise immunity. To maintain a reasonable impedance match during the negative excursion when the isolator input diode is reversed biased, a diode having about the same turn-on voltage as the input diode should be connected in reverse polarity across the input diode. For this purpose two silicon diodes in series could be used, or one LED, such as the RS standard red 0.2in LED.

Figure 14 **Typical line driver/receiver system**



Formulas for the terminating resistances are given below.

TABLE 2

	Basically	Given R_O, I_L	Given R_O, V_L	For best CMR
R_P	$\frac{V_D}{I_L - I_D}$	$\frac{V_D}{I_L - I_D}$	$R_O\left(\frac{V_D}{V_L - I_D R_O}\right)$	Connect ½RP from each side of isolator input to cable shield.
R_S	$\frac{V_L - V_D}{I_L}$	$R_O - \frac{V_D}{I_L}$	$R_O\left(1 - \frac{V_D}{V_L}\right)$	Connect ½ RS in series from each line to input terminal of isolator.

Where:

R_O – Line-to-line terminating resistor which gives least reflection.

V_L, I_L – line-to-line voltage and line current with R_O connected.

V_D, I_D – isolator input diode forward voltage and current.

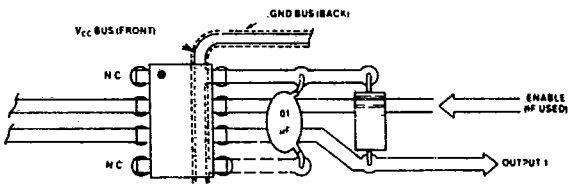
Circuit board layout

Careful attention is required for the 6N137 circuit layout due to the high gain employed in its internal amplifier. Power Supply lead lengths (Pins 5 and 8) are particularly important as their inductance provides an impedance across which a positive feedback signal may appear. A socket may be used, but it should be of a type having very short lead lengths. Proper bypassing is also essential. A total of at least 1μF of capacitance from V_{CC} to ground should be used on the board. Part of this 1μF may come from other bypasses installed to serve other circuits on the same board. In addition to the 1μF total, a bypass capacitor of 0.01μF should be connected directly from Pin 8 to Pin 5 of each 6N137 used on the board. These individual bypass capacitors must be low inductance disc ceramic. It is also important to have adequate bypassing for those circuits whose response is related to the signals produced in regenerative phase (circuit feedback) with variations in the V_{CC} line voltage. If the common practice of having 1μF for each two circuits is adopted, there should be no problem, and much less bypassing will ordinarily suffice.

Common mode decoupling

Common mode decoupling can be significantly enhanced by running a ground trace midway between the rows of isolator terminals. This trace is, of course, connected to the output ground (Pin 5) of the 6N137 (see Figure 15). Its purpose is to cause electric potential at the input side to be coupled to ground at the output, rather than to some signal amplifying terminal. If no socket or if in-the-board socket pins are used, this ground lead may be simply a printed trace, but if a socket is used, the ground trace should be paralleled by a piece of grounded wire running up over the socket. When the common mode voltage is very high (>1000V) the ground wire should be insulated to prevent electric discharge from the ground wire to the input terminals.

Figure 15 **Typical printed circuit board layout**



RS data

Typical applications

Ground loops involving peripheral equipment are effectively prevented by the use of optically coupled isolators. A typical situation is shown in Figure 16 in which the information on a set of BDC lines is made available at the electrically isolated outputs of the optically coupled isolators.

Although the use of the enable feature of the 6N137 is not always required, strobing of the enable inputs improves propagation delay times and helps to eliminate the change-of-state glitches that are sometimes present on BCD and other word lines. When the enable inputs are held at logic '0' (low) the outputs will all be at logic '1' (high). When the enable inputs are high, the outputs will be low on only those isolators whose **isolated** input is at the logic '1' state; the other outputs will remain high.

Figure 16 **Strobed optically coupled isolators**