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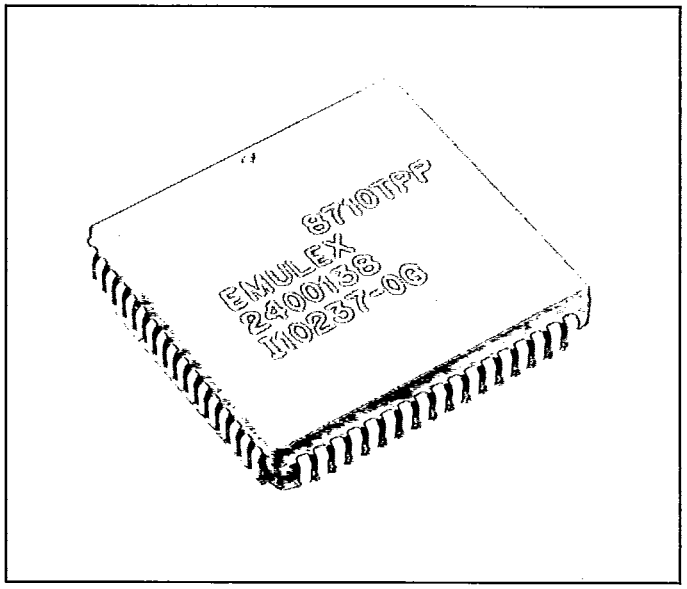
Storage

Technology

EMULEX SCSI PROCESSOR

2400138

EMULEX



ESP Chip

FEATURES

- Supports ANSI X3T9.2 SCSI standard
- Utilizes buffer controller interface for I/O and fast DMA
- Provides on-chip single-ended receivers and 48 mA drivers for SCSI bus
- Contains control logic for differential transceivers
- Generates and checks parity on SCSI bus (checking can be disabled)
- Functions as initiator or target
- Supports asynchronous SCSI bus data transfers up to 6M bytes per second depending on cable characteristics
- Supports synchronous SCSI bus data transfers up to 5M bytes per second
  - Programmable synchronous transfer period
  - Programmable synchronous transfer offsets up to 15
- Provides sixteen-byte data FIFO between the DMA and SCSI channels
- Utilizes pipelined command structure
- Implements common SCSI sequences without microprocessor intervention
  - Selection sequence, from arbitration through command
  - Reselection sequence, from arbitration through message
  - Bus-initiated selection through received command
  - Bus-initiated reselection through received message
  - Command complete sequences
  - Terminate and disconnect sequences
- Interrupts microprocessor only when service is required
  - Disconnect or bus reset
  - Selection/reselection sequence complete
  - Target mode command complete or ATN detected
  - Initiator mode command complete or phase change and REQ detected
- Supports clock rates of up to 25 MHz
- Interfaces to eight-bit microprocessor data bus with no support logic
- Low power requirements

DESCRIPTION

The Emulex SCSI Processor (ESP) chip is a VLSI device which implements the detailed protocol of the SCSI bus standard. The ESP performs such functions as bus arbitration, selection of a target, or reselection of an initiator. It handles message, command, status, and data transfers between the SCSI bus and its internal FIFO or a buffer memory.

Figure 1 shows the internal architecture of the ESP. The ESP is essentially a sophisticated sequencer. The sequencers are a collection of high- and low-level state machines that perform the various functions required by the SCSI bus and the DMA channel. The high-level state machines manage the disconnect, target, and initiator modes of operation. The low-level state machines perform the actual interface operations.

The main data paths are the buffer controller input and output data buses (BI and BO), and the SCSI input and output data buses (SDI and SDO). All are eight-bit buses. In differential mode, the SDI bus becomes bidirectional and the SDO bus controls the direction of the external differential transceivers.

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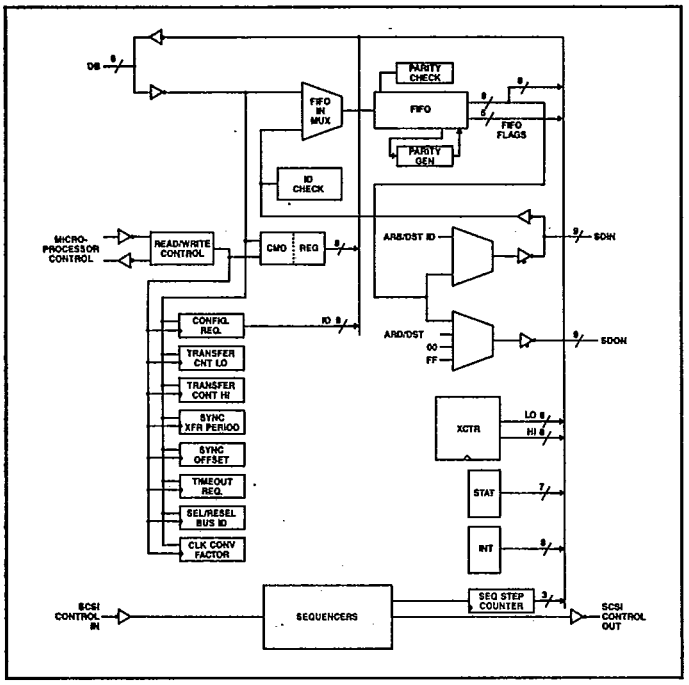

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Figure 1. ESP Block Diagram

The ESP replaces existing SCSI interface circuitry, which typically consists of discrete devices, external drivers, and a low performance SCSI interface chip. The ESP contains a fast DMA interface, a sixteen-byte FIFO, and fast asynchronous and synchronous data interface to the SCSI bus, including drivers.

The ESP has been optimized for interaction with the controller microprocessor. Common SCSI bus sequences that would typically require significant amounts of processing and interaction have been reduced to single commands. These include:

Sequence	Description
Selection	Arbitration, target selection, transmission of an optional one-byte message followed by a multiple-byte command
Reselection	Arbitration, initiator reselection, and transmission of a one-byte message

(continued)

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Sequence	Description
Bus-Initiated Selection	Selection detection, receipt of a one-byte message, command length decode and receipt of a command (if the message was IDENTIFY)
Bus-Initiated Reselection	Reselection detection and receipt of a one-byte message
Target Command Complete	Transmission of a status byte and a one-byte message
Target Terminate	Transmission of a status byte and a one-byte message followed by disconnection from the SCSI bus
Target Disconnection	Transmission of two one-byte messages followed by disconnection from the SCSI bus
Initiator Command Complete	Receipt of a status byte and a one-byte message

To further reduce overhead, the ESP contains a double-ranked Command Register and Transfer Counter which provides a transfer-command pipeline. With Emulex's Buffer Controller 2, which supports buffer setup overlap, the time lost in interbuffer overhead can be reduced to zero.

Using the ESP reduces firmware, part count, board area, and cost while enhancing system performance.

SYSTEM ORGANIZATION

Figure 2 shows a block diagram of a typical SCSI disk controller. The ESP chip provides the controller with a complete SCSI interface. The other major chips in the circuit include the Emulex Merged Architecture Controller (MAC) and a microprocessor.

The MAC chip controls data movement in and out of the buffer memory. It supports up to four DMA channels with a total throughput rate up to 4M bytes per second and provides format control for a wide spectrum of 14-, 8-, 5¼- and 3½-inch disk drives.

The 8031 microprocessor coordinates the interaction of the VLSI devices on the board. It also implements high level SCSI protocol, such as the message system, SCSI pointers, and command set.

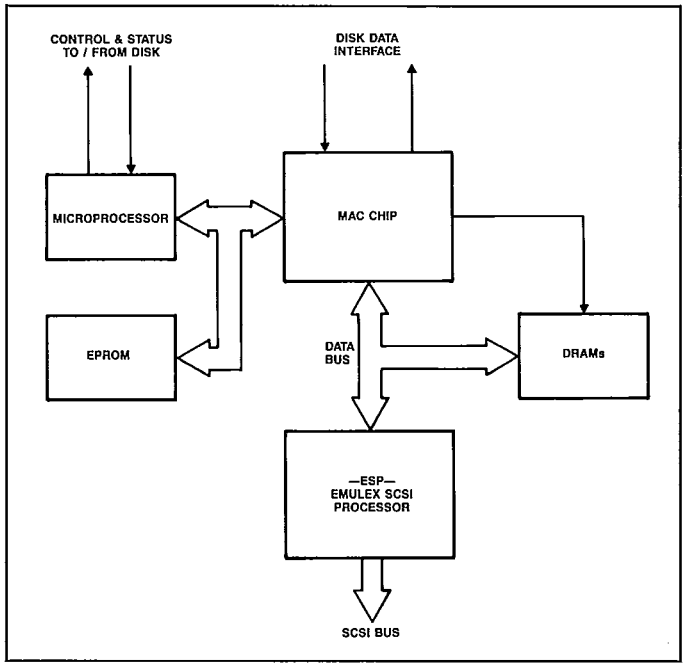

Figure 2. Typical SCSI Controller.

PACKAGING

The ESP chip is available in a 68-pin PLCC for surface or socket mounting. The Emulex part number is 2400138.

REGISTERS

The ESP has 15 registers which are used to configure, command, monitor, and pass data to the chip. These registers are shown in Figure 3 and are more fully described in the paragraphs that follow.

Transfer Count Register

This 16-bit write-only register specifies the number of bytes to be transferred during a DMA operation. Zero specifies the maximum count (65536).

FIFO Register

The FIFO is a 16-byte deep, first-in-first-out buffer between the SCSI bus and buffer memory. The controller microprocessor can access the FIFO using this register. "Writes" load to the top of the FIFO; "Reads" unload from the bottom.

Command Register

This eight-bit read/write register is used to give commands to the ESP. The register is double ranked, enabling the microprocessor to stack commands to the ESP.

The ESP's command set is listed in the following table.

Bits 654	Bits 3210	Command	Interrupt
000	0000	NOP	No
000	0001	Flush FIFO	No
000	0010	Reset chip	No
000	0011	Reset SCSI bus	No[1]
100	0000	Reconnect sequence	Yes
100	0001	Select without ATN sequence	Yes
100	0010	Select with ATN sequence	Yes
100	0011	Select with ATN and stop sequence	Yes
100	0100	Enable selection/reselection	No
100	0101	Disable selection/reselection	Yes
010	0000	Send message	Yes
010	0001	Send status	Yes
010	0010	Send data	Yes
010	0011	Disconnect sequence	Yes
010	0100	Terminate sequence	Yes
010	0101	Target command complete sequence	Yes
010	0111	Disconnect	No
010	1000	Receive message sequence	Yes
010	1001	Receive command	Yes
010	1010	Receive data	Yes
010	1011	Receive command sequence	Yes
001	0000	Transfer information	Yes
001	0001	Initiator command complete sequence	Yes
001	0010	Accept message	Yes
001	1000	Transfer pad	Yes
001	1010	Set ATN	No

[1] External connection of the RSTO pin to the RSTI pin causes an interrupt if the SCSI reset interrupt is not disabled in the Configuration Register.

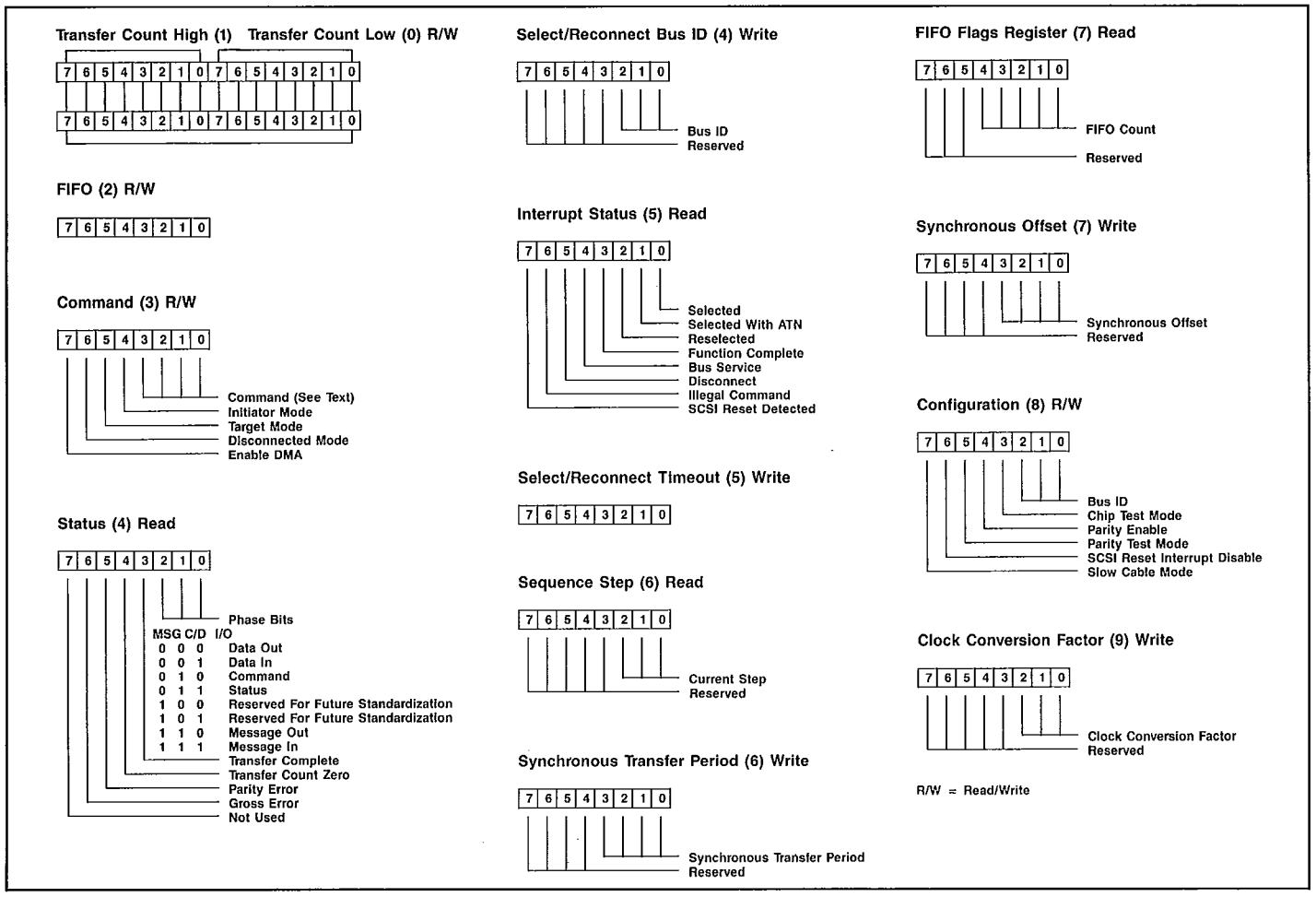

Figure 3. ESP Registers

Status Register

This eight-bit read-only register contains fields to indicate the status of the chip and to qualify the reason for an interrupt.

Bits 2 through 0 indicate the state of the SCSI MSG, C/D, and I/O signals, respectively. These bits define the information phase being asserted by the target (see Figure 3).

Select/Reconnect Bus ID Register

This three-bit write-only register specifies the destination bus ID for a select or reconnect command.

Interrupt Status Register

This eight-bit read-only register is used in conjunction with the Status Register and Sequence Counter to determine the cause of an interrupt.

Select/Reconnect Timeout Register

This eight-bit write-only register specifies the number of time units to wait for a response during selection or reselection. The value of a time unit is based on the clock applied to the ESP (CK). At 24 MHz this value is 1.7 msec, which allows an absolute timeout period of from 1.7 msec to 435 msec (1 to 255 units).

Sequence Step

This eight-bit read-only register indicates the current substep within a command sequence when an interrupt occurs.

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Synchronous Transfer Period Register

This eight-bit write-only register specifies the minimum time between leading edges of successive REQ or ACK pulses during synchronous transfers. At present, only 4 bits are actively used and the remaininng four are reserved.

FIFO Flags Register

This is a read-only register. The least significant five bits encode the 16 "FIFO full" flags to indicate the number of bytes remaining in the FIFO. The remaining bits are reserved.

Synchronous Offset Register

This four-bit write-only register specifies the maximum REQ/ACK offset allowed during synchronous transfers. An offset of zero specifies asynchronous operation.

Configuration Register

This eight-bit read/write register is used to specify different operating options for the ESP, including the ESP's SCSI bus address, parity configuration, and cable speed configuration. Slow cable mode provides longer data setup times on the SCSI bus to compensate for high capacitance on the SCSI cable.

Clock Conversion Factor Register

The microprocessor loads this three-bit write-only register with a clock conversion factor. This factor is required to run the ESP at various clock speeds while maintaining consistent SCSI interface timing. The factor used is one-half the number of clock cycles (CK) required to generate a 400 nsec period clock. For example, at 24 MHz the clock conversion factor is five.

PROCESSOR OVERHEAD

The following table shows the processor overhead required for the target to change phases during a command. Times are estimated based on using an ESP and an 8031 microprocessor running at 12 MHz.

	Change Time (usec)
Selection to ID message	<2
ID message to command	<2
* Command to Disconnect message	150
Disconnect message to bus free	<1
Reselect to ID message	<2
* ID message to data transfer	200
* Data transfer to status	120
Status to Complete message	<2
Complete message to bus free	<1
Total phase change overhead	<480
Interbuffer time for data transfers	0

* Associated with the 8031 microprocessor functions.

PIN DESCRIPTION

The ESP pins are described below. The pin type is indicated by "I" for input, "O" for output, and "I/O" for bidirectional. Figure 4 shows the ESP's pinouts.

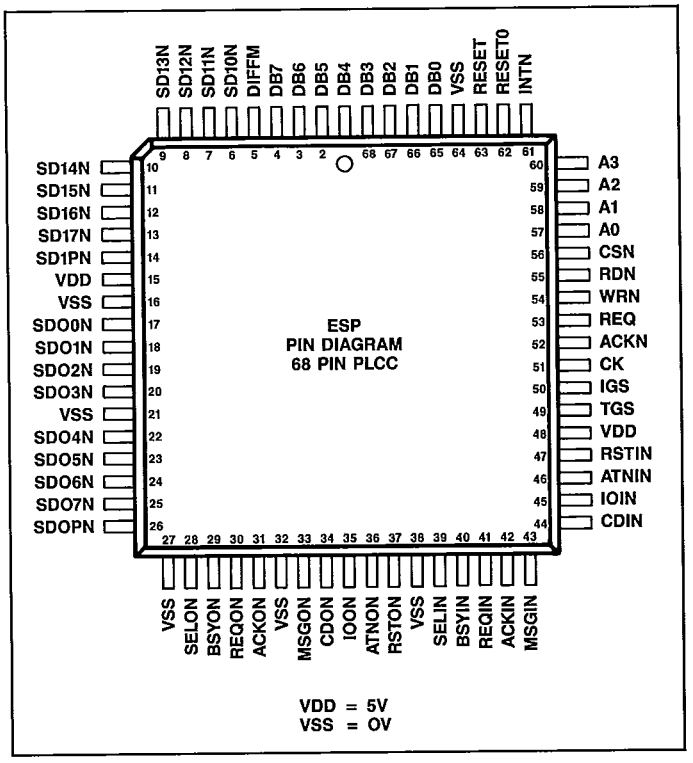

Figure 4. ESP Pinouts

Pin	Symbol	Dir.	Driver	Function
Buffer Controller Interface				
4	DB7	I/O	TTLP/TTL3	Data Bus
3	DB6	I/O	TTLP/TTL3	Data Bus
2	DB5	I/O	TTLP/TTL3	Data Bus
1	DB4	I/O	TTLP/TTL3	Data Bus
68	DB3	I/O	TTLP/TTL3	Data Bus
67	DB2	I/O	TTLP/TTL3	Data Bus
66	DB1	I/O	TTLP/TTL3	Data Bus
65	DB0	I/O	TTLP/TTL3	Data Bus
60	A3	I	TTL	Register Address
59	A2	I	TTL	Register Address
58	A1	I	TTL	Register Address
57	A0	I	TTL	Register Address
56	CSN	I	TTL	Chip Select
55	RDN	I	TTL	Read Strobe
54	WDN	I	TTL	Write Strobe
53	REQ	O	TTL3	DMA Request
52	ACKN	I	TTL	DMA Acknowledge
61	INTN	O	OD3	Microprocessor Interrupt
SCSI Bus Interface				
25	SDO7N	O	OD48	SCSI Data Bus Out
24	SDO6N	O	OD48	SCSI Data Bus Out
23	SDO5N	O	OD48	SCSI Data Bus Out
22	SDO4N	O	OD48	SCSI Data Bus Out
20	SDO3N	O	OD48	SCSIData Bus Out
19	SDO2N	O	OD48	SCSI Data Bus Out
18	SDO1N	O	OD48	SCSI Data Bus Out
17	SDO0N	O	OD48	SCSI Data Bus Out
26	SDOPN	O	OD48	SCSI Parity Out
13	SDI7N	I/O	ST/TTL3	SCSI Data Bus In
12	SDI6N	I/O	ST/TTL3	SCSI Data Bus In
11	SDI5N	I/O	ST/TTL3	SCSI Data Bus In
10	SDI4N	I/O	ST/TTL3	SCSI Data Bus In
9	SDI3N	I/O	ST/TTL3	SCSI Data Bus In
8	SDI2N	I/O	ST/TTL3	SCSI Data Bus In
7	SDI1N	I/O	ST/TTL3	SCSI Data Bus In
6	SDI0N	I/O	ST/TTL3	SCSI Data Bus In
14	SDIPN	I/O	ST/TTL3	SCSI Parity In
28	SELON	O	OD48	SCSI Select Out
29	BSYON	O	OD48	SCSI Busy Out
36	ATNON	O	OD48	SCSI Attention Out
31	ACKON	O	OD48	SCSI Acknowledge Out
30	REQON	O	OD48	SCSI Request Out
33	MSGON	O	OD48	SCSI Message Out
34	CDON	O	OD48	SCSI Control Data Out
35	IOON	O	OD48	SCSI Input/Output Out
37	RSTON	O	OD48	SCSI Reset Out
39	SELIN	I	ST	SCSI Select In
40	BSYIN	I	ST	SCSI Busy In
46	ATNIN	I	ST	SCSI Attention In
42	ACKIN	I	ST	SCSI Acknowledge In
41	REQIN	I	ST	SCSI Request In
43	MSGIN	I	ST	SCSI Message In
44	CDIN	I	ST	SCSI Control Data In
45	IOIN	I	ST	SCSI Input/Output In
47	RSTIN	I	ST	SCSI Reset In

(continued)

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Miscellaneous Pins				
50	IGS	O	TTL3	Initiator Group Select
49	TGS	O	TTL3	Target Group Select
5	DIFFM	I	TTL	Differential Mode Enable
63	RESET	I	TTL	ESP Reset
62	RESETO	O	OD4	Reset Output
51	CK	I	TTL	Clock
15	V_{DD}			+5Vdc
48	V_{DD}			+5Vdc
16	V_{SS}			Ground
21	V_{SS}			Ground
27	V_{SS}			Ground
32	V_{SS}			Ground
38	V_{SS}			Ground
64	V_{SS}			Ground

INTERFACES

The ESP has two separate interfaces: the buffer data bus and the SCSI bus.

Buffer Data Bus

The buffer data interface is used for DMA (in conjunction with a buffer controller) and to allow microprocessor access to ESP registers.

The interface consists of an eight-bit data bus (DB7-DB0), four address lines (A3-A0), a read strobe (RDN), a write strobe (WRN), DMA request (REQ), DMA acknowledge (ACKN), and microprocessor interrupt (INTN) signals.

To access an ESP register, the microprocessor presents an address on A0-A3, drives CSN true, and strobes the data in or out of the register using WRN or RDN.

For DMA operations, the buffer controller manages access timing and generates all buffer memory addresses. When a DMA operation is enabled, the ESP drives REQ true, the buffer controller acknowledges with ACKN and strobes the data into or out of the ESP with WRN or RDN.

SCSI Interface

The SCSI interface can be configured for operation in either differential mode or single-ended mode using the differential mode enable (DIFFM) pin. When DIFFM is grounded, the ESP operates in single-ended mode; when it is held high, the ESP operates in differential mode.

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Single-Ended Mode

In single-ended mode, all SCSI bus signals have separate input and output pins. That is, the ESP drives data out on SDO7-0N and receives data on SDI7-0N.

Differential Mode

In differential mode, the SDI7N-0N pins carry bidirectional data and the SDO7N-0N pins configure the direction of the external transceivers.

During arbitration, the ESP drives the SDO7-0N lines with the appropriate ID bit set, which sets the desired differential transceiver's direction to out. The other transceivers are configured for input, allowing the ESP to determine whether it has won arbitration. During selection and information transfers, the SDO7-0N lines are driven, either all high or all low, to configure the transceivers for output or input, respectively.

The other SCSI bus signals have separate input and output pins. The direction of the transceivers for ATN, ACK, REQ, MSG, C/D, and I/O is selected by the IGS and TGS outputs, which indicate whether the chip is operating in the initiator or the target role. The BSY, SEL, and RST signals are OR-tied on the SCSI bus.

Absolute Maximum Ratings (Referenced to V_{SS})			
Symbol	**Parameter**	**Limits**	**Unit**
V_{DD}	DC Supply Voltage	0.5 to +7.0	V
V_I	Input Voltage	V_{SS}-0.7 to V_{DD} +0.3	V
I_I	DC Input Current	±10	mA
T_{STG}	Storage Temperature Range (Plastic)	-40 to +125	°C
Recommended Operating Conditions			
Symbol	**Parameter**	**Range**	**Unit**
V_{DD}	DC Supply Voltage	4.75 to 5.25	V
TA	Operating Ambient Temperature Range	0 to +70	°C
CK	Rate, Asynchronous Rate, Synchronous	10 to 24 12 to 24	MHz MHz
I_{DD}	Static (all inputs at V_{SS}, all outputs floating, all bidirects configured as inputs)	10	mA
I_{DD}	Dynamic	70	mA

ESD/SCR Requirements			
Symbol	**Parameter**	**Limits**	**Unit**
ESP	Electrostatic Discharge (100 pF via 1500 ohms)	1500	V
IMAX	Current into or out of any pin (25°C, V_{DD} -V_{SS} = 5 V)	50	mA

DC Electrical Characteristics

Specified at V_{DD} = 5V ±5% over the temperature of 0 to +70°C					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Condition**
TTL: TTL Input					
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
I_{IH}	Input High Current	0	20	µA	V_{IN} = V_{DD}
I_{IL}	Input Low Current	0	-100	µA	V_{IN} = 0 V
TTLP: TTL Input With Pullup					
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
I_{IH}	Input High Current	0	20	µA	V_{IN} = V_{DD}
I_{IL}	Input Low Current	0	-400	µA	V_{IN} = 0 V
TTL3: TTL 3.2 mA Output					
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -80 µA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3.2 mA
OD3: 3.2 mA Open Drain Output					
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3.2 mA
I_{ZL}	High Z Leakage	-20	20	µA	V_O = 0V or V_{DD}
ST: Schmidt Trigger Input					
V_{T+}	Input High Threshold	2.1		V	
V_{T-}	Input Low Threshold		0.7	V	
V_{HYS}	Hysteresis	0.2		V	
I_{IN}	Input Leakage	-10	10	µA	V_{IN} = 0V or V_{DD}
OD48: 48 mA Open Drain Output					
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 48 mA
I_{ZL}	High Z Leakage	-30	30	µA	V_O = 0V or V_{DD}
TTL4: 4 mA Output					
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -4 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA

AC Timing

The following figures and the table of values that accompanies them are illustrative of the ESP chip's AC timing characteristics. For definitive values, see the ESP Applications Manual or Specification.

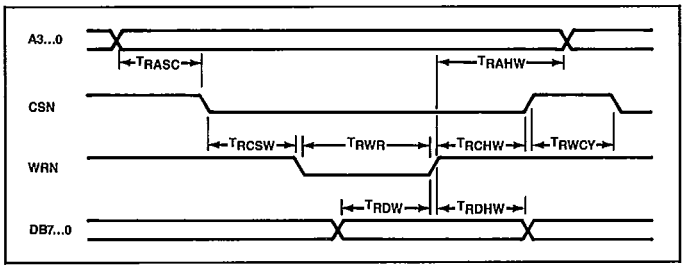

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Figure 5. Register Write Operation

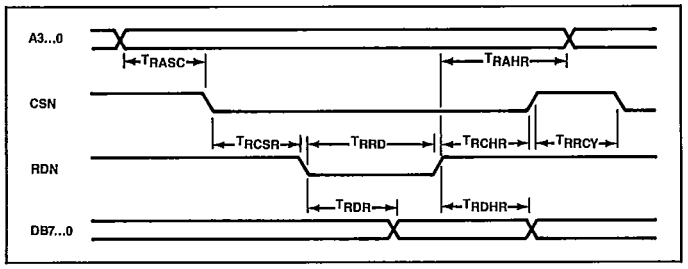

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Figure 6. Register Read Operation

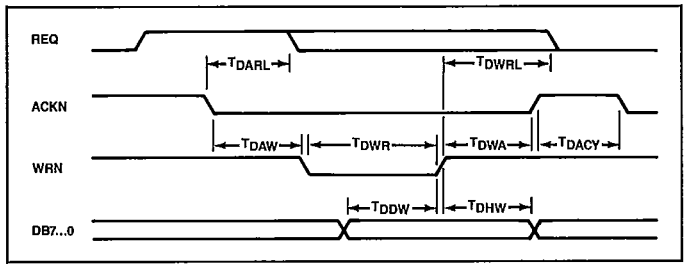

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Figure 7. DMA Write Operation

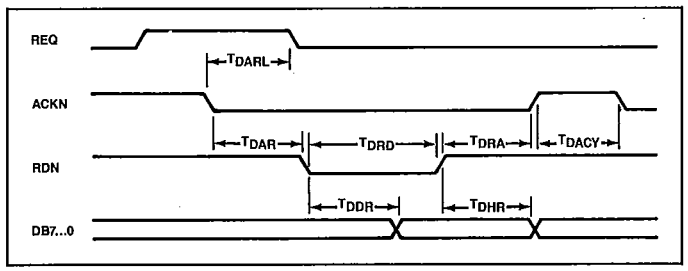

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Figure 8. DMA Read Operation

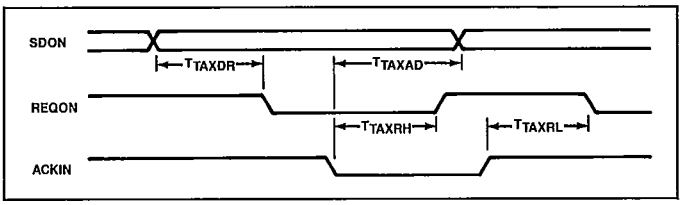

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Figure 9. Target Asynchronous Transmit

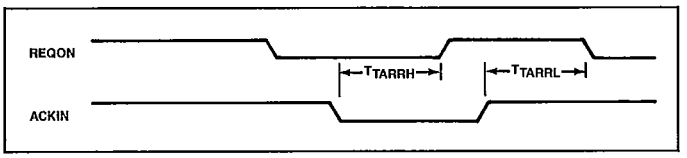

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Figure 10. Target Asynchronous Receive

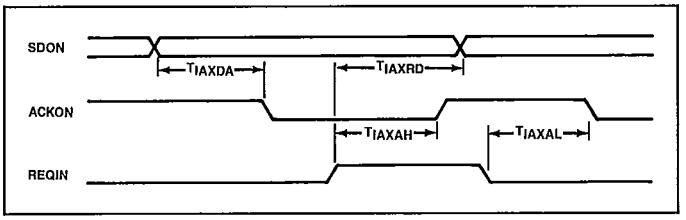

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Figure 11. Initiator Asynchronous Transmit

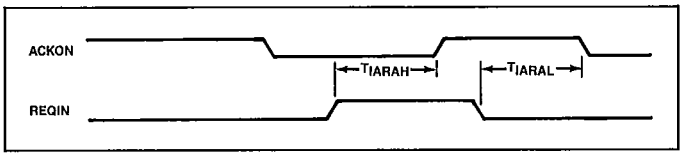

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Figure 12. Initiator Asynchronous Receive

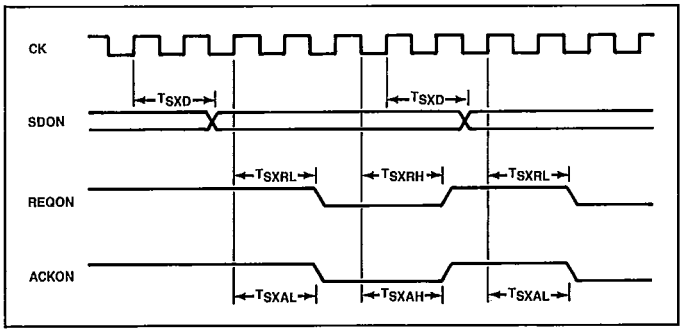

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Figure 13. Synchronous Transmit

Symbol	Parameter	Min	Max	Units
T_{DACY}	ACKN High to ACKN Low	12		Nsec
T_{DAR}	ACKN Low to RDN Low	0		Nsec
T_{DARL}	ACKN Low to REQ Low	0	65	Nsec
T_{DAW}	ACKN Low to WRN Low	0		Nsec
T_{DDR}	RDN to Data		50	Nsec
T_{DDW}	Data to WRN High	20		Nsec
T_{DHR}	Data Hold Time	0	50	Nsec
T_{DHW}	Data Hold Time	10		Nsec
T_{DRA}	RDN High to ACKN High	0		Nsec
T_{DRD}	RDN Pulse Width	40		Nsec
T_{DWA}	WRN High to ACKN High	12		Nsec
T_{DWR}	WRN Pulse Width	40		Nsec
T_{DWRL}	WRN High to REQ Low		44	Nsec
T_{IARAH}	REQIN High to ACKON High		37	Nsec
T_{IARAL}	REQIN Low to ACKON Low		57	Nsec
T_{IAXAH}	REQIN High to ACKON High		55	Nsec
T_{IAXAL}	REQIN Low to ACKON Low		33	Nsec
T_{IAXDA}	Data to ACKON	55		Nsec
T_{IAXRD}	REQIN High to Data		75	Nsec
T_{RAHR}	Address Hold Time	0		Nsec
T_{RAHW}	Address Hold Time	0		Nsec
T_{RASC}	Address Setup to CSN	12		Nsec
T_{RCHR}	RDN High to CSN High	12		Nsec
T_{RCHW}	WRN High to CSN High	12		Nsec
T_{RCSR}	CSN Setup to RDN	12		Nsec
T_{RCSW}	CSN Setup to WRN	12		Nsec
T_{RDHR}	Data Hold Time	0	50	Nsec
T_{RDHW}	Data Hold Time	10		Nsec
T_{RDR}	RDN to Data		50	Nsec
T_{RDW}	Data to WRN High	20		Nsec
T_{RRCY}	CSN High to CSN Low	30		Nsec
T_{RRD}	RDN Pulse Width	40		Nsec
T_{RWCY}	CSN High to CSN Low	60		Nsec
T_{RWR}	WRN Pulse Width	40		Nsec
T_{SXAH}	ACKON High from CK Low	27	50	Nsec
T_{SXAL}	ACKON Low from CK High	13	39	Nsec
T_{SXD}	Data from CK High	30	60	Nsec
T_{SXRH}	REQON High from CK Low	27	50	Nsec
T_{SXRL}	REQON Low from CK High	13	39	Nsec
T_{TARRH}	ACKIN Low to REQON High	40		Nsec
T_{TARRL}	ACKIN High to REQON Low	47		Nsec
T_{TAXAD}	ACKIN Low to Data		59	Nsec
T_{TAXDR}	Data to REQON	55		Nsec
T_{TAXRH}	ACKIN Low to REQON High		40	Nsec
T_{TAXRL}	ACKIN High to REQON Low		44	Nsec

ESP Reference Sheet

#	ESP Read Registers	#	ESP Write Registers
0	Transfer counter lo	0	Transfer count lo
1	Transfer counter hi	1	Transfer count hi
2	FIFO	2	FIFO
3	Command	3	Command
4	Status	4	S/R bus ID
5	Interrupt	5	S/R timeout
6	Sequence step	6	Sync period
7	FIFO flags	7	Sync offset
8	Configuration	8	Configuration
9		9	Clock factor

COMMAND REGISTER (RW3) (Bit 7 = DMA)

Misc Cmds	Initiator Cmds	Target Cmds
00 NOP	10 Transfer info	20 Send msg
01 Flush FIFO	11 Cmd comp seq	21 Send status
02 Reset chip	12 Accept msg	22 Send data
03 Reset SCSI	18 Transfer pad	23 Disconnect seq
	1A Set ATN	24 Terminate seq
Disconnected Cmds		25 Cmd comp seq
40 Reconnect		27 Disconnect
41 Sel w/o ATN		28 Rcv msg seq
42 Sel w/ATN		29 Rcv cmd
43 Sel w/ATN/stop		2A Rcv data
44 Enable S/R		2B Rcv cmd seq
45 Disable S/R		
STATUS (RO4)	**INTERRUPT (RO5)**	**CONFIG (RW8)**
0 I/O	0 Selected	0 Bus ID 0
1 C/D	1 Selected w/ATN	1 Bus ID 1
2 MSG	2 Reselected	2 Bus ID 2
3 Xfr complete	3 Func complete	3 (0)
4 Xfr count 0	4 Bus service	4 Parity enable
5 Parity error	5 Disconnect	5 Parity test mode
6 Gross error	6 Illegal cmd	6 SCSI rst int dis
7	7 SCSI reset	7 Slow cable
SEQ STEP (RO6)		
0 Seq step 0		
1 Seq step 1		
2 Seq step 2		