PA7024
PEEL™ Array

AMI SEMICONDUCTORS

February 1993

Features

User-Configurable High Density Logic Array

- Create multi-level I/O-buried logic circuits
- Over 80 sum-of-products functions
- 20 I/Os, 2 Input/system-clocks
- 24-pin DIP, 28-pin PLCC packaging

CMOS EE Technology

- Low power, ICC = 140mA + 0.5mA/MHz
- Reprogrammable in plastic package
- Low risk inventory, superior factory testing

High Performance

- Wide gate functions in single level delays
- t_{PD} = 13ns/20ns (internal/external)
- f_{MAX} = from 41.6MHz to 58.8MHz

Flexible Architecture

- Input registers and latches
- I/0 buried D, T and JK registers with independent clock, preset and reset
- Separate output enables per I/O

Logic Integration and Customization of:

- PLDs, SSI/MSI, random logic, decoders, encoders, muxes, comparators, shifters, counters, state machines, etc.

Simplified Development Methodology

- Predictable symmetrical timing, no routing
- Design support with PLACE Software

General Description

The PA7024 is a user-configurable high-density Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. Designed in AMI's advanced 1-micron CMOS EE technology, the PA7024 offers low power consumption, high speed performance, and reprogrammability in a plastic package allowing superior factory testing and a low risk reusable inventory. The PA7024's wide-gate architecture can implement complex combinatorial and sequential functions within single-level delays as fast as 13ns (internal) and at clock rates greater than 50MHz.

Its flexible architecture offers input reg/latches per I/O, buried D, T, or JK registers with independent clock, preset and reset, and separate output enables. This versatility makes the PA7024 ideal for integrating SSI/MSI, multiple PLDs and customizing random logic, decoders, muxes, comparators, shifters, counters, state machines, etc. Extensive signal interconnectivity makes all timing paths symmetrical, simplifying design with predictable performance and the elimination of gate array -like routing. Complete development support is provided by AMI's PLACE Software. Programming support is supplied by third-party programmers.

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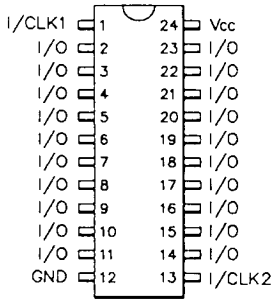
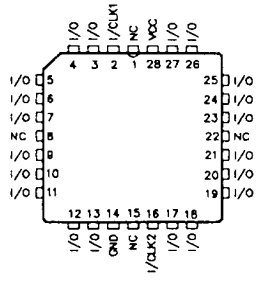
Figure 44: PA7024 Pin and Block Diagram

Pin Configuration



DIP

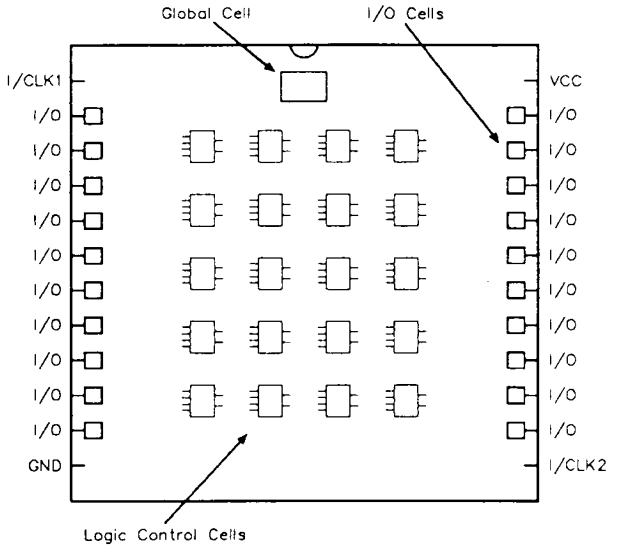


PLCC

Pin Names:

I/CLK = Input and/or System Clock
I/O = Bi-directional I/O
GND = Ground
Vcc = Power Supply

Block Diagram



PA7024 Functional Description

The PA7024 is a user-configurable high-density CMOS Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. As illustrated by figure 44 shown on the previous page (pin configuration and block diagram), the PA7024 has 20 I/O pins and 2 Input/System-Clock pins and is available in both 24-pin 300-mil DIP or 28-pin PLCC packages. The internal architecture of the PA7024 consists of 20 Logic Control Cells (LCCs), 20 I/O Cells (IOCs), and a Global Cell, all of which are interconnected and controlled via a distributed programmable logic array matrix.

Logic Control Cell (LCC) Inputs and Outputs

Logic Control Cells (LCCs) are used to allocate and control the logic functions created in the distributed logic array matrix. Each of the twenty PA7024 LCCs have four primary inputs and two primary outputs. The inputs to each LCC are complete sum-of-product logic functions from the array matrix. The PA7024 has a total of 80 sum-of-product functions for controlling LCC registers, IOC output enables, and combinatorial and sequential logic functions.

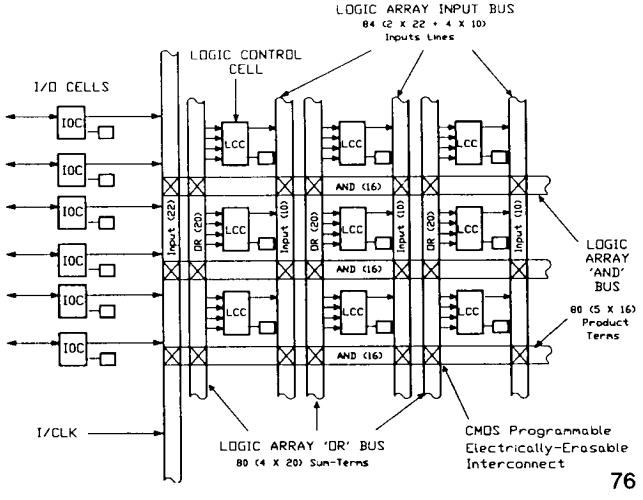
The two outputs of each LCC can function with complete independence from one another. This makes it possible with the PA7024 to have up to 40 independent output functions for internal and external use. (To put this in perspective, the popular 22V10PLD architecture provides a total of 10 output logic functions.) Of the two LCC outputs, one can be connected to any I/O Cell (IOC) and associated I/O pin, and the other is "buried" for use within the logic array matrix. The PA7024 allows up to 20 levels of I/O buried logic, making it possible to implement, for example, a 20-bit high speed binary counter, without sacrificing any I/O pins for input or output use.

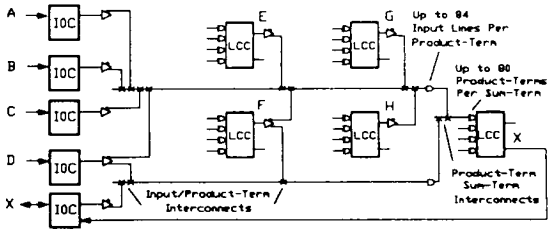
Distributed Logic Array Matrix

To better understand how sum-of-products logic functions are created and how the interconnects between LCCs and IOCs work, figure 45 illustrates the distributed logic array matrix. The logic array matrix is made up of multiple busses of input lines (Input bus), product terms (AND bus) and sum terms (OR bus). One output of each LCC can be connected to any IOC; the other is connected to the internal Input bus. The four inputs to each LCC are actually complete sum-of-product functions from the OR bus.

At the intersection of each Input/AND bus and AND/OR bus reside programmable CMOS EEPROM memory cells for controlling interconnectivity between input lines and product terms, and product terms and sum terms. When selectively programmed, complete sum-of-product logic functions can be created similar to that of a PLA structure. The end result allows each sum-term feeding into an LCC to share up to 80 product-terms and each product-term to share up to 84 input lines (the true and complements of the 22 input pins and the 20 LCC buried outputs). This extensive sharing means product-term resources can be used where they are needed and not left unutilized as with traditional programmable-AND fixed-OR PLDs.

Figure 45: Distributed Logic Array Matrix (partial view) and Illustration of a Sum-of-Products Logic Equation Interconnected in the Array





$$X = (\overline{A} * B * \overline{C} * \overline{D} * E * \overline{F} * G * H) + (X * D * F)$$

Eliminating Complex Routing and Timing Issues

Because of the extensive interconnectivity in the PA7024's distributed logic array structure, the complex routing and timing issues that are often associated with field programmable gate arrays (FPGAs) are eliminated. This makes it possible to predict performance and utilization results before actually implementing the design. With few exceptions, all signals route automatically, as expressed in equation form, provided that the maximum number of product terms are not exceeded. Also, all timing delays are completely symmetrical between I/O pins, IOCs or LCCs. For instance, the internal combinatorial delay from the output of any LCC, through the array, to the input of another LCC, is a maximum of one tPDI (13ns with a PS7024-1). External I/O pin, through and LCC, to any I/O pin, is tPDX (20ns). Clock signals are also symmetrical, abiding any problems of clock skew.

Inside the Logic Control Cell (LCC)

Each PA7024 LCC includes three signal routing and control multiplexers, a versatile register with synchronous or asynchronous D, T, or JK flip-flops, and several EEPROM memory cells for programming a desired configuration. The key elements of the LCC are illustrated in the LCC block diagram, figure 46. The diagram shows how the four LCC inputs (SUM terms A, B, C, and D) are distributed into the cell and how each SUM term can be selectively used for multiple functions as listed below.

Sum-A = D, T, J, or Sum-A
Sum-B = Preset, K, or Sum-B
Sum-C = Reset, Clock, Sum-C
Sum-D = Clock, Output Enable, Sum-D

SUM-A can serve as the D, T, or J input of the register or a combinatorial path. SUM-B can serve as the K input or the preset to the register, or a combinatorial path. SUM-C can be the clock or the reset to the register, or a combinatorial path. And SUM-D can be the clock to the register, or the output enable for the connected I/O cell. It is important to note that unlike many PLDs, the PA7024 has complete sum-of-product (not just product term) control of clocks, resets, presets, and output enables. The two primary outputs of the LCC can independently select the Q output from the register or the Sum A, B, or C combinatorial paths. Thus, one LCC output can be combinatorial while the other is registered.

Besides the SUM inputs, several inputs from the Global Cell are provided for control. The Global Cell inputs are routed to all LCCs. These signals include a high speed clock of positive or negative polarity, global preset and reset, and a special register-type control that allows dynamic switching of register selection. This last feature is useful for implementing loadable counters and state machines by dynamically switching from D to T, for instance.

The I/O Cell (IOC)

The block diagram for the PA7024 I/O Cell (IOC) is shown in figure 47. The input to the IOC can be provided from any one of the LCCs in the array. Each IOC consists of routing and control multiplexers, an input register/transparent latch, a three-state buffer, and an output polarity control. The reg/latch can be clocked from a variety of sources determined in the Global Cell. It can also be bypassed for a non-registered input.

Figure 46: PA7024 Logic Control Cell (LCC)

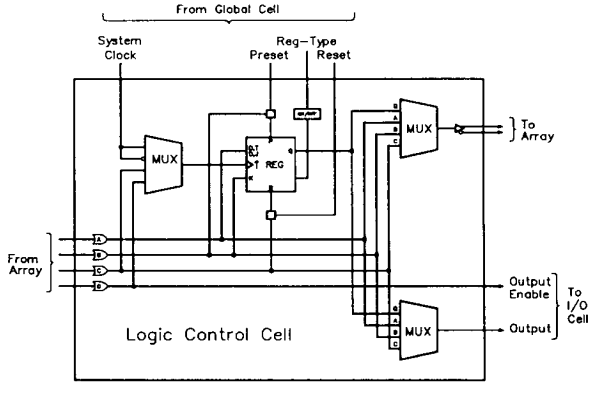
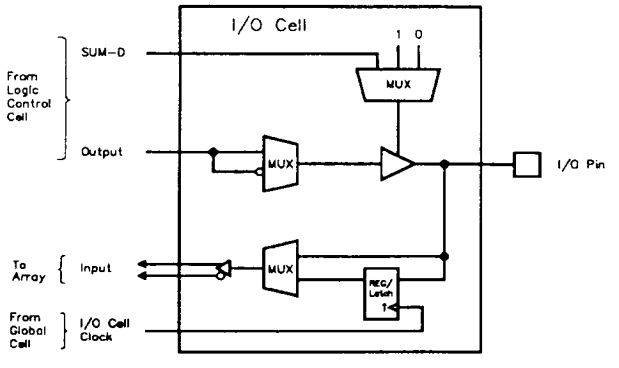


Figure 47: PA7024 I/O Cell (IOC)



The Global Cell

The PA7024's Global Cell, shown in figure 48, is used primarily to control the allocation of the system clock signals to the LCCs and the IOCs. The global cell also contains several global product and sum control terms for LCC functions such as reset, preset, register type, and IOC clock. If additional partitioning of global cell clocks and control terms is needed, a second global cell can be selected that allows the LCCs to be divided into two groups, A and B. That is, half of the LCCs can be controlled by Global Cell A and half with Global Cell B. Global Cell A controls the LCCs connected to IOCs 2-11, and Global Cell B, the LCCs connected to IOCs 14-23. This allows, for instance, two high speed clocks to be used among the LCCs in the same PA7024. Unless the second global cell is selected, all LCCs and IOCs will be controlled by Global Cell A.

PA7024 Applications

The unique combination of wide gate performance and logic cell flexibility allows the PA7024 to address a multitude of logic functions ranging from random logic to high-speed state machines. The PA7024 is ideal for implementing wide-path applications at high speeds such as fast binary counters, clock dividers, state machines, address decoders, encoders, comparators, adders, and look-ahead carry. Yet, its LCC flexibility makes possible standard random logic functions such as D flip-flops (74LS74) with independent clock reset and preset, SR latches, and gated latches. Additionally, the number of registers and latches available for data storage, as well as three-state I/Os, open up many possibilities for bus interfaced sub-systems.

Design Security

The PA7024 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs. Once set, the programmed bits of the PA7024 cannot be accessed until the entire chip has been electrically erased.

Development Support

Development support for the PA7024 is provided by the PLACE Development Software and PEEL Development System from AMI. The PLACE (PEEL Architectural Compiler and Editor) software creates a software design environment that combines the attributes of logic equation and schematic entry. The mouse-driven PLACE editor graphically illustrates and controls the PA7024's architecture, making the overall design easy to understand, while allowing the effectiveness of boolean logic equations or state machine design entry.

The PLACE compiler performs logic transformation and logic reduction, making it possible to specify equations in almost any fashion and to get the maximum logic into every design. PLACE also provides a multi-level logic simulator that allows the external and internal signals to be fully simulated and analyzed via a waveform display. Programming is supported with direct interface to the AMI PEEL Development System programmer (PDS-1) as well as with a down-load capability to other popular programmers. System requirements for PLACE are IBM XT/AT or compatible, 640K memory, EGA or VGA graphics, and mouse.

Figure 48: PA7024 Global Cell

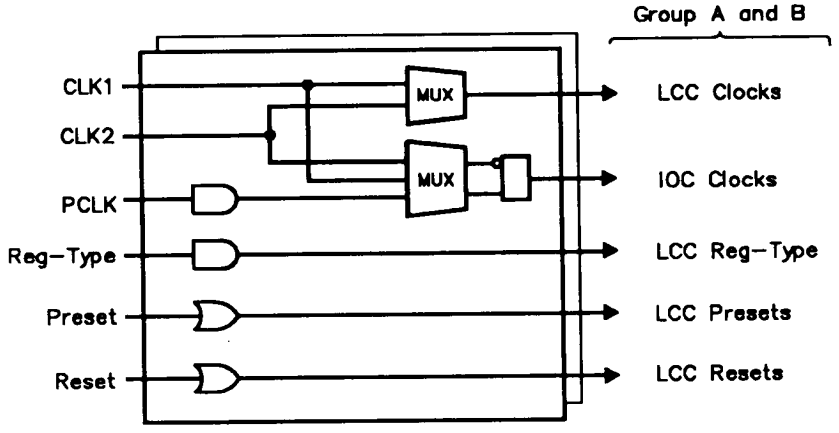


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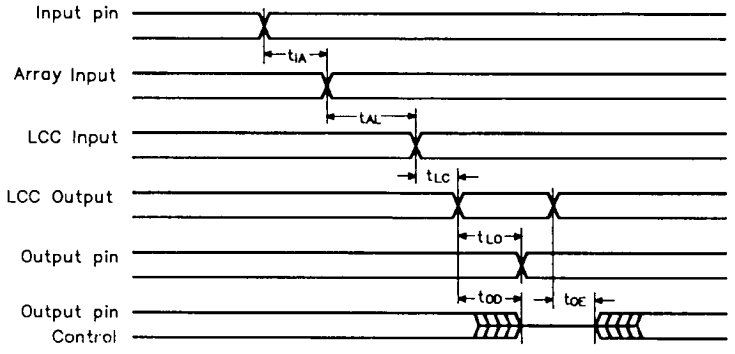
Figure 49: Combinatorial Timing - Waveforms and Block Diagram



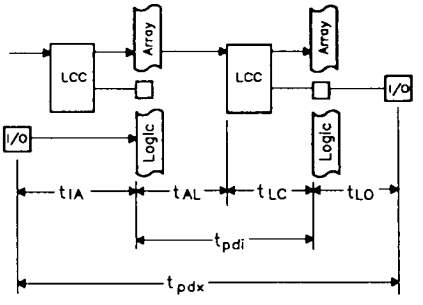
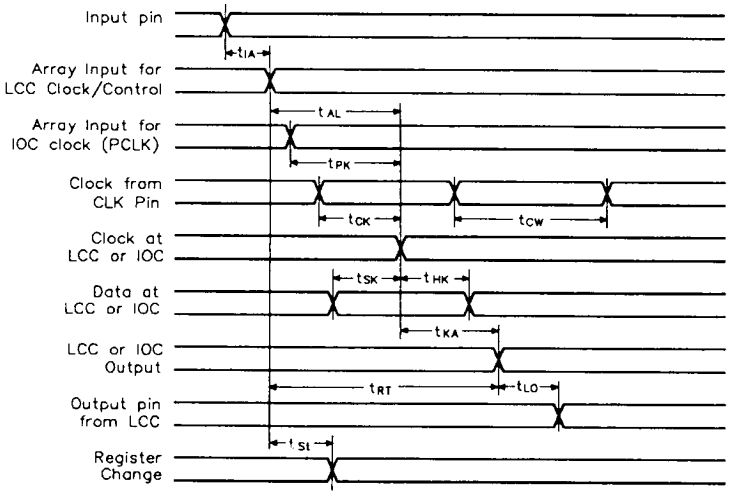


Figure 50: Sequential Timing - Waveforms and Block Diagram



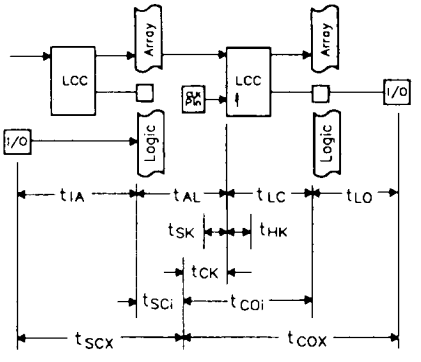
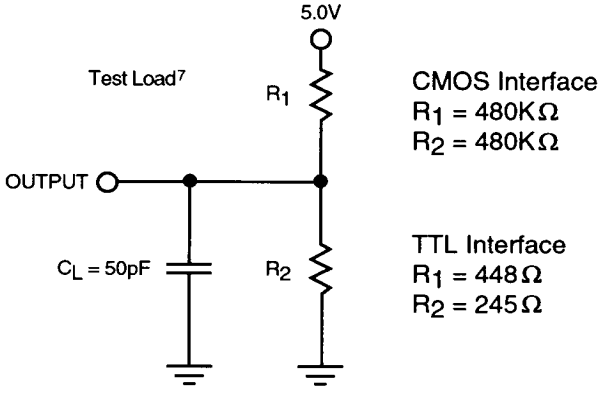
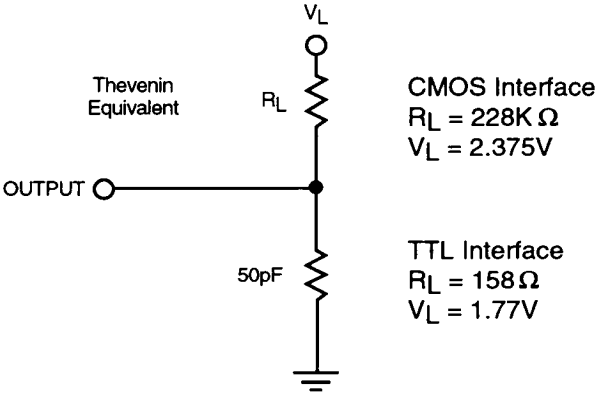


Figure 51: AC Test Loads





Absolute Values

Absolute Maximum Ratings[8]

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Vcc	Supply Voltage	Relative to GND	-0.5	7.0	V
Vi	Voltage applied to Input[4]	Relative to GND[1,10]	-0.5	Vcc +0.6	V
Vo	Voltage applied to Output	Relative to GND[1]	-0.5	Vcc +0.6	V
Io	Output Current	Per pin (Iol, Ioh)		+25	mA
Tst	Storage Temperature		-65	+150	C
Tlt	Lead Temperature	(soldering 10 seconds)		+300	C

Operating Ranges

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Vcc	Supply Voltage	Commercial	4.75	5.25	V
Ta	Operating Temperature	Commerical	0	+70	C
Tr	Clock Rise Time[5]	Test points at 10% and 90% levels		250	ns
Tf	Clock Fall Time[5]	Test points at 10% and 90% levels		250	ns
Trvcc	Vcc Rise Time[5]	Test points at 10% and 90% levels		250	ms

DC Characteristics (Over Operating Range Specifications)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Iil	Input Leakage	Vin = GND to Vcc			±10	µA
Ioz	Output Leakage	I/O = High Impedance Vo = GND to Vcc			±10	µA
Icca	Vcc Current, Active[9,15]	Vin = Vil or Vih			125+ 0.5mA/MHz	mA
Vil	Input Low Voltage		-0.3		0.8	V
Vih	Input High Voltage		2.0		Vcc+0.3	V
Vol	Output Low Voltage TTL	Iol = +8.0mA			0.45	V
Volc	Output Low Voltage CMOS	Iol = 10µA			0.1	V
Voh	Output High Voltage TTL	Ioh = -4.0mA	2.4			V
Vohc	Output Low Voltage CMOS	Ioh = -10µA	Vcc -0.1			v

Capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Cin	Input Capacitance[3,7]	Frequency = 1MHz		4	6	pF
Cout	Output Capacitance[3,7]	Frequency = 1MHz		8	12	pF
Cclk	Clk Pin Capacitance[3,7]	Frequency = 1MHz		8	13	pF

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AC Electrical Characteristics Combinatorial
Vcc=5V ± 5% (over operating range specifications)

SYMBOL	PARAMETER[12,17]	UNITS	PA7024-1 MIN	PA7024-1 MAX
tPDI	Propagation delay Internal (tAL + tLC)	ns		13
tPDX	Propagation delay External (tIA + tAL + tLC + tLO)	ns		20
tIA	Input or I/O pin to Array Input	ns		2
tAL	Array input to LCC	ns		12
tLC	LCC input to LCC output	ns		1
tLO	LCC output to output pin	ns		5
tOD	Output Disable from LCC output[6]	ns		5
tOE	Output Enable from LCC output[6]	ns		5
tOX	Output Disable, Enable from Input pin[6]	ns		20

AC Electrical Characteristics Sequential
Vcc=5V ± 5% (over operating range specifications)

SYMBOL	PARAMETER[12,13,16,17]	UNITS	PA7024-1 MIN	PA7024-1 MAX
tSCI	Input set-up to system-clock, sys-clk, (tAL+tSK+tLC-tCK)}LCC	ns	10	
tSCX	Input set-up to sys-clk, (tIA+tSCI)}LCC	ns	12	
tCOI	Sys-clk to Array Int. (tCK+tLC)} LCC/IOC	ns		7
tCOX	Sys-clk to Output Ext. (tCOI+tLO)} LCC	ns		12
tHX	Input hold time from sys-clk} LCC	ns	0	
tSK	LCC input set-up to async clock} LCC	ns	3	
tHK	LCC input hold time from async. clock} LCC	ns	4	
tSI	Input set-up to sys-clk (tSK-tCK)}IOC	ns	0	
tHI	Input hold time from sys-clk (tCK-tSK)} IOC	ns	3	
tPK	Array input to IOC PCLK clock, PCLK	ns		7
tSPI	Input set-up to PCLK (tSK-tPK-tSK)}IOC[18]	ns	0	
tHPI	Input hold time from PCLK (tPK+tIA+tSK)} IOC	ns	6	
tCK	Sys-clk delay to LCC and IOC	ns		6
tCW	Sys-clk low or high pulse width	ns	7	
fmax1	Max sys-clk freq Int/Int 1/ (tSCI+tCOI)	MHz		58.8
fmax2	Max sys-clk freq Ext/Int 1 (tSCX+tCOL)	MHz		52.6
fmax3	Max sys-clk freq Int/Ext 1/ (tSCI+tCOX)	MHz		45.7

AC Electrical Characteristics Sequential (cont.)
Vcc=5V ± 5% (over operating range specifications)

			PA7024-1	
SYMBOL	PARAMETER[12,13,16,17]	UNITS	MIN	MAX
fmax4	Max sys-clk freq Ext/Ext1 (tSCX + tCOX)[14]	MHz		41.6
fTGL	Max sys-clk toggle freq 1/(tCW + tCW)	MHz		71.4
tPR	LCC Preset/Reset to LCC output	ns		1
tST	Input to Global cell pre/reset (tIA + tAL + tPR)	ns		15
tAW	Async preset/reset pulse width	ns	8	
tRT	Input to LCC reg-Type, RT	ns		8
tRTV	LCC RT to LCC output register change	ns		1
tRTC	Input to Global cell RT change (tRT + tRTV)	ns		9
tRW	Asynchronous RT pulse width	ns	10	

Notes:

1. Minimum DC input =-0.5V; however, inputs may undershoot to - 2.0V for periods < 20ns.
2. Voltage applied to input or output must not exceed Vcc+1.0V.
3. These measurements are periodically sample tested.
4. The term "Input" without any reference to another term refers to an (external) input pin.
5. Test points for Clock and Vcc in Tr, Tf, and Trvcc are referenced at 10% and 90% levels.
6. See AC test point/load circuit table for test loads. tOE is measured from input transition to VREF + 0.1V. tOD is measured from input transition to Voh-0.1V or Vol+0.1V.
7. Typical values and capacitance are measured at Vcc=5.0 V and Ta = 25°C.
8. Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum rating may cause permanent damage.
9. I/O pins are open (no load).
10. Vin specified is not for program/verify operation. Contact AMI for information regarding PEEL program verify specifications.
11. Test one output at a time for a duration of less than 1 sec.
12. Test conditions assume signal transition times of 5ns or less from the 10% and 90% points, and timing reference levels of 1.5V (unless otherwise specified).
13. "System-clock" or "Sys-clk" refers to pin 1 or pin 13 high speed clocks.
14. For T or JK registers in toggle (divide by 2) operation only.
15. Icc is tested with the device programmed as a 20-bit Counter.
16. "Async clock" refers to the clock from the Sum term (OR gate).
17. The "LCC" term indicates that the timing parameter is applied to the LCC register. The "IOC" term indicates that the timing parameter is applied to the IOC register. The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and the IOC registers.
18. The parameter tSPI indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (tSK-tPK-tIA). This means that no set-up time for the data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for the tHPI time, i.e., to wait for the PCLK signal to arrive at the IOC register.