DATA SHEET

Hi-IQ
High Integration QUBiC array family

Preliminary specification

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Philips Semiconductors

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High Integration QUBiC array family — Hi-IQ

DESCRIPTION

Hi-IQ (High Integration QUBiC) is a logic array family targeted for the implementation of high density and high performance user specific and standard products. The array family is implemented in the QUBiC process, a dual layer metal, high performance sub-micron BiCMOS process. This data sheet provides the specifications for the arrays, design system, macro cell library and a SRAM Compiler.

Hi-IQ arrays are high density and high performance semi-custom devices that integrate state-of-the-art CMOS transistors and high performance bipolar transistors on the same chip. Hi-IQ arrays take advantage of the high speeds of bipolar transistors while keeping the low power dissipation and high density of CMOS transistors to implement arrays ranging from 40,500 to 259,920 available gates and system speeds in excess of 50MHz. The Design System, with the help of the SRAM Compiler, allows the user to implement designs with near-custom density and performance with gate array productivity.

Study of large digital subsystem designs implemented in CMOS gate arrays has revealed that the most critical performance limitation is due to the poor pull-up capability of PMOS transistors at the output of macro cells. Therefore, replacing these PMOS transistors with bipolar NPN transistors significantly improves the performance. On the other hand, NMOS transistors provide better or equal pull-down capability than BiCMOS NPN pull-down transistors for over 95% of all nets found in gate arrays and standard cell designs. This circuit configuration is referred to as BiNMOS.

FEATURES

- 0.7 micron channel length, 1.0 micron poly-silicon emitter BiCMOS technology
- Six array sizes ranging from 40,500 to 259,920 available gates
- Up to 104,882 usable gates
- Up to 120K bits of configurable SRAM blocks
- Up to 284 signal I/Os with choice of:
  - Input, output, or bi-directional buffers
  - TTL/CMOS level input compatibility
  - Registered outputs
  - Configurable output drive up to 48mA
  - Programmable slew rate control
- BiCMOS clock drivers for minimum clock skew
- High latch-up immunity
- Multiple drive strengths for macro cells

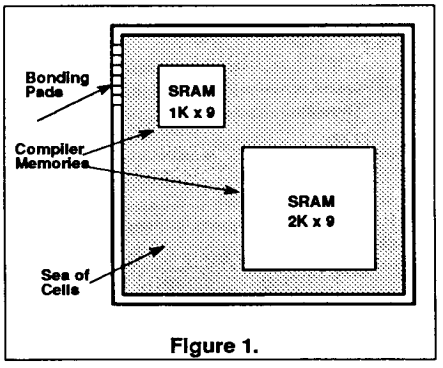

Figure 1.

BENEFITS

- Solution for high performance designs (>50MHz)
- Up to 50% higher system speed than CMOS gate arrays
- Optimized system performance through the use of registered input and output buffers
- Up to 40% higher gate density than CMOS gate arrays, approaching standard cell gate densities
- Up to 300% denser SRAM than CMOS gate arrays, approaching standard cell SRAM densities
- Fast prototype and production delivery with metal mask programmable technology
- Reduced board space and power dissipation through single chip integration of bus drivers and external SRAM blocks
- Higher pre-layout performance predictability through use of BiNMOS drivers for all macro cells
- High design productivity through the use of Hi-IQ design environment
- Extensive macro cell library for area and performance optimization

Table 1. HI-IQ Array Family

Device Name	Available Gates	Usable Gates	Available Compute/Drive Cells	Total Pads	Min V_{DD} Pads	Min GND Pads	I/O Pads
HIQ1030	40,500	16,200	24,300 / 8,100	120	8	8	104
HIQ1060	58,320	23,328	34,992 / 11,664	144	8	8	128
HIQ1080	79,380	31,752	50,700 / 16,900	168	8	8	152
HIQ1150	121,680	48,672	73,008 / 24,336	208	8	12	188
HIQ1200	184,320	73,728	110,592 / 36,864	256	8	12	236
HIQ1250	259,920	103,968	155,952 / 51,984	304	8	12	284

Hi-IQ Array Family

The Hi-IQ array family initially consists of five members ranging in size from 40,500 to 259,920 available gates. Table 1 shows the available and usable number of gates for the members of the array family along with their characteristics. For a typical mix of combinational and sequential logic approximately 40% array utilization is achieved.

One compute cell can implement a single bit of single-ported SRAM. As the SRAM portion of a design increases the percent utilization of the array also increases. Figure 2 shows a graph of array utilization as a function of the percent of chip used for SRAM. If a large percentage of the array is occupied by SRAM, higher array utilizations will be achieved.

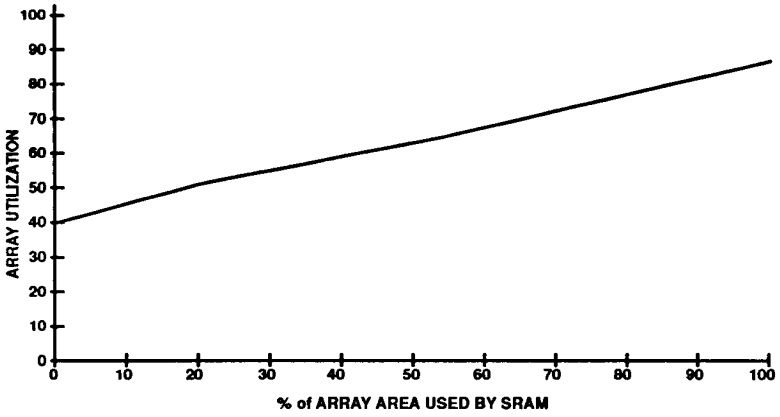

Figure 2. Array Utilization as a Function of Array Area Used by SRAM

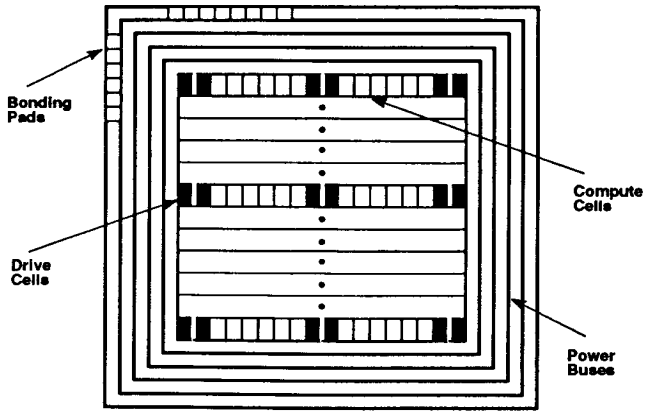

Figure 3. HI-IQ Array Core and Periphery

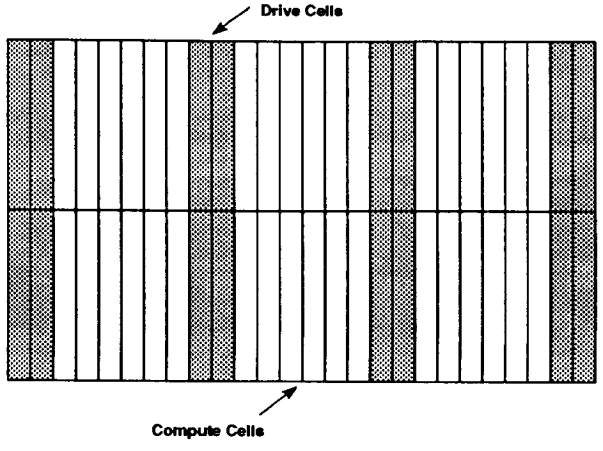

Figure 4. Array of Basic Hi-IQ Compute and Drive Cells

The reduced size transistors in compute cells realize SRAM densities comparable to custom SRAMs. The array is composed of a core and a periphery, both contain MOS as well as NPN bipolar transistors (Figure 3).

Array Architecture

The Hi-IQ array architecture takes advantage of a new architecture called BiNMOS-CBA (Cell Based Array) from SiArc. BiNMOS-CBA utilizes both CMOS and BiCMOS technologies to implement logic and SRAM efficiently at high speeds and low power. The Hi-IQ array consists of two different type of cells; compute cells and drive cells. The compute cells employ small CMOS transistors for implementing logic and SRAM efficiently; the drive cells contain a single pull-up NPN device to improve drive and achieve full BiCMOS high performance. Large NMOS transistors are used in the drive cell for pull-down. Macrocells are created using the compute and drive cells. Since each macro cell can contain a BiNMOS driver, the size of CMOS transistors in the compute cell can be significantly reduced.

Array Core

The core is configured as a channelless array of CBA compute and drive cells. Each compute cell consists of eight CMOS transistors of varying sizes that allow efficient implementation of logic and SRAM. The drive cell consists of a single NPN pull-up transistor, two large NMOS pull-down transistors and a small PMOS level restoring transistor to provide high speed for all fanouts. The compute and drive cells are arrayed such that two adjacent drive cells can utilize additional large NMOS pull-down transistors to optimize performance and area (Figure 4).

Array Periphery

The periphery consists of a ring of I/O cells placed under the five rings of V_{DD} and GND buses (Figure 3). Separate V_{DD} and GND bus rings are used for array and I/O power supplies. Each I/O cell can be configured as a TTL or CMOS input, TTL output, three-state or bi-directional buffer with programmable drive and slew rate. I/O cells can also be configured as programmable strength clock drivers. This driver can be used to drive other very high fanout nets. Each configured output buffer can be registered to optimize system-level performance.

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IL}	Input low voltage	TTL			0.8	V
		CMOS			1.5	V
V_{IH}	Input high voltage	TTL	2.0			V
		CMOS	3.5			V
V_T	Switching threshold	TTL		1.5		V
		CMOS		2.5		V
I_{IN}	Input current	$V_{IN} = V_{DD}$	–10	±1	10	µA
		$V_{IN} = V_{SS}$	–10	±1	10	µA
V_{OL1}	Output low voltage	I_{OL1} = 4mA			0.4	V
		I_{OL1} = 8mA			0.4	V
		I_{OL1} = 12mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = –1mA	2.4			V
		I_{OH} = –2mA	2.4			V
		I_{OH} = –3mA	2.4			V
I_{OS}	Output short current	V_O = 0V	50	100	300	mA
I_{OZ}	3-state leak current	$V_{OH} = V_{SS}$	–10	±1	10	µA
		$V_{OH} = V_{DD}$	–10	±1	10	µA
C_{IN}	Input capacitance	Input only			2	pF
C_{OUT}	Output capacitance	12mA output buffer			5	pF

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Power supply	-0.3 to +6.0	V
V_I	Input voltage	–0.3 to V_{DD} + 0.3	V
V_O	Output voltage	–0.5 to +5.5	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature Plastic Ceramic	 –40 to +125 –65 to +150	 °C °C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Power supply (commercial)	+4.75 to +5.25	V
V_{DD}	Power supply (military)	+4.5 to +5.5	V
T_{AC}	Commercial ambient temperature	0 to 70	°C
T_{AM}	Military ambient temperature	–55 to +125	°C

Table 1. Sample Input Buffer Specifications (ns)

		Fanout							
Input Buffers	**Symbol**	**1**	**2**	**3**	**4**	**5**	**6**	**8**	**16**
CMOS non-inverting input buffer	t_{PLH}	0.65	0.68	0.71	0.74	0.77	0.80	0.84	1.0
	t_{PHL}	0.57	0.60	0.63	0.65	0.68	0.70	0.74	0.89
TTL non-inverting input buffer	t_{PLH}	0.47	0.50	0.53	0.56	0.59	0.62	0.66	0.86
	t_{PHL}	0.65	0.68	0.71	0.74	0.77	0.79	0.84	1.01
CMOS inverting input buffer	t_{PLH}	0.32	0.38	0.43	0.48	0.51	0.57	0.65	0.91
	t_{PHL}	0.37	0.44	0.51	0.56	0.60	0.70	0.77	1.1
TTL inverting input buffer	t_{PLH}	0.32	0.33	0.33	0.34	0.35	0.35	0.36	0.42
	t_{PHL}	0.31	0.36	0.39	0.43	0.47	0.51	0.57	0.86

Table 2. Sample Output Buffer Specifications (ns)

		Load			
Output Buffers	**Symbol**	**15pF**	**35pF**	**50pF**	**100pF**
Output buffer 4mA	t_{PLH}	1.29	1.88	2.32	3.79
	t_{PHL}	1.23	2.08	2.70	4.78
Output buffer 8mA	t_{PLH}	1.08	1.43	1.67	2.42
	t_{PHL}	0.96	1.50	1.89	3.18
Output buffer 12/24mA	t_{PLH}	1.04	1.35	1.56	2.20
	t_{PHL}	0.90	1.30	1.59	2.52
3-State buffer 4mA	t_{PLH}	1.29	1.88	2.32	3.79
	t_{PHL}	1.23	2.08	2.70	4.78
3-State buffer 8mA	t_{PLH}	1.08	1.43	1.67	2.42
	t_{PHL}	0.96	1.50	1.89	3.18
3-State buffer 12/24mA	t_{PLH}	1.04	1.35	1.56	2.20
	t_{PHL}	0.90	1.30	1.59	2.52
Bi-directional buffer 4mA	t_{PLH}	1.42	2.01	2.45	3.92
	t_{PHL}	1.41	2.28	2.88	4.82
Bi-directional buffer 8mA	t_{PLH}	1.29	1.74	2.06	3.09
	t_{PHL}	1.16	1.79	2.24	3.6
Bi-directional buffer 12/24mA	t_{PLH}	1.18	1.51	1.72	2.4
	t_{PHL}	1.03	1.45	1.76	2.74

Table 3. Sample Clock Buffer Specifications (ns)

		Fanout			
Clock Buffer	**Symbol**	**200**	**400**	**800**	**1600**
Clock buffer (TTL)	t_{PLH}	1.35	1.48	1.69	2.10
	t_{PHL}	1.20	1.38	1.66	2.13
Clock buffer (CMOS)	t_{PLH}	0.94	1.10	1.27	1.64
	t_{PHL}	1.01	1.18	1.46	1.92

Table 4. Sample Combinational Macro Specifications (ns)

		Fanout							
Input Buffers	**Symbol**	**1**	**2**	**3**	**4**	**5**	**6**	**8**	**16**
Inverter									
inv1a1	t_{PLH}	0.18	0.20	0.21	0.22	0.23	0.25	0.27	0.35
	t_{PHL}	0.13	0.17	0.20	0.24	0.30	0.33	0.38	0.66
inv1a2	t_{PLH}	0.19	0.20	0.21	0.23	0.24	0.26	0.27	0.35
	t_{PHL}	0.10	0.11	0.13	0.15	0.19	0.21	0.23	0.37
2 Input NAND Gate									
nand2a1	t_{PLH}	0.28	0.29	0.30	0.31	0.32	0.33	0.34	0.42
	t_{PHL}	0.20	0.24	0.30	0.34	0.40	0.45	0.53	0.92
2 Input NOR Gate									
nor2a1	t_{PLH}	0.32	0.34	0.35	0.36	0.37	0.39	0.41	0.50
	t_{PHL}	0.14	0.18	0.22	0.24	0.29	0.34	0.38	0.65
4 Input AND Gate									
and4a1	t_{PLH}	1.0	1.01	1.03	1.04	1.05	1.07	1.09	1.17
	t_{PHL}	0.34	0.38	0.42	0.46	0.50	0.54	0.60	0.84
2-AND Into 2-OR Gate									
ao1a1	t_{PLH}	0.68	0.69	0.70	0.71	0.72	0.74	0.76	0.84
	t_{PHL}	0.71	0.74	0.80	0.85	0.90	0.95	1.05	1.34
2 Input XOR Gate									
xor2a1	t_{PLH}	0.54	0.55	0.56	0.57	0.58	0.59	0.61	0.68
	t_{PHL}	0.50	0.51	0.54	0.58	0.65	0.70	0.77	1.09

Table 5. Sample Sequential Macro Specifications (ns)

		Fanout							
Input Buffers	**Symbol**	**1**	**2**	**3**	**4**	**5**	**6**	**8**	**16**
D Flip Flop									
fd1a1	t_{PLH}	1.55	1.56	1.58	1.59	1.61	1.62	1.65	1.74
	t_{PHL}	1.19	1.23	1.28	1.33	1.38	1.42	1.50	1.79
	t_{SU}	0.68	0.68	0.68	0.68	0.68	0.68	0.68	0.68
	t_{HD}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15

V_{DD} and GND Pad Requirements

Hi-IQ arrays allow the user complete freedom in choosing placement of the V_{DD} and GND pads for their designs. Refer to Table 1 to determine the minimum number of required V_{DD} and GND pairs for each array. It may be necessary to use additional V_{DD} and GND pads according to the number and strength of output buffers and how these are used in the system. These additional V_{DD} and GND pads will reduce the number of pads available for use as signal I/Os. One V_{DD} and GND pair is required for every eight 12mA DC non-switching output driver equivalent. In the case of simultaneously switching outputs, large transient currents can occur, increasing the minimum number of V_{DD} and GND pairs required for proper operation. For each eight 12mA current equivalent outputs which are switched simultaneously (buffers switching within a 10ns window are simultaneous), an additional V_{DD} and GND pair is required.

Power Dissipation

When designing high performance integrated circuits and systems, it is very important to make sure that the power dissipation of the device does not exceed the heat dissipation capability of the package. The amount of dissipated power depends on the frequency of the input clock, rate at which the internal cells are switching, number of inputs and outputs and their switching rate. Total power dissipation for the device can be calculated by determining the individual components of power. The Hi-IQ design system will calculate the power for a given design based on user inputs and compiled functions.

$$P_m = 1.40 \cdot N_1 \cdot PS_1 \cdot \left[\frac{1}{2} C_1 \cdot V_{DD}^2 \cdot F\right]$$

$$P_o = 1.25 \cdot N_2 \cdot PS_2 \cdot \left[\frac{1}{2} C_2 \cdot V_{DD}^2 \cdot F\right]$$

$$P_i = 1.40 \cdot N_3 \cdot PS_3 \cdot \left[\frac{1}{2} C_3 \cdot V_{DD}^2 \cdot F\right] + [N_3 \cdot (0.5mA) \cdot V_{DD}]^*$$

$$P_c = 1.25 \cdot N_4 \cdot [C_4 \cdot V_{DD}^2 \cdot F]$$

P_r = Computed by SRAM Compiler as a function of operating conditions.

$P_t = P_m + P_o + P_i + P_c + P_r$

where

P_m = Power consumption due to core macros (Watts).
P_o = Power consumption due to output buffers (Watts).
P_i = Power consumption due to input buffers (Watts).
P_c = Power consumption due to clock buffers (Watts).
P_r = Power consumption due to RAM cells (Watts).
P_t = Total power consumption (Watts).
F = The clock frequency of the design (Hz).
N_1 = Total number of core macros in the design.
C_1 = Average load each core macro is driving (Farads).
PS_1 = The percentage of core macros switching in a clock cycle (default 10%).
N_2 = Total number of output buffers in the design.
C_2 = Average load each output buffer is driving (Farads).
PS_2 = The percentage of output buffers switching in a clock cycle (default 40%).
N_3 = Total number of input buffers in the design.
C_3 = Average load each input buffer is driving (Farads).
PS_3 = The percentage of input buffers switching in a clock cycle (default 40%).
N_4 = Total number of clock buffers in the design.
C_4 = Average load each clock buffer is driving (Farads).
V_{DD} = Power supply (Volts).

Example of Dynamic Power Calculation

To calculate the power dissipation for a design which contains 10,000 macros, of which 15% are switching at 50MHz driving 200fF load, 30% of 100 outputs switching at 50MHz driving an average load of 35pF, 30% of 100 inputs switching at 50MHz driving an average load of 200fF and clock buffer driving 30pF at 100MHz.

$$P_m = 1.40 \cdot (10,000) \cdot 0.15 \cdot \left[\frac{1}{2} 200fF \cdot 25 \cdot 50MHz\right] = 0.26W$$

$$P_o = 1.25 \cdot 100 \cdot 0.3 \cdot \left[\frac{1}{2} 35pF \cdot 25 \cdot 50MHz\right] = 0.82W$$

$$P_i = 1.40 \cdot 100 \cdot 0.3 \cdot \left[\frac{1}{2} 200fF \cdot 25 \cdot 50MHz\right] + [100 \cdot (0.5mA) \cdot 5]^* = 0.26W$$

$$P_c = 1.25 \cdot 1 \cdot [30pF \cdot 25 \cdot 100MHz] = 0.1W$$

$P_t = 0.26 + 0.82 + 0.26 + 0.10 = 1.44W$

*for TTL inputs only

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MEMORY COMPILER

Description

Hi-IQ single port static RAM Compiler allows the user to automatically generate single-port SRAMs. The user can efficiently generate SRAMs of arbitrary sizes which can be placed anywhere within the array core. The compiler generates two different sets of output files. The first set contains a Cadence schematic symbol, a Verilog® simulation model with timing information, data sheet including timing, area and power estimates and functional test vectors. The second set includes physical layout models to be used by place and route tools. The physical dimensions of the compiled SRAMs are also generated. The density and performance of the generated SRAMs are competitive with cell based SRAMs. Thus SRAM intensive designs normally requiring all-layer customization can be efficiently implemented in metal mask programmable Hi-IQ arrays. Automatically generated Verilog simulation models and test vectors allow the user to fully simulate the SRAM for functionality and timing before building it. The timing models can also be incorporated with the rest of the design to perform complete chip simulation.

The single port Memory Compiler is capable of generating bit R/W and word R/W SRAMs. The bit R/W SRAM allows the user to write any number of bits in the word. The word R/W SRAM read and writes the complete word at a time. The word R/W SRAMs are available with chip select which when deactivated save power consumption.

Hi-IQ's single port SRAMs use the traditional six transistor cell which can be efficiently implemented in one compute cell of the CBA architecture. The sense amplifiers are also implemented using the CBA compute and drive cells. This provides the flexibility of placing arbitrary size SRAMs anywhere within the core array. The bipolar pull-up devices are used in the word line drivers.

FEATURES

- High density single-ported SRAMs of sizes up to 18K bits
- SRAM density competitive with cell based technologies
- Access times competitive with high performance commercially available SRAMs
- Data word widths from 1 to 144 bits are supported
- Number of words from 16 to 2K are supported
- Power down option provided for low power dissipation
- Cadence schematic symbols and Verilog simulation models are automatically generated for the Hi-IQ design environment
- Functional test vectors are automatically generated

The SRAM Compiler provides an easy-to-use interface for specifying SRAM parameters from within the Cadence environment. The user is provided with a window in which parameters such as the name of library the RAM should reside in, name of RAM cell, number of words, number of bits per word, column decode ratio and output drive strength of RAMs can be specified. Figure 5 shows the Design flow of the Memory Compiler for creating a 1K x 9 single-ported SRAM. Table 6 contains sample SRAM blocks with their area and timing parameters which can be generated using the Hi-IQ Memory Compiler.

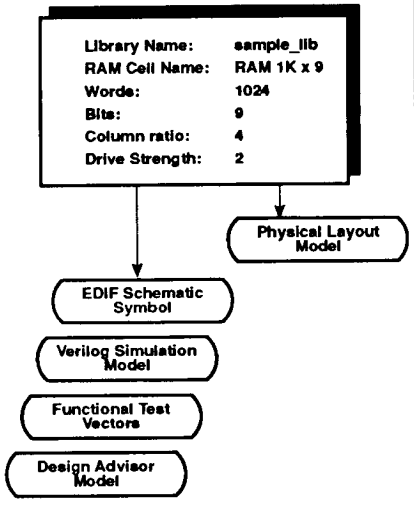
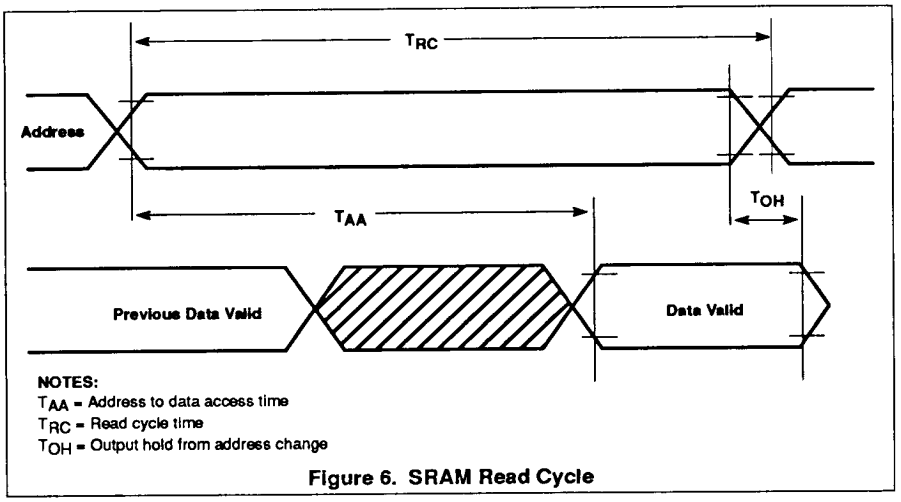


Figure 5. Memory Compiler Design Flow

Table 6. Sample SRAMs

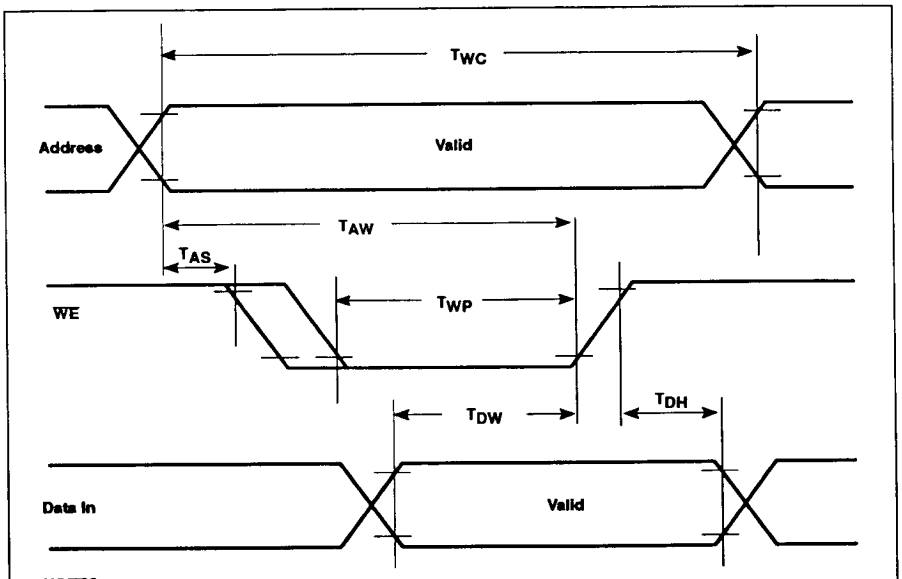
Memory Config.	Compute / Drive Cells	Taa	Twc
32 x 16	1035 / 368	4.7	2.8
64 x 64	5499 / 1872	5.5	3.7
1K x 9	11076 / 3834	7.1	5.8
2K x 9	21300 / 7242	8.2	6.9

* All timing numbers are in nanoseconds and assume typical conditions.



NOTES:
T_{AA} = Address to data access time
T_{RC} = Read cycle time
T_{OH} = Output hold from address change

Figure 6. SRAM Read Cycle



NOTES:
T_{WC} = Write cycle time
T_{WP} = Write pulse width
T_{AS} = Address set-up time
T_{AW} = Address Valid to end of write
T_{DW} = Data set-up time
T_{DH} = Data hold time

Figure 7. SRAM Write Cycle

DESIGN SYSTEM

The Hi-IQ Design System incorporates popular design tools on workstations for design entry, optimization, simulation, verification, and place and route. These tools combined together provide an easy and efficient environment for the designer.

The front end of the Design System integrates Synopsys and Verilog tools for design synthesis, optimization and verification with proprietary libraries and SRAM Compiler. Together these allow users to describe and simulate their designs in any combination of gate-level and high-level descriptions, and to efficiently map their designs to the Hi-IQ cell library.

Hi-IQ libraries include Cadence (OPUS) descriptions for all macro cell symbols, and the back-end of the system accepts EDIF 2 0 0 netlists for placement and routing, providing a straightforward interface for users to integrate the schematic capture tool with the Design System.

The Hi-IQ Design Advisor and SRAM Compiler complete the front end of the system. The Design Advisor checks complete or partial designs for errors, and provides the user with useful feedback on design statistics. The SRAM Compiler outputs symbols and simulation models for the compiled SRAMs in addition to producing layouts for the back-end tools. Figure 8 shows the tools, libraries and interfaces for the Design System.

The back end of the system consists primarily of Cadence's Gate Ensemble place and route tools, together with Hi-IQ libraries and interfaces. The back end also includes the SRAM Compiler and extraction of post-layout wiring delays for back-annotation to Verilog simulator.

Synthesis Libraries

The Design System contains the Synopsys Technology and Symbol libraries. The Technology library supports synthesis, timing and area optimization and technology mapping for the Hi-IQ library. The Symbol library contains the symbol graphics information for Hi-IQ library cells needed by the Synopsys schematic generator.

Simulation Library

The Verilog library includes gate-level simulation models for all the compiled SRAMs.

The Design System supports delay annotation to Verilog for gate level simulation. Prior to placement and routing, delay estimates are made using statistical estimates based on net loading and base array size. Post-layout annotation uses delays computed from the actual routed wire lengths. The user is also able to specify temperature, voltage and process conditions to be used in computing delays.

Design Advisor

The Design Advisor checks that a design obeys all electrical rules required by the Hi-IQ Design System, and provides useful information and statistics for each design. The Advisor can check partial or complete designs. Checking partial designs can be useful in catching design problems at an early stage, or to get summaries of cell utilization for a portion of the design.

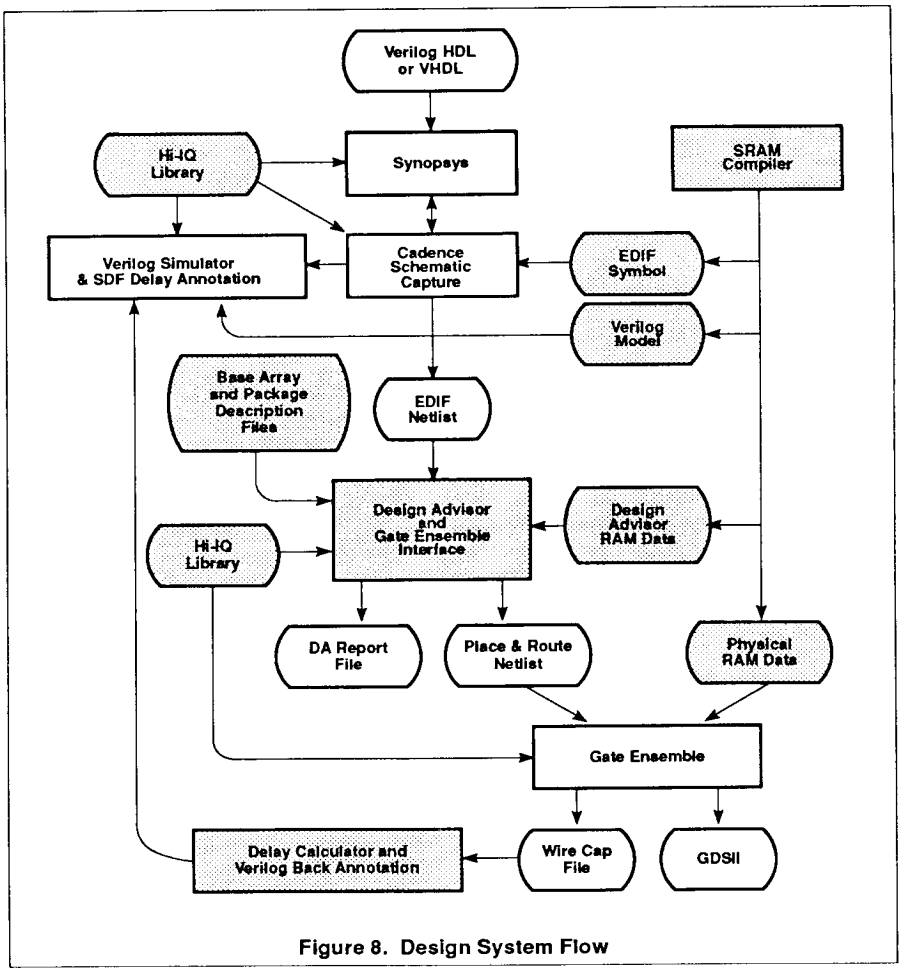


Figure 8. Design System Flow

The input to the design advisor is an EDIF 2 0 0 netlist for the design using cells from the Hi-IQ cell library.

The Advisor generates a report file containing design statistics, and possible error, warning and informational messages. The user is responsible for correcting all errors reported by the Design Advisor; all errors must be corrected before the user can proceed to the next step, place and route.

Place and Route

Place and Route is supported using Cadence's Gate Ensemble tools, and the Hi-IQ library in Gate Ensemble format. The major options and capabilities of Gate Ensemble are fully supported, namely clock tree synthesis and power distribution.

The Place and Route portion of the Design System accepts the same EDIF 2 0 0 netlist read by the Design Advisor.

CELL LIBRARY

The macro cell library contains the specifications for all the hard macros available for Hi-IQ arrays. A hard macro is created using one or more of the CBA compute and drive cells. The macro cell library is divided into three functional groups. The first contains all the input and output cells including clock drivers, the second contains all combinational cells and third the sequential cells. Following is the list of macro cells with different drives available in the library and the number of compute and drive cells required to implement them.

x,y = Number of compute and drive cells used for macro cell.

– = Version not available

NAME	DESCRIPTION	I/Os
INPUT BUFFERS		
bic1a1	CMOS input buffer	
bic1b1	CMOS inverting input buffer	
bit1a1	TTL input buffer	
bit1b1	TTL inverting input buffer	
bits1a1	TTL schmitt input buffer	
bics1a1	CMOS schmitt input buffer	
bits1a1	TTL inverting schmitt input buffer	
bics1a1	CMOS inverting schmitt input buffer	
CLOCK BUFFERS		
bct1a1	TTL clock buffer, strength-1	
bct1a2	TTL clock buffer, strength-2	
bcc1a1	CMOS clock buffer, strength-1	
bcc1a2	CMOS clock buffer, strength-2	
bcc2a1	Internal clock buffer, strength-1	
bcc2a2	Internal clock buffer, strength-2	
OUTPUT BUFFERS		
bo1a4	4mA output buffer, slew-1	
bo2a4	4mA output buffer, slew-2	
bo3a4	4mA output buffer, slew-3	
bo1a8	8mA output buffer, slew-1	
bo2a8	8mA output buffer, slew-2	
bo3a8	8mA output buffer, slew-3	
bo1a12	12mA output buffer, slew-1	
bo2a12	12mA output buffer, slew-2	
bo3a12	12mA output buffer, slew-3	
bo1a24	24mA output buffer, slew-1	
bo2a24	24mA output buffer, slew-2	
bo3a24	24mA output buffer, slew-3	
TRI-STATE BUFFERS		
bt1a4	4mA 3-state output buffer, slew-1	
bt2a4	4mA 3-state output buffer, slew-2	
bt3a4	4mA 3-state output buffer, slew-3	
bt1a8	8mA 3-state output buffer, slew-1	
bt2a8	8mA 3-state output buffer, slew-2	
bt3a8	8mA 3-state output buffer, slew-3	
bt1a12	12mA 3-state output buffer, slew-1	
bt2a12	12mA 3-state output buffer, slew-2	
bt3a12	12mA 3-state output buffer, slew-3	
bt1a24	24mA 3-state output buffer, slew-1	
bt2a24	24mA 3-state output buffer, slew-2	
bt3a24	24mA 3-state output buffer, slew-3	

BI-DIRECTIONAL BUFFERS

bbt1a4	4mA bi-directional output buffer, slew-1
bbt2a4	4mA bi-directional output buffer, slew-2
bbt3a4	4mA bi-directional output buffer, slew-3
bbt1a8	8mA bi-directional output buffer, slew-1
bbt2a8	8mA bi-directional output buffer, slew-2
bbt3a8	8mA bi-directional output buffer, slew-3
bbt1a12	12mA bi-directional output buffer, slew-1
bbt2a12	12mA bi-directional output buffer, slew-2
bbt3a12	12mA bi-directional output buffer, slew-3
bbt1a24	24mA bi-directional output buffer, slew-1
bbt2a24	24mA bi-directional output buffer, slew-2
bbt3a24	24mA bi-directional output buffer, slew-3

COMBINATIONAL MACROS

NAME	DESCRIPTION	DRIVE STRENGTH			
		0	1	2	4
BUFFERS					
buf1a	Non-inverting internal buffer	–	1,1	2,1	3,2
tri1a	Non-inverting internal 3-state buffer	–	3,1	4,1	5,2
tri1b	Inverting internal 3-state buffer	–	3,1	4,1	–
inv1a	Inverting internal buffer	1,0	1,1	1,1	2,2
AND GATES					
and2a	2-input AND gate	2,0	2,1	2,1	–
and2b	2-input AND gate, one input inverted	2,0	2,1	2,2	–
and2c	2-input AND gate, two inputs inverted	1,0	1,1	1,2	–
and3a	3-input AND gate	2,0	2,1	2,1	–
and3b	3-input AND gate, one input inverted	3,0	3,1	–	–
and3c	3-input AND gate, two inputs inverted	3,0	3,1	–	–
and3d	3-input AND gate, three inputs inverted	2,0	2,1	–	–
and4a	4-input AND gate	3,0	3,1	3,1	–
and4b	4-input AND gate, one input inverted	3,0	4,1	4,2	–
and4c	4-input AND gate, two inputs inverted	–	4,1	4,2	–
and4d	4-input AND gate, three inputs inverted	–	5,1	5,2	–
and4e	4-input AND gate, four inputs inverted	–	3,1	–	–
and5a	5-input AND gate	–	4,1	4,2	–
and5b	5-input AND gate, one input inverted	–	4,1	4,2	–
and5c	5-input AND gate, two inputs inverted	–	4,1	4,2	–
and5d	5-input AND gate, three inputs inverted	–	4,1	4,2	–
and5e	5-input AND gate, four inputs inverted	–	4,1	4,1	–
and5f	5-input AND gate, five inputs inverted	–	5,1	5,1	–
and6a	6-input AND gate	–	4,1	4,2	–
and8a	8-input AND gate	–	5,1	5,2	–

NAME	DESCRIPTION	DRIVE STRENGTH			
		0	1	2	4
NAND GATES					
nand2a	2-input NAND gate	1,0	1,1	1,2	–
nand2b	2-input NAND gate, one input inverted	2,0	2,1	2,2	–
nand2c	2-input NAND gate, two inputs inverted	2,0	2,1	2,1	–
nand3a	3-input NAND gate	3,0	3,1	3,1	–
nand3b	3-input NAND gate, one input inverted	3,0	3,1	3,1	–
nand3c	3-input NAND gate, two inputs inverted	2,0	2,1	2,2	–
nand3d	3-input NAND gate, two inputs inverted	4,0	4,1	4,1	–
nand4a	4-input NAND gate	–	3,1	–	–
nand4b	4-input NAND gate, one input inverted	–	4,1	4,1	–
nand4c	4-input NAND gate, two inputs inverted	3,0	3,1	3,1	–
nand4d	4-input NAND gate, three inputs inverted	–	4,1	4,2	–
nand4e	4-input NAND gate, four inputs inverted	3,0	3,1	3,2	–
nand5a	5-input NAND gate	–	4,1	4,1	–
nand5b	5-input NAND gate, one input inverted	–	4,1	4,1	–
nand5c	5-input NAND gate, two inputs inverted	–	4,1	4,2	–
nand5d	5-input NAND gate, three inputs inverted	–	4,1	4,2	–
nand5e	5-input NAND gate, four inputs inverted	–	4,1	4,2	–
nand5f	5-input NAND gate, five inputs inverted	–	4,1	4,2	–
nand6a	6-input NAND gate	–	5,1	5,1	–
nand8a	8-input NAND gate	–	6,1	6,1	–
OR GATES					
or2a	2-input OR gate	2,0	2,1	2,1	–
or2b	2-input OR gate, one input inverted	2,0	2,1	2,2	–
or2c	2-input OR gate, two inputs inverted	1,0	1,1	1,2	–
or3a	3-input OR gate	4,0	4,1	4,1	–
or3b	3-input OR gate, one input inverted	2,0	2,1	2,2	–
or3c	3-input OR gate, two inputs inverted	3,0	3,1	3,1	–
or3d	3-input OR gate, three inputs inverted	3,0	3,1	3,1	–
or4a	4-input OR gate	3,0	3,1	3,2	–
or4b	4-input OR gate, one input inverted	4,0	4,1	4,2	–
or4c	4-input OR gate, two inputs inverted	3,0	3,1	3,1	–
or4d	4-input OR gate, three inputs inverted	–	4,1	4,1	–
or4e	4-input OR gate, four inputs inverted	–	3,1	–	–
or5a	5-input OR gate	–	4,1	4,2	–
or5b	5-input OR gate, one input inverted	–	4,1	4,2	–
or5c	5-input OR gate, two inputs inverted	–	4,1	4,2	–
or5d	5-input OR gate, three inputs inverted	–	4,1	4,2	–
or5e	5-input OR gate, four inputs inverted	–	4,1	4,1	–
or5f	5-input OR gate, five inputs inverted	–	4,1	4,1	–
or6a	6-input OR gate	–	4,1	4,2	–

NAME	DESCRIPTION	DRIVE STRENGTH			
		0	1	2	4
NOR GATES					
nor2a	2-input NOR gate	1,0	1,1	1,2	–
nor2b	2-input NOR gate, one input inverted	2,0	2,1	2,2	–
nor2c	2-input NOR gate, two inputs inverted	2,0	2,1	2,1	–
nor3a	3-input NOR gate, one input inverted	2,0	2,1	–	–
nor3b	3-input NOR gate, two inputs inverted	3,0	3,1	–	–
nor3c	3-input NOR gate, two inputs inverted	3,0	3,1	–	–
nor3d	3-input NOR gate, three inputs inverted	2,0	2,1	2,1	–
nor4a	4-input NOR gate	–	3,1	–	–
nor4b	4-input NOR gate, one input inverted	–	5,1	5,2	–
nor4c	4-input NOR gate, two inputs inverted	–	4,1	4,2	–
nor4d	4-input NOR gate, three inputs inverted	3,0	4,1	4,2	–
nor4e	4-input NOR gate, four inputs inverted	3,0	3,1	3,1	–
nor5a	5-input NOR gate	–	5,1	5,1	–
nor5b	5-input NOR gate, one input inverted	–	4,1	4,1	–
nor5c	5-input NOR gate, two inputs inverted	–	4,1	4,2	–
nor5d	5-input NOR gate, three inputs inverted	–	4,1	4,2	–
nor5e	5-input NOR gate, four inputs inverted	–	4,1	4,2	–
nor5f	5-input NOR gate, five inputs inverted	–	4,1	4,2	–
nor6a	6-input NOR gate	–	5,1	5,1	–
XOR GATES					
xor2a	2-input XOR gate	2,0	2,1	2,1	–
xor2b	2-input XOR gate, one input inverted	2,0	2,1	2,1	–
xor3a	3-input XOR gate	–	4,1	4,1	–
xor3b	3-input XOR gate, one input inverted	–	4,1	4,1	–
xnor2a	2-input XNOR gate	–	2,1	2,1	–
xnor3a	3-input XOR gate	–	4,1	4,1	–
ANDOR_GATES					
ao1a	and2a into or2a	2,0	2,1	2,1	–
ao1b	and2b into or2a	3,0	3,1	–	–
ao1c	and2c into or2a	2,0	3,1	–	–
ao1d	and2a into or2b	2,0	2,1	2,2	–
ao1e	and2b into or2b	2,0	3,1	–	–
ao1f	and2c into or2b	2,0	2,1	–	–
ao2a	and2a into or3a	3,0	3,1	3,1	–
ao2b	and2b into or3a	3,0	3,1	3,1	–
ao2d	and2a into or3b	–	3,1	3,1	–
ao2e	and2b into or3b	–	4,1	4,1	–
ao2f	and2c into or3b	–	4,1	4,1	–
ao3a	and3a into or2a	3,0	3,1	3,1	–
ao3b	and3b into or2a	3,0	3,1	3,1	–
ao3c	AND3C into or2a	–	4,1	4,1	–
ao3d	AND3D into or2a	–	4,1	4,1	–
ao3e	and3a into or2b	3,0	3,1	3,2	–
ao4a	and2a, and2a into or2a	3,0	3,1	3,1	–
ao4b	and2b, and2a into or2a	3,0	3,1	3,1	–
ao4d	and2b, and2b into or2a	–	4,1	4,1	–
ao4f	and2c, and2c into or2a	2,0	4,1	–	–
ao5a	and3a, and2a into or2a	–	3,1	3,1	–
ao5b	and3b, and2a into or2a	–	4,1	4,1	–
ao6a	mAjority gate	3,0	3,1	3,1	–

NAME	DESCRIPTION	DRIVE STRENGTH			
		0	1	2	4
ORAND_GATES					
oa1a	or2a into and2a	2,0	2,1	2,1	–
oa1b	or2b into and2a	3,0	3,1	3,1	–
oa1c	or2c into and2a	2,0	3,1	–	–
oa1d	or2a into and2b	2,0	2,1	2,2	–
oa1e	or2b into and2b	2,0	3,1	–	–
oa1f	or2c into and2b	2,0	2,1	–	–
oa2a	or2a into and3a	3,0	3,1	3,1	–
oa2b	or2b into and3a	3,0	3,1	3,1	–
oa2c	or2c into and3a	–	4,1	–	–
oa2d	or2a into and3b	3,0	3,1	3,1	–
oa3a	or3a into and2a	3,0	3,1	3,1	–
oa3b	or3b into and2a	3,0	3,1	3,1	–
oa3e	or3a into and2b	3,0	3,1	3,2	–
oa4a	or2a, or2a into and2a	3,0	3,1	3,1	–
oa4b	or2b, or2a into and2a	3,0	3,1	3,1	–
oa5a	or3a, or2a into and2a	–	3,1	3,1	–
oa5b	or3b, or2a into and2a	–	4,1	4,1	–
XOR INTO GATES					
xa1a	xor2a into and2a	3,0	3,1	3,1	–
xa1b	xor2b into and2a	3,0	3,1	3,1	–
xa1d	xor2b into and2b	3,0	3,1	3,2	–
ax1a	and2a into xor2a	3,0	3,1	3,1	–
MULTIPLEXERS					
mx2a	2:1 Mux	3,0	3,1	3,1	–
mx2d	2:1 Mux, inverting output	2,0	2,1	2,1	–
mx3a	3:1 Mux	–	4,1	4,1	–
mx4a	4:1 Mux	–	5,1	5,1	–
ADDERS					
ha1a	1 bit half adder	4,0	4,2	–	–
fa1a	1 bit full adder	–	6,2	6,2	–
fa2a	1 bit full adder, C_{OUT} inverted	–	6,2	6,2	–

SEQUENTIAL MACROS

LATCHES					
ld1a	D latch	–	2,1	2,1	–
ld1b	D latch, low enable	–	2,1	2,1	–
ld1c	D latch, low output	–	3,1	3,1	–
ld2a	D latch, low clear	–	3,1	3,1	–
ld2b	D latch, low clear and enable	–	3,1	3,1	–
ldm1a	Scan latch	–	4,1	4,1	–
ldm1b	Scan latch, low enable	–	4,1	4,1	–
ldm1c	Scan latch, low output	–	4,1	4,1	–
ldm2a	Scan latch, low clear	–	4,1	4,1	–
ldm2b	Scan latch, low clear and enable	–	4,1	4,1	–
ldm2c	Scan latch, low clear, low output	–	5,1	5,1	–

NAME	DESCRIPTION	DRIVE STRENGTH			
		0	1	2	4
FLIP FLOPS					
fd1a	D flip flop	–	3,1	3,1	–
fd1b	D flip flop, low clock	–	3,1	3,1	–
fd1c	D flip flop, low output	–	3,1	3,1	–
fd2a	D flip flop, low clear	–	4,1	4,1	–
fd4a	D flip flop, low clear and preset	–	6,1	6,1	–
fdm1a	Scan flip flop	–	5,1	5,1	–
fdm1b	Scan flip flop, low clock	–	5,1	5,1	–
fdm1c	Scan flip flop, low output	–	5,1	5,1	–
fdm1e	Scan flip flop, D0 inverted	–	5,1	5,1	–
fdm1i	Scan flip flop, D1 inverted	–	5,1	5,1	–
fdm2a	Scan flip flop, low clear	–	6,1	6,1	–
fdm5a	3:1 Mux D flip flop	–	6,1	6,1	–
fde1a	Enable flip flop	–	5,1	5,1	–
fde2a	Enable flip flop, low clear	–	6,1	6,1	–

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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