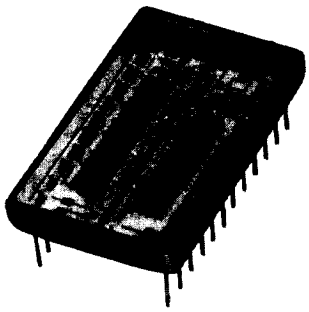
12 BIT 35NSEC HYBRID D/A CONVERTER
Video Speed Settling; Low Glitch



FEATURES

- *FAST SETTLING: 35 NSEC TO 0.02%*
- *LOW GLITCH: 50 MV·NSEC*
- *PIN FOR PIN REPLACES HDS 1250 TYPES AT LOWER POWER*
- *–55°C TO +125°C OPERATING TEMPERATURE*
- *HIGH RELIABILITY 4,000,000 HOUR MTBF*
- *HERMETICALLY SEALED 24 DDIP PACKAGE*

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DESCRIPTION

The DDC–1250 is a 12 bit 35 nanosecond hybrid D/A converter packaged in a hermetically sealed 24 DDIP. It is a pin for pin replacement for HDS 1250 types. Featuring –55°C to +125°C operating temperature range, 50 mV • nsec glitch under optimum conditions, and an MTBF of 4,000,000 hours, the DDC–1250 is offered with MIL-STD-883B screening. Other features include TTL logic compatibility and internal precision DC reference.

APPLICATIONS

With its small size, wide operating temperature range and hermetically sealed package, the DDC-1250 is ideal for the most demanding military and industrial requirements. Its high speed and low glitch are well suited for numerous CRT display applications, including TV and radar video reconstruction and vector stroke X-Y deflection. Additional applications include high speed A/D converters and waveform generators.

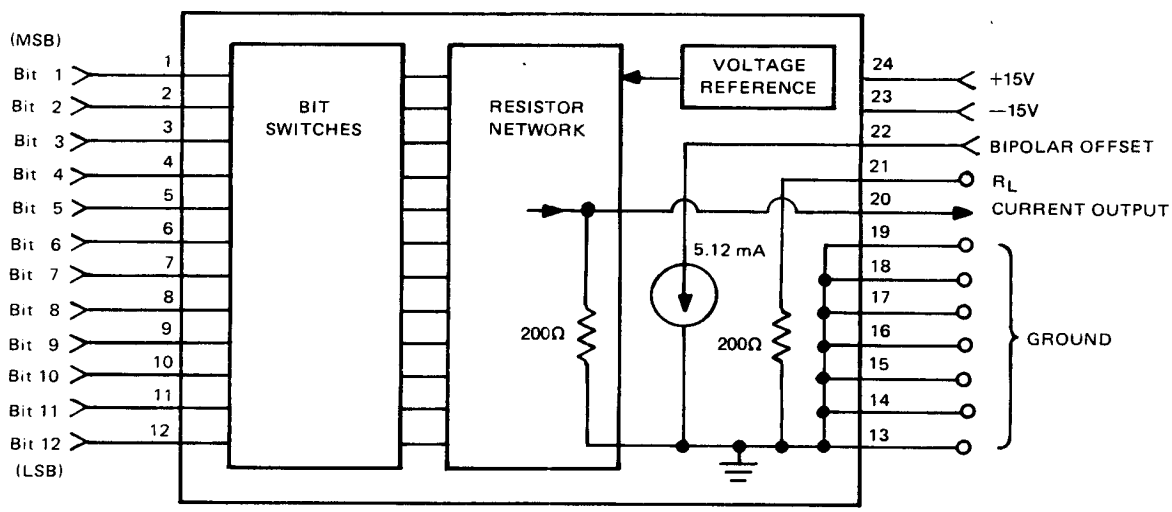


FIGURE 1. DDC-1250 BLOCK DIAGRAM

SPECIFICATIONS
Typical values at 25°C and at nominal power supply voltages unless otherwise noted.

PARAMETER	UNITS	VALUE 10 BIT LIN	VALUE 12 BIT LIN
RESOLUTION	bits	12	12
ACCURACY			
Linearity Error (Max.)	% F.S.R.	±0.05	±0.012
Linearity Tempco	ppm/°C	±3	±3
Gain Error (1)	% F.S.R.	±0.1	±0.05
Gain Tempco	ppm/°C	30	30
Zero Offset (Max)	nA	30	15
Offset Tempco			
Unipolar	ppm/°C	3	3
Bipolar	ppm/°C	15	15
Monotonocity		Guaranteed	
DYNAMIC CHARACTERISTICS (1)			
Settling Time (2)			
Current	nsec	35	
Voltage	nsec	60	
Glitch Energy (3)	mV • nsec	50	
DIGITAL INPUTS			
Logic Compatibility		TTL and 5V CMOS	
Voltage Input			
Logic "1"	V	+2 to +7.0	
Logic "0"	V	0 to +0.8	
Current Load			
Logic "1"	μA	1	
Logic "0"	μA	15	
Coding			
Unipolar		Binary	
Bipolar		Offset Binary	
OUTPUT			
Current			
Unipolar	mA	0 to +10.24	
Bipolar	mA	±5.12	
Voltage (1)			
Unipolar	V	0 to +1.024	
Bipolar	V	±0.512	
Compliance	V	−2 to +1.5	
Impedance	Ω	200	
POWER SUPPLIES			
Voltages	V	+14.5 to +15.5	−12 to −16
Current (Max)	mA	35	15
Power Supply			
Rejection Ratio	%/V	0.2	0.2
TEMPERATURE RANGE			
Operating (Case)			
−1 Option	°C	−55 to +125	
−3 Option	°C	0 to +70	
Storage	°C	−65 to +150	
PHYSICAL			
Package		24 pin DDIP	
Size	in (mm)	1.3x0.8x0.2 (33x20.3x5.1)	
Weight	oz. (g)	0.4 (11.3)	

Notes:
1. With internal 200 ohm R_L connected to output.
2. Full scale change to within 0.02% of final value.
3. With zero input logic skew and DAC logic threshold adjustment.

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the DDC-1250. Functional elements of the DAC include bit switches, a precision thin film resistor network, a DC voltage reference, a current source and a load resistor.

TTL compatible bit switches are used to steer equally weighted currents to either the resistor network or ground. The resistor network contains a precision R/2R ladder, which produces binarily weighted currents at the putput. The combination of equally weighted currents and R/2R ladder network yields the optimum fast settling and low glitch performance.

The precision DC voltage reference is used, along with bias resistors in the thin film network, to program the bit switch currents. The voltage reference also provides the bias for the 5.12 mA current source, which is used to generate a bipolar output. For a unipolar output the resistor network provides an output current of zero to +10.24 mA. When the bipolar offset current is connected to the output, ±5.12 mA is provided. The 200 ohm load resistor is provided as a convenient way to implement a zero to +1 volt output voltage swing. If other output voltages are required, the 200 ohm internal resistor may not be connected and an external load resistor will be used.

DYNAMIC CHARACTERISTICS AND GLITCH

The DDC-1250 is designed for fast settling operation, along with low output glitch. This is achieved by using equally weighted current mode switches and a binarily weighted R/2R ladder network. For a full scale input code change, the output current settles to within 0.02% of final value within 35 nanoseconds. Output glitch area of 50 mV • nsec can be achieved with zero input logic skew and adjustment of the DAC logic threshold.

All DACs exhibit output glitch when major carry code changes are made. Glitch is the response to a momentary erroneous code which occurs due to the input data skew and unequal bit switch turn on/off times. Glitch energy, rather than glitch amplitude, is used as a basis of comparison because it is the product of amplitude and time, and is therefore independent of bandwidth considerations. Glitch energy is defined as the net area contained under the glitch waveform.

To minimize DDC-1250 glitch area, great care was taken in design and layout to minimize unequal bit switch turn on and turn off times. To maintain this low glitch performance, care must be taken to keep input data skew as small as possible. The use of input latches, preferably LS logic types, placed close to the DAC is a good way to minimize data skew. Further reduction of output glitch can be achieved by monitoring the glitch as the +15 volt supply is varied slightly. Variation of the +15 volt supply causes small changes in the input logic switching threshold and therefore acts like a data skew trim.

INPUT CODING

The DDC-1250 requires Binary coded input data for unipolar analog outputs. Offset Binary input data is required

for bipolar analog outputs. Figure 2 illustrates the input coding for various analog outputs with each of the code configurations. It is to be noted that for unipolar operation +FS is equal to +10.24 mA. For bipolar operation +FS is equal to +5.12 mA and −FS is equal to −5.12 mA.

ANALOG OUTPUT RANGES

The DDC-1250 may be configured for a current output of either zero to +10.24 mA or ±5.12 mA. The output voltage corresponding to these currents depends on the equivalent resistance from the output to ground. Figure 3 illustrates the 3 most commonly used analog output ranges, along with the required connections for Bipolar Offset and R_L.

External load resistors can be used to obtain other output voltage ranges, as long as the compliance voltage limits are adhered to. The output voltage range is calculated by multiplying the output current times the parallel combination of external load resistance and 200 ohm internal resistance. External load resistors are typically metal film types. The load resistor tempco should be less than 100 ppm/°C since it directly affects DAC gain tempco.

EXTERNAL OP AMP

If a voltage output swing is required that is larger than the compliance voltage limits of the DDC-1250, then an external op amp can be used. Figure 4 illustrates the connection required to interface the DAC and the op amp. The selection of an appropriate op amp will depend primarily on the settling time requirements of the application. The op amp should be placed as close as possible to the DAC to minimize stray capacitance and inductive affects.

The output voltage range is calculated by multiplying the DAC output current times R_f. DAC output current will be either zero to +10.24 mA or ±5.12 mA, depending on the connection of the Bipolar Offset pin. The R_L pin should not be connected, since this would lower the loop gain of the op amp.

OFFSET TRIM

Some applications may require a lower output offset than the DDC-1250 exhibits after factory adjustment. This will be true only for bipolar output applications, since the offset for unipolar operation is a small fraction of 1 LSB. Figure 5 illustrates the connections required to trim the DDC-1250 offset to zero. A mulit-turn trimpot, with a temperature coefficient less than 100 ppm/°C, is recommended for best performance.

OUTPUT COMPLIANCE

Output compliance is the maximum voltage swing that is allowed on the current output pin. Voltages outside of this range will cause gross errors at the output. Permanent damage may result from externally applied voltages greater than the output compliance range. The DDC-1250 has an output compliance voltage range of −2 volts to +1.5 volts. An example of a violation of the output compliance spec is if the DDC-1250 is connected for unipolar operation with the internal R_L not connected. This configuration will result in an output voltage range of zero to +2.048 V, which is an out of spec condition.

LAYOUT PRECAUTIONS

Care must be taken in the printed circuit layout to achieve the optimum performance of the DDC-1250. To minimize

UNIPOLAR BINARY	BIPOLAR OFFSET BINARY	SCALE
1111 1111 1111	1111 1111 1111	+FS −1 LSB
1100 0000 0000	1110 0000 0000	+3/4 FS
1000 0000 0000	1100 0000 0000	+1/2 FS
0000 0000 0001	1000 0000 0001	+1 LSB
0000 0000 0000	1000 0000 0000	0
	0111 1111 1111	−1 LSB
	0100 0000 0000	−1/2 FS
	0010 0000 0000	−3/4 FS
	0000 0000 0000	−FS

FIGURE 2. INPUT CODING

OUTPUT RANGE	CONNECT BIPOLAR PIN 22 TO	CONNECT R_L PIN 21 TO	OUTPUT IMPEDANCE
0 to +10.24 mA 0 to +1.024 V	PIN 19	PIN 20	100 Ω
±5.12 mA ±1.024 V	PIN 20	N/C	200 Ω
±5.12 mA ±0.512 V	PIN 20	PIN 20	100 Ω

FIGURE 3. ANALOG OUTPUT RANGES

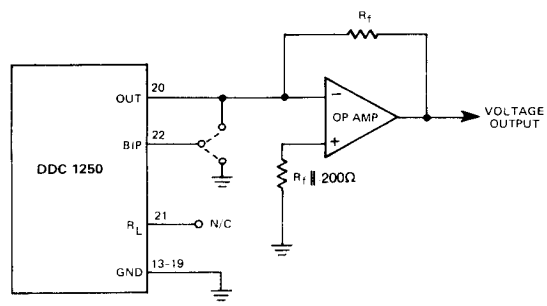


FIGURE 4. EXTERNAL OP AMP

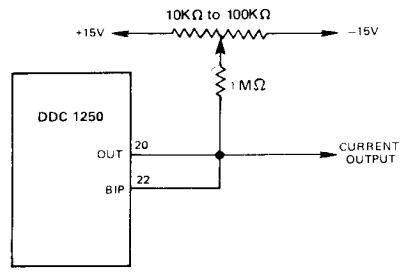


FIGURE 5. OFFSET TRIM

crosstalk and inductive effects, digital input lines and analog output lines should be separated from each other, and made as short as possible. To minimize ground noise, particular attention must be paid to achieving a low impedance ground path. A large area ground plane under the DAC is recommended for best results. Interface circuits such as input latches and output op amp should be placed as close as possible to the DAC.

POWER SUPPLY DECOUPLING

Capacitive decoupling of all power supplies is recommended to minimize noise. Tantalum or electrolytic capacitors of 1 μf or greater will filter out low frequency noise. Ceramic capacitors of 0.01 μf or greater will filter out high frequency noise. For best results, all capacitors should be placed as close to the DAC as possible.

RELIABILITY

The DDC-1250 is manufactured in accordance with the requirements of MIL-STD-883. Screening is based upon the requirements of Method 5008, except for burn-in which is optional.

Thick film and thin film circuits, as well as careful thermal design, have resulted in a very low calculated failure rate for the DDC-1250. The predicted MTBF is 4,000,000 hours, in accordance with MIL-HDBK-217C at +25°C in ground fixed applications.

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	13	GND
2	BIT 2	14	GND
3	BIT 3	15	GND
4	BIT 4	16	GND
5	BIT 5	17	GND
6	BIT 6	18	GND
7	BIT 7	19	GND
8	BIT 8	20	OUTPUT
9	BIT 9	21	R_L (200Ω)
10	BIT 10	22	BIPOLAR OFFSET
11	BIT 11	23	−15V
12	BIT 12 (LSB)	24	+15V

ORDERING INFORMATION

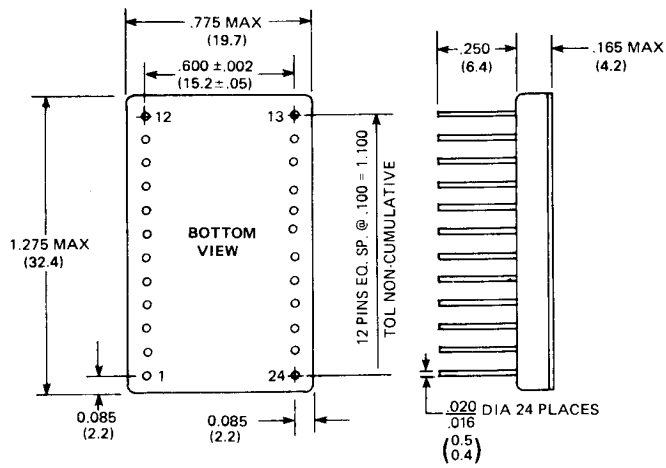
DDC-1250 – 12 – 1 – 883B

Reliability Grade:
- 883B = Fully compliant with MIL-STD-883.
- —B = Screened to MIL-STD-883 but without QCI testing.
- Blank = Screened to MIL-STD-883 but without pre burn-in testing, burn-in, and QCI testing.

Operating Temperatures Range (Case):
- 1 = −55°C to +125°C
- 3 = 0°C to +70°C

Linearity:
- 10 = ±.05%
- 12 = ±.012%

MECHANICAL OUTLINE



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

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