# CMOS Programmable Synchronous State Machine

## Features

- Twelve I/O macrocells each having:
  - registered, three-state I/O pins
  - input register clock select multiplexer
  - feed back multiplexer
  - output enable (OE) multiplexer
- All twelve macrocell state registers can be hidden
- User-configurable state registers—JK, RS, T, or D
- One input multiplexer per pair of I/O macrocells allows I/O pin associated with a hidden macrocell state register to be saved for use as an input
- Four dedicated hidden registers
- Eleven dedicated, registered inputs
- Three separate clocks—two inputs, one output
- Common (pin 14–controlled) or product term–controlled output enable for each I/O pin
- 256 product terms—32 per pair of macrocells, variable distribution
- Global, synchronous, product term–controlled, state register set and reset—inputs to product term are clocked by input clock
- 66-MHz operation
  - 3-ns input set-up and 12-ns clock to output
  - 15-ns input register clock to state register clock
- Low power
  - 130 mA $I_{CC}$
- 28-pin, 300-mil DIP, LCC
- Erasable and reprogrammable

## Functional Description

The CY7C330 is a high-performance, erasable, programmable, logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance synchronous state machines.

The unique architecture of the CY7C330, consisting of the user-configurable output macrocell, bidirectional I/O capability, input registers, and three separate clocks, enables the user to design high-performance state machines that can communicate either with each other or with microprocessors over bidirectional parallel buses of user-definable widths.

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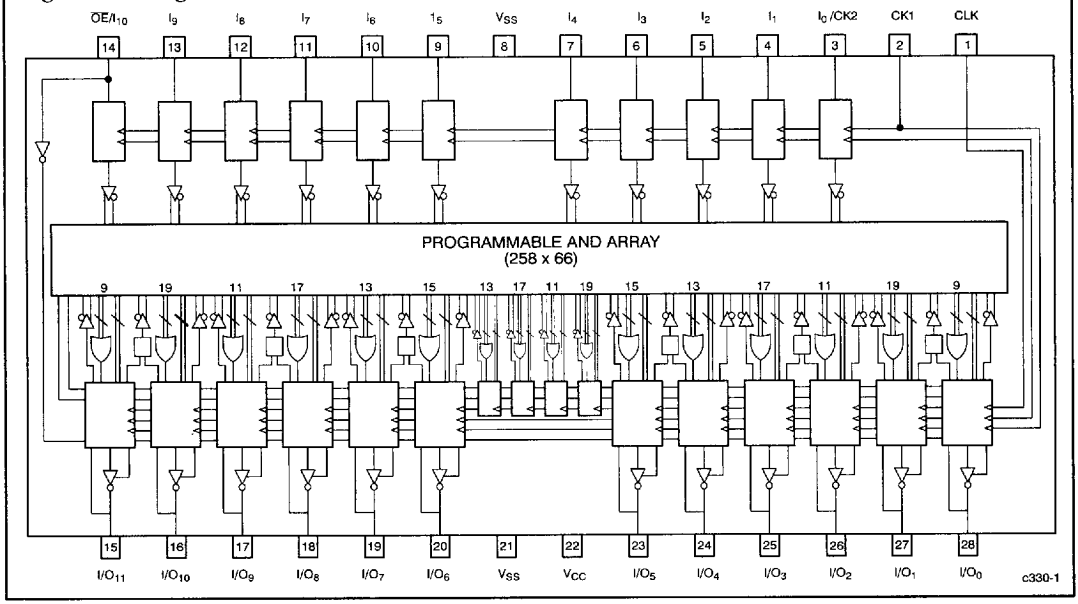
## Logic Block Diagram

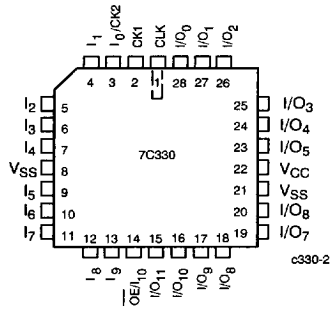



## Selection Guide

| | | 7C330–66 | 7C330–50 | 7C330–40 | 7C330–33 | 7C330–28 |
|---|---|---|---|---|---|---|
| Maximum Operating Frequency, $f_{MAX}$ (MHz) | Commercial | 66.6 | 50.0 | | 33.3 | |
| | Military | | 50.0 | 40.0 | | 28.5 |
| Power Supply Current $I_{CC1}$ (mA) | Commercial | 140 | 130 | | 130 | |
| | Military | | 160 | 150 | | 150 |

## Pin Configuration

LCC/PLCC
Top View




## Functional Description (continued)

Three separate clocks permit independent, synchronous state machines to be synchronized to each other. The two input clocks, C1, C2, enable the state machine to sample input signals that may be generated by another system and that may be available on its bus for a short period of time.

The user-configurable state register flip-flops enable the designer to designate JK-, RS-, T-, or D-type devices, so that the number of product terms required to implement the logic is minimized.

The major functional blocks of the CY7C330 are (1) the input registers and (input) clock multiplexers, (2) the EPROM (AND) cell array, (3) the twelve I/O macrocells and (4) the four hidden registers.

### Input Registers and Clock Multiplexers

There are a total of eleven dedicated input registers. Each input register consists of a D flip-flop and a clock multiplexer. The clock multiplexer is user-programmable to select either CK1 or CK2 as the clock for the flip-flop. CK2 and $\overline{OE}$ can alternatively be used as inputs to the array. The twenty-two outputs of the registers (i.e., the Q and $\overline{Q}$ outputs of the input registers) drive the array of EPROM cells.

An architecture configuration bit (C4) is reserved for each dedicated input register cell to allow selection of either input clock CK1 or CK2 as the input register clock for each dedicated input cell. If the CK2 clock is not needed, that input may also be used as a general-purpose array input. In this case the input register for this input can only be clocked by input clock CK1. *Figure 1* illustrates the dedicated input cell composed of an input register, an Input Clock Multiplexer, and architecture configuration bit C4 which determines the input clock selected.

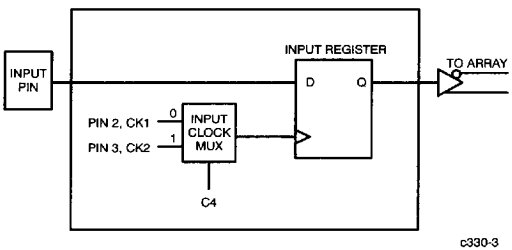



**Figure 1. Dedicated Input Cell**

### I/O Macrocell

The logic diagram of CY7C330 I/O macrocell is shown in *Figure 2* There are a total of twelve identical macrocells.

Each macrocell consists of:

– An Output State register that is clocked by the global state counter clock, CLK (Pin 1). The state register can be configured as a D, JK, RS, or T flip-flop (default is a D-type flip-flop). Polarity can be controlled in the D flip-flop implementation by use of the exclusive or function. Data is sampled on the LOW to HIGH clock transition. All of the state registers have a common reset and set which are controlled synchronously by Product Terms which are generated in the EPROM cell array.

– A Macrocell Input register that may be clocked by either the CK1 or CK2 input clock as programmed by the user with architecture configuration bit C2, which controls the I/O Macrocell Input Clock Multiplexer. The Macrocell Input registers are initialized upon power-up such that all of the Q outputs are at logic LOW level and the $\overline{Q}$ outputs are at a logic HIGH level.

– An Output Enable Multiplexer (OE), which is user programmable using architecture configuration bit C0, can select either the common $\overline{OE}$ signal from pin 14 or, for each cell individually, the signal from the output enable product term associated with each macrocell. The output enable input signal to the array product term is clocked through the input register by the selected input register clock, CK1 or CK2.

– An Input Feedback Multiplexer, which is user programmable, can select either the output of the state register or the output of the Macrocell Input register to be fed back into the array. This option is programmed by architecture configuration bit C1. If the output of the Macrocell Input register is selected by the Feedback Multiplexer, the I/O pin becomes bidirectional.

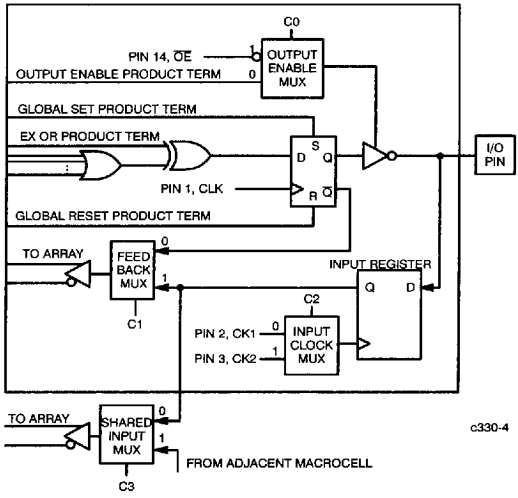



**Figure 2. Macrocell and Shared Input Multiplexer**

## Functional Description (continued)

### Macrocell Input Multiplexer

Each pair of I/O macrocells share a Macrocell Input Multiplexer that selects the output of one or the other of the pair's input registers to be fed to the input array. This multiplexer is shown in *Figure 2*. The Macrocell Input Multiplexer allows the input pin of a macrocell, for which the state register has been hidden by feeding back its input to the input array to be preserved for use as an input pin. This is possible as long as the other macrocell of the pair is not needed as an input or does not require state register feedback. The input pin input register output that would normally be blocked by the hidden state register feedback can be routed to the array input path of the companion macrocell for use as array input.

### State Registers

By use of the exclusive OR gate, the state register may be configured as a JK-, RS-, or T-type register. The default is a D-type register. For the D-type register, the exclusive OR function can be used to select the polarity or the register output.

The set and reset of the state register are global synchronous signals. They are controlled by the logic of two global product terms, for which input signals are clocked through the input registers by either of the input clocks, CK1 or CK2.

### Hidden Registers

In addition to the twelve macrocells, which contain a total of twenty-four registers, there are four hidden registers whose outputs are not brought out to the device output pins. The Hidden State Register Macrocell is shown in *Figure 3*.

The four hidden registers are clocked by the same clock as the macrocell state registers. All of the hidden register flip-flops have a common, synchronous set, S, as well as a common, synchronous reset, R, which override the data at the D input. The S and R signals are product terms that are generated in the array and are the same signals used to preset and reset the state register flip-flops.

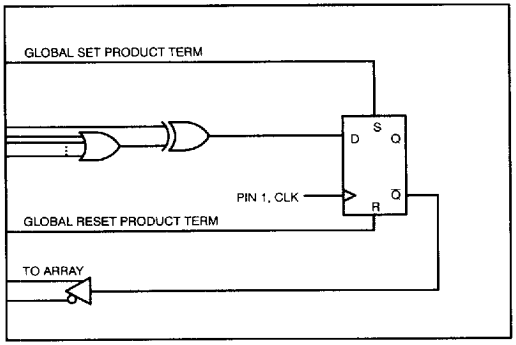



**Figure 3. Hidden State Register Macrocell**

### Macrocell Product Term Distribution

Each pair of macrocells has a total of thirty-two product terms. Two product terms of each macrocell pair are used for the output enables (OEs) for the two output pins. Two product terms are also used as one input to each of the two exclusive OR gates in the macrocell pair. The number of product terms available to the designer is then 32 − 4 = 28 for each macrocell pair. These product terms are divided between the macrocell state register flip-flops as show in *Table 1*.

**Table 1. Product Term Distribution for Macrocell State Register Flip-Flops**

| Macrocell | Pin Number | Product Terms |
|---|---|---|
| 0 | 28 | 9 |
| 1 | 27 | 19 |
| 2 | 26 | 11 |
| 3 | 25 | 17 |
| 4 | 24 | 13 |
| 5 | 23 | 15 |
| 6 | 20 | 15 |
| 7 | 19 | 13 |
| 8 | 18 | 17 |
| 9 | 17 | 11 |
| 10 | 16 | 19 |
| 11 | 15 | 9 |

### Hidden State Register Product Term Distribution

Each pair of hidden registers also has a total of 32 product terms. Two product terms are used as one input to each of the exclusive OR gates. However, because the register outputs do not go to any output pins, output enable product terms are not required. Therefore, 30 product terms are available to the designer for each pair of hidden registers. The product term distribution for the four hidden registers is shown in *Table 2*.

**Table 2. Product Term Distribution for Hidden Registers**

| Hidden Register Cell | Product Terms |
|---|---|
| 0 | 19 |
| 1 | 11 |
| 2 | 17 |
| 3 | 13 |

### Architecture Configuration Bits

The architecture configuration bits are used to program the multiplexers. The function of the architecture bits is outlined in *Table 3*.

**Table 3. Architecture Configuration Bits**

| Architecture Configuration Bit | | Number of Bits | Value | Function |
|---|---|---|---|---|
| C0 | Output Enable Select MUX | 12 Bits, 1 per I/O Macrocell | 0—Virgin State | Output Enable Controlled by Product Term |
| | | | 1—Programmed | Output Enable Controlled by Pin 14 |
| C1 | State Register Feedback MUX | 12 Bits, 1 per I/O Macrocell | 0—Virgin State | State Register Output is Fed Back to Input Array |
| | | | 1—Programmed | I/O Macrocell is Configured as an Input and Output of Input Register is Fed to Array |
| C2 | I/O Macrocell Input Register Clock Select MUX | 12 Bits, 1 per I/O Macrocell | 0—Virgin State | CK1 Input Register Clock (Pin 2) is Connected to I/O Macrocell Input Register Clock Input |
| | | | 1—Programmed | CK2 Input Register Clock (Pin 3) is Connected to I/O Macrocell Input Register Clock Input |
| C3 | I/O Macrocell Pair Input Select MUX | 6 Bits, 1 per I/O Macrocell Pair | 0—Virgin State | Selects Data from I/O Macrocell Input Register of Macrocell A of Macrocell Pair |
| | | | 1—Programmed | Selects Data from I/O Macrocell Input Register of Macrocell B of Macrocell Pair |
| C4 | Dedicated Input Register Clock Select MUX | 11 Bits, 1 per Dedicated Input Cell | 0—Virgin State | CK1 Input Register Clock (Pin 2) is Connected to Dedicated Input Register Clock Input |
| | | | 1—Programmed | CK2 Input Register Clock (Pin 3) is Connected to Dedicated Input Register Clock Input |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 12 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Programming Voltage ..... 13.0V

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +75°C | 5V ± 10% |
| Military[1] | −55°C to +125°C | 5V ± 10% |

**Note:**

1. $T_A$ is the "instant on" case temperature.

## Electrical Characteristics Over the Operating Range[2]

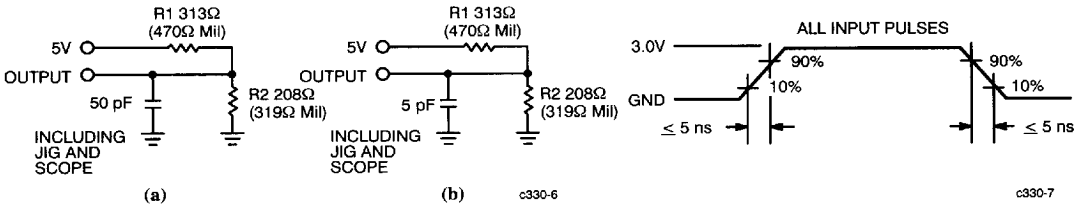
| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −3.2 mA (Com'l), $I_{OH}$ = −2 mA (Mil) | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$,<br>$I_{OL}$ = 12 mA (Com'l), $I_{OH}$ = 8 mA (Mil) | | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Logical HIGH Voltage for all Inputs[3] | | 2.2 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Logical LOW Voltage for all Inputs[3] | | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $V_{SS}$ < $V_{IN}$ < $V_{CC}$, $V_{CC}$ = Max. | | −10 | +10 | μA |
| $I_{OZ}$ | Output Leakage Current | $V_{CC}$ = Max., $V_{SS}$ < $V_{OUT}$ < $V_{CC}$, | | −40 | +40 | μA |
| $I_{SC}$[4] | Output Short Circuit Current | $V_{CC}$ = Max., $V_{OUT}$ = 0.5V[5] | | −30 | −90 | mA |
| $I_{CC1}$ | Standby Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND<br>Outputs Open | Commercial −66 | | 140 | mA |
| | | | Commercial −33, −50 | | 130 | |
| | | | Military −50 | | 160 | |
| | | | Military −28, −40 | | 150 | |
| $I_{CC2}$ | Power Supply Current at Frequency[4,6] | $V_{CC}$ = Max.<br>Outputs Disabled<br>(in High Z State),<br>Device Operating at $f_{MAX}$<br>External ($f_{MAX1}$) | Commercial −66 | | 180 | mA |
| | | | Commercial −33, −50 | | 160 | |
| | | | Military −50 | | 200 | |
| | | | Military −28, −40 | | 180 | |

## Capacitance[4]

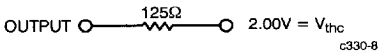
| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V at f = 1 MHz, | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V at f = 1 MHz, | | 10 | pF |

**Notes:**
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT}$ = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Tested by periodic sampling of production product.

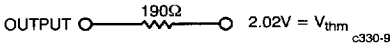
## AC Test Loads and Waveforms



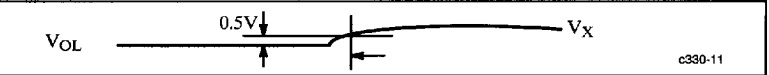
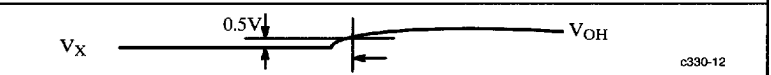
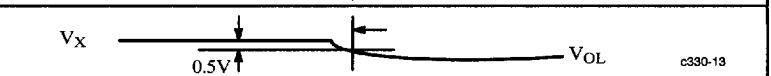
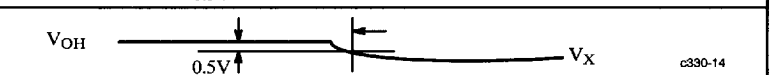
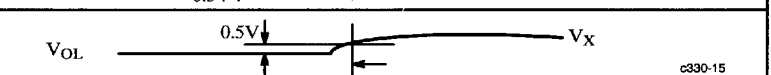
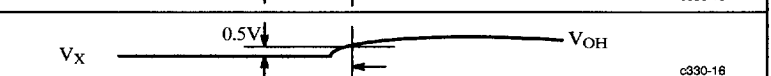
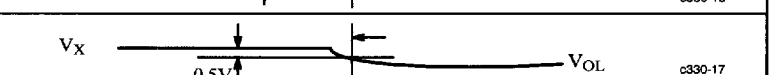

Equivalent to: THÉVENIN EQUIVALENT (Commercial)




Equivalent to: THÉVENIN EQUIVALENT (Military)



## AC Test Loads and Waveforms (continued)

| Parameter | Vx | Output Waveform—Measurement Level |
|---|---|---|
| $t_{PXZ(-)}$ | 1.5V |   |
| $t_{PXZ(+)}$ | 2.6V |   |
| $t_{PZX(+)}$ | $V_{thc}$ |   |
| $t_{PZX(-)}$ | $V_{thc}$ |   |
| $t_{CER(-)}$ | 1.5V |   |
| $t_{CER(+)}$ | 2.6V |   |
| $t_{CEA(+)}$ | $V_{thc}$ |   |
| $t_{CEA(-)}$ | $V_{thc}$ |   |

**(c) Test Waveforms and Measurement Levels**

## Switching Characteristics Over the Operating Range[2, 7]

| | | Commercial | | | | | | Military | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | −66 | | −50 | | −33 | | −50 | | −40 | | −28 | | |
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Unit |
| $t_{IS}$ | Input or Feedback Set-Up Time to Input Register Clock | 3 | | 5 | | 10 | | 5 | | 5 | | 10 | | ns |
| $t_{OS}$ | Input Register Clock to Output Register Clock | 15 | | 20 | | 30 | | 20 | | 25 | | 35 | | ns |
| $t_{CO}$ | Output Register Clock to Output Delay | | 12 | | 15 | | 20 | | 15 | | 20 | | 25 | ns |
| $t_{IH}$ | Input Register Hold Time | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{CEA}$ | Input Register Clock to Output Enable Delay | | 20 | | 20 | | 30 | | 20 | | 25 | | 35 | ns |
| $t_{CER}$ | Input Register Clock to Output Disable Delay[8] | | 20 | | 20 | | 30 | | 20 | | 25 | | 35 | ns |
| $t_{PZX}$ | Pin 14 Enable to Output Enable Delay | | 20 | | 20 | | 30 | | 20 | | 25 | | 35 | ns |
| $t_{PXZ}$ | Pin 14 Disable to Output Disable Delay[8] | | 20 | | 20 | | 30 | | 20 | | 25 | | 35 | ns |
| $t_{WH}$ | Input or Output Clock Width HIGH[4, 6] | 6 | | 8 | | 12 | | 8 | | 10 | | 15 | | ns |
| $t_{WL}$ | Input or Output Clock Width LOW[4, 6] | 6 | | 8 | | 12 | | 8 | | 10 | | 15 | | ns |

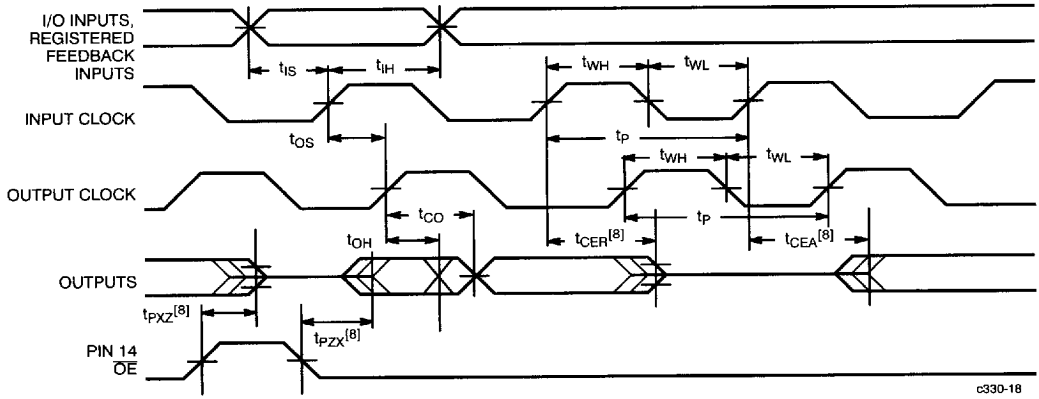
## Switching Characteristics Over the Operating Range[2, 7] (continued)

| Parameter | Description | Commercial | | | | | | Military | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | −66 | | −50 | | −33 | | −50 | | −40 | | −28 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{OH}$ | Output Data Stable Time from Synchronous Clock Input[9] | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{IOH} - t_{IH}$ | Output Data Stable Time This Device Minus I/P Reg Hold Time Same Device[10] | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OH} - t_{IH}$ 33x | Output Data Stable Time Minus I/P Reg Hold Time 7C330 and 7C332 Devices[11] | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_P$ | External Clock Period ($t_{ICO} + t_{IS}$), Input and Output Clock Common | 15 | | 20 | | 30 | | 20 | | 25 | | 35 | | ns |
| $f_{MAX1}$ | Maximum External Operating Frequency ($1/(t_{CO} + t_{IS})$)[12] | 66.6 | | 50.0 | | 33.3 | | 50.0 | | 40.0 | | 28.5 | | MHz |
| $f_{MAX2}$ | Maximum Register Toggle Frequency[6, 13] | 83.3 | | 62.5 | | 41.6 | | 62.5 | | 50.0 | | 33.3 | | MHz |
| $f_{MAX3}$ | Maximum Internal Operating Frequency[14] | 74.0 | | 57.0 | | 37.0 | | 57.0 | | 45.0 | | 30.0 | | MHz |

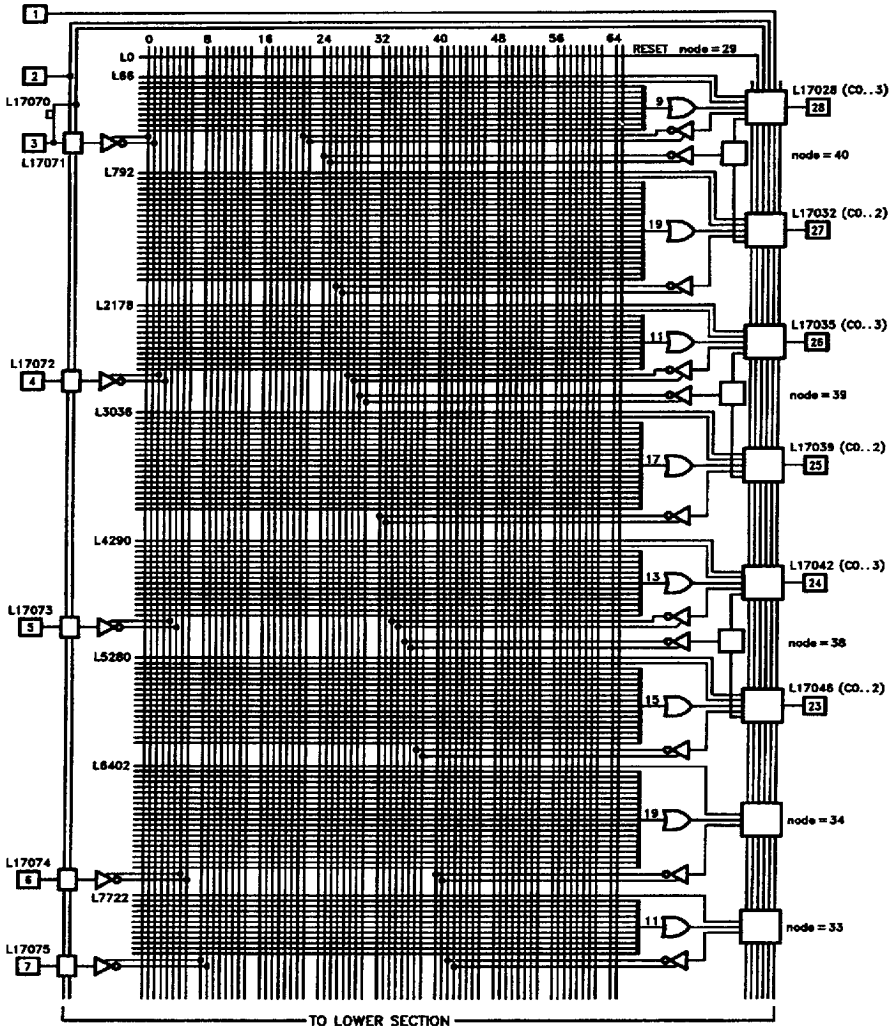
**Notes:**

7. Part (a) of AC Test Loads is used for all parameters except $t_{CEA}$, $t_{CER}$, $t_{PZX}$, and $t_{PXZ}$, which use part (b).
8. This parameter is measured as the time after output register disable input that the previous output data state remains stable on the output. This delay is measure to the point at which a previous HIGH level has fallen to 0.5V below $V_{OH}$ Min. or a previous LOW level has risen to 0.5V above $V_{OL}$ Max. Please see part (c) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
9. This parameter is measured as the time after output register clock input that the previous output data state remains stable on the output.
10. This difference parameter is designed to guarantee that any 7C330 output fed back to its own inputs externally or internally will satisfy the input register minimum input hold time. This parameter is guaranteed for a given individual device and is tested by a periodic sampling of production product.
11. This specification is intended to guarantee feeding of this signal to another 33X family input register cycled by the same clock with sufficient output data stable time to insure that the input hold time minimum of the following input register is satisfied. This parameter difference specification is guaranteed by periodic sampling of production product of 7C330 and 7C332. It is guaranteed to be met only for devices at the same ambient temperature and $V_{CC}$ supply voltage.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
13. This specification indicates the guaranteed maximum frequency at which an individual input or output register can be cycled.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with only internal feedback can operate. This parameter is tested periodically on a sample basis.

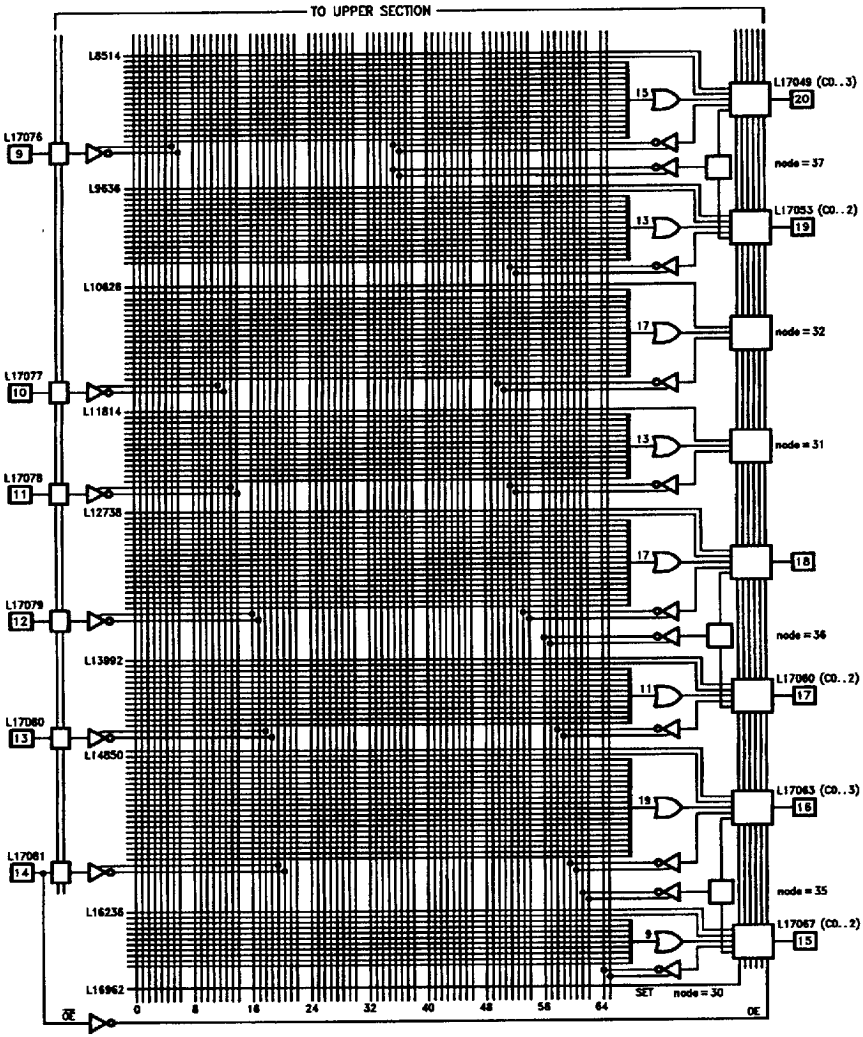
## Switching Waveform



## CY7C330 Logic Diagram (Upper Half)



## CY7C330 Logic Diagram (Lower Half)



## Ordering Information

| $I_{CC1}$ (max) | $f_{MAX}$ (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|---|
| 140 | 66.6 | CY7C330–66HC | H64 | 28-Pin Windowed Leaded Chip Carrier | Commercial |
| | | CY7C330–66JC | J64 | 28-Lead Plastic Leaded Chip Carrier | |
| | | CY7C330–66PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | | CY7C330–66WC | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 160 | 50 | CY7C330–50DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | | CY7C330–50HMB | H64 | 28-Pin Windowed Leaded Chip Carrier | |
| | | CY7C330–50LMB | L64 | 28-Square Leadless Chip Carrier | |
| | | CY7C330–50QMB | Q64 | 28-Pin Windowed Leadless Chip Carrier | |
| | | CY7C330–50TMB | T74 | 28-Lead Windowed Cerpack | |
| | | CY7C330–50WMB | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 130 | 50 | CY7C330–50HC | H64 | 28-Pin Windowed Leaded Chip Carrier | Commercial |
| | | CY7C330–50JC | J64 | 28-Lead Plastic Leaded Chip Carrier | |
| | | CY7C330–50PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | | CY7C330–50WC | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 150 | 40 | CY7C330–40DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | | CY7C330–40HMB | H64 | 28-Pin Windowed Leaded Chip Carrier | |
| | | CY7C330–40LMB | L64 | 28-Square Leadless Chip Carrier | |
| | | CY7C330–40QMB | Q64 | 28-Pin Windowed Leadless Chip Carrier | |
| | | CY7C330–40TMB | T74 | 28-Lead Windowed Cerpack | |
| | | CY7C330–40WMB | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 130 | 33.3 | CY7C330–33HC | H64 | 28-Pin Windowed Leaded Chip Carrier | Commercial |
| | | CY7C330–33JC | J64 | 28-Lead Plastic Leaded Chip Carrier | |
| | | CY7C330–33PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | | CY7C330–33WC | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 150 | 28.5 | CY7C330–28DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | | CY7C330–28HMB | H64 | 28-Pin Windowed Leaded Chip Carrier | |
| | | CY7C330–28LMB | L64 | 28-Square Leadless Chip Carrier | |
| | | CY7C330–28QMB | Q64 | 28-Pin Windowed Leadless Chip Carrier | |
| | | CY7C330–28TMB | T74 | 28-Lead Windowed Cerpack | |
| | | CY7C330–28WMB | W22 | 28-Lead (300-Mil) Windowed CerDIP | |

## MILITARY SPECIFICATIONS
### Group A Subgroup Testing

### DC Characteristics

| Parameter | Subgroups |
|---|---|
| $V_{OH}$ | 1, 2, 3 |
| $V_{OL}$ | 1, 2, 3 |
| $V_{IH}$ | 1, 2, 3 |
| $V_{IL}$ | 1, 2, 3 |
| $I_{IX}$ | 1, 2, 3 |
| $I_{OZ}$ | 1, 2, 3 |
| $I_{CC}$ | 1, 2, 3 |

### Switching Characteristics

| Parameter | Subgroups |
|---|---|
| $t_{IS}$ | 9, 10, 11 |
| $t_{OS}$ | 9, 10, 11 |
| $t_{CO}$ | 9, 10, 11 |
| $t_{CEA}$ | 9, 10, 11 |
| $t_{PZX}$ | 9, 10, 11 |

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