Semiconductor Corporation

CS5030 CS5031

12-Bit, 400 kHz, Sampling A/D Converters

Features

- Monolithic CMOS A/D Converter
  - 0.5µs Track/Hold Amplifier
  - 2µs A/D Converter
  - 2.5V Voltage Reference
  - Flexible Parallel, Serial and Byte interface
- 12-Bit ADC and Reference Accuracy
  - Total Unadjusted Error: ±1/2 LSB
  - Ref Tempco: 1ppm/°C
- Low Distortion
  - Signal-to-Noise Ratio: 72 dB
  - Total Harmonic Distortion: 0.01%
  - Peak Harmonic or Noise: 0.01%
- Low Power: 50mW

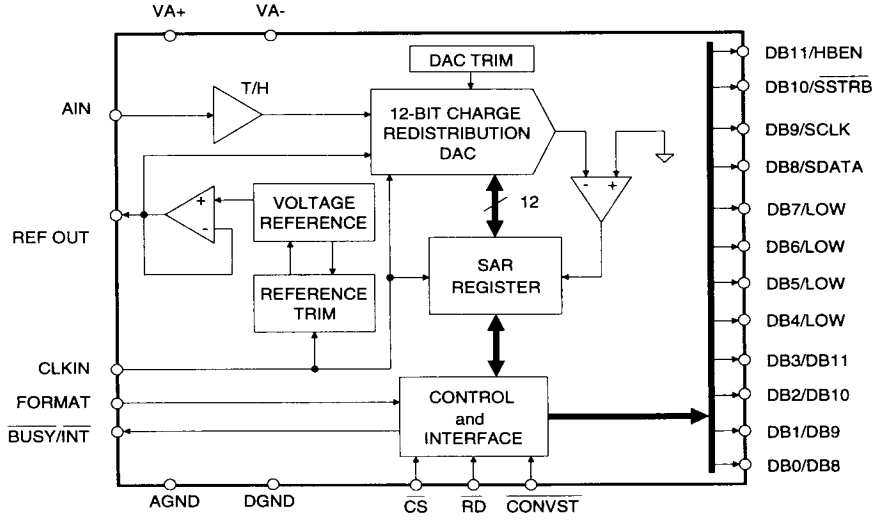
General Description

The CS5030, and CS5031 are complete monolithic CMOS analog-to-digital converters capable of 400 kHz throughput. On-chip calibration circuitry achieves true 12-bit accuracy for the ADC and on-chip reference over the full operating temperature range without external adjustments.

The CS5030/CS5031 have a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data.

The CS5030/CS5031 are available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), Cerdip and small outline (SOIC) package.

ORDERING INFORMATION:
See Page 22



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (VA+ = +5V±5%; VA- = -5V±5%; AGND = DGND = 0V; CLKIN = 10MHz, unless otherwise specified. $T_A = T_{MIN}$ to T_{MAX})

Parameter *		Symbol	B min	B typ	B max	T min	T typ	T max	Units
Specified Temperature Range			-40 to +85			-55 to +125			°C
Accuracy									
Total Unadjusted Error	(Note 1)	TUE			±1			±1	LSB
Differential Nonlinearity		DNL			±1/2			±1/2	LSB
Integral Nonlinearity		INL		1/4			1/4		LSB
Unipolar Offset Error		V_{UP}		1/4			1/4		LSB
Bipolar Offset Error		V_{BP}		1/4			1/4		LSB
Positive Full Scale Error	(Note 2)	FSE_P		1/4			1/4		LSB
Bipolar Negative Full Scale Error	(Note 2)	FSE_N		1/4			1/4		LSB
Dynamic Performance	(Note 3)								
Signal-to-Noise Ratio	(Note 4)	SNR	72			72			dB
Total Harmonic Distortion	(Note 5)	THD			0.01			0.01	%
Peak Harmonic or Spurious Noise	(Note 5)	SPN			0.01			0.01	%
Intermodulation Distortion	(Note 6, 7)	IMD							
Second Order Terms					0.01			0.01	%
Third Order Terms					0.01			0.01	%
Analog Input									
Input Voltage Range									
CS5030		V_{IN}	-2.5		+2.5	-2.5		+2.5	V
CS5031			0		+5	0		+5	V
Aperture Delay		t_{apd}		25			25		ns
Aperture Jitter		t_{apj}		100			100		ps
Input Capacitance	(Note 7)	A_{cin}		10			10		pF
Reference Output									
Output Voltage		V_R	2.499	-	2.501	2.499	-	2.501	v
REF OUT Tempco	(Note 7)			1	±10		1	±10	ppm/°C
Line Regulation	(Note 7, 8)	$\Delta V_R/\Delta I$			±1			±1	mV
Output Noise Voltage		e_N		100			100		μV_{RMS}
Output Current Drive	(Note 7)								
Source Current		I_{SOURCE}			500			500	µA
Sink Current		I_{SINK}			TBD			TBD	µA

* Parameter definitions are given at the end of this datasheet prior to the package outline information.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	B min	B typ	B max	T min	T typ	T max	Units
Specified Temperature Range		-40 to +85			-55 to +125			°C
Conversion & Throughput								
Conversion Time External Clock (CLKIN = 10MHz) Internal Clock	t_{conv}		2.0 TBD			2.0 TBD		µs
Acquisition Time	t_{acq}		0.5			0.5		µs
Throughput	f_{tp}	400			400			kHz
Power Supplies								
Positive Supply Current	I_{DD}		6.0	8.0		6.0	8.0	mA
Negative Supply Current	I_{SS}		5.0	6.0		5.0	6.0	mA
Power Dissipation	P_D			70			70	mW

Notes:
1. TUE is measured using the on-chip reference.
2. Measured with respect to internal reference and includes bipolar offset error.
3. V_{IN} (pk-pk) = ±2.5V (CS5030), 0 → 5V (CS5031)
4. V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 400kHz. Typically 71.5dB for 10kHz<V_{IN}<200kHz.
5. V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 400kHz. Typically -86dB for 0<V_{IN}<200kHz.
6. fa = 9kHz, fb = 9.8kHz, f_{SAMPLE} = 400kHz.
7. Guaranteed by design and/or characterization.
8. Reference Load Current Change (0-500 µA). Reference Load should not be changed during conversion

LSB	%FS	ppm FS	mV
0.25	.0061	61	0.31
0.50	.0122	122	0.61
1.00	.0244	244	1.22
2.00	.0488	488	2.44
4.00	.0976	976	4.88

Unit Conversion Factors: CS5030(VIN = ±2.5V), CS5031 (VIN = 0V to 5V)

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+ = +5V ±5%, VA- = -5V±5%; AGND = DGND = 0V, (Note 9))

Parameter			Symbol	B min	B typ	B max	T min	T typ	T max	Units
Specified Temperature Range				-40 to +85			-55 to +125			°C
CLKIN	Period		t_{clk}	100	-	400	100	-	400	ns
CLKIN	Low Time		t_{clkl}	0.4	-	0.6	0.4	-	0.6	MCC*
CLKIN	High Time		t_{clkh}	0.4	-	0.6	0.4	-	0.6	MCC*
Rise Times	Any Digital Input		t_{rise}	-	-	20	-	-	20	ns
	Any Digital Output		t_{rise}	-	20	-	-	20	-	ns
Fall Times	Any Digital Input		t_{fall}	-	-	20	-	-	20	ns
	Any Digital Output		t_{fall}	-	20	-	-	20	-	ns
Conversion Time			t_{conv}	-	-	20	-	-	20	MCC*
Mode 1 Timing										
$\overline{CONVST}$ Pulse Width			t_{cpw}	50	-	-	50	-	-	ns
$\overline{CS}$ to $\overline{RD}$ Setup Time			t_{css1}	0	-	-	0	-	-	ns
$\overline{RD}$ Pulse Width			t_{rpw1}	60	-	-	75	-	-	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time			t_{csh1}	0	-	-	0	-	-	ns
$\overline{RD}$ to $\overline{INT}$ Delay			t_{rdd}	-	-	70	-	-	70	ns
Data Access Time after $\overline{RD}$		(Note 10)	t_{ra1}	-	-	57	-	-	70	ns
Output Float Delay: $\overline{RD}$ Rising to Hi-Z		(Note 11)	t_{fd1}	5	-	50	5	-	50	ns
HBEN to $\overline{RD}$ Setup Time			t_{hrs}	0	-	-	0	-	-	ns
HBEN to $\overline{RD}$ Hold Time			t_{hrh}	0	-	-	0	-	-	ns
SCLK to $\overline{SSTRB}$ Falling Time		(Note 12)	t_{sss}	25	-	-	25	-	-	ns
Serial Clock Timing										
Serial Clock	Pulse Width High		t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
	Pulse Width Low		t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK to Valid Data		(Note 13)	t_{ss}	-	-	30	-	-	30	ns
SCLK rising to $\overline{SSTRB}$			t_{ssr}	10	-	25	10	-	25	ns
SCLK rising to SDATA Hold Time			t_{sh}	10	-	25	10	-	25	ns

*MCC = Master Clock Cycles, 1 MCC = t_{clk}

Notes:
9. All input signals are specified with $t_{rise} = t_{fall} = 5ns$ (10% to 90% of 5V) and timed from a voltage level of 1.6V.
10. Measured with the load circuits of Figure 5 and defined as the time required for an output to cross 0.8V or 2.4V.
11. Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 6.
12. t_{sss} = MCC/2 - 25. t_{sss} = 25ns for t_{clk} = 100ns.
13. CL = 35pF. SDATA will drive higher capacitive loads but this will add to t_{SS}.

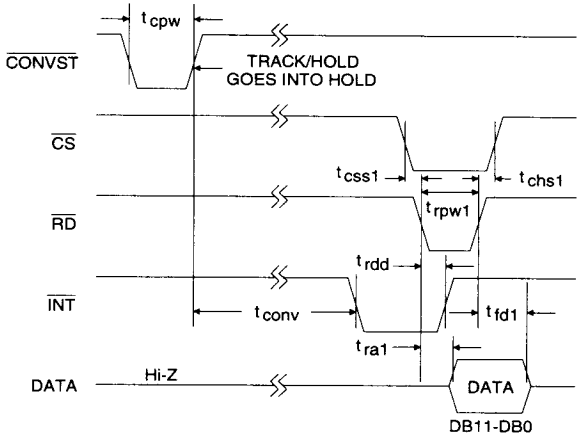
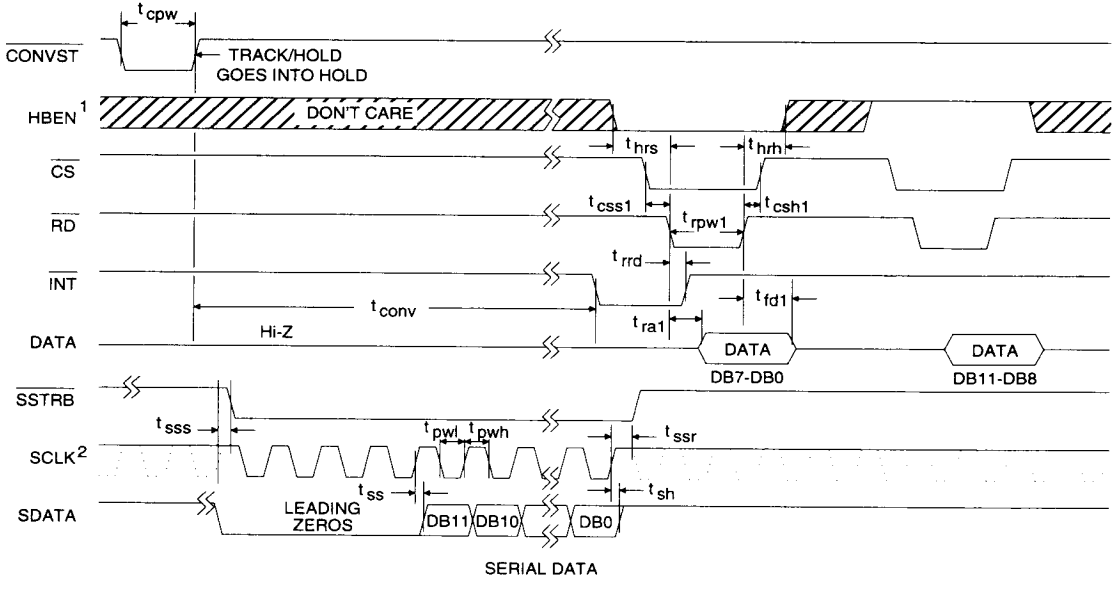


Figure 1. Mode 1 Timing Diagram, 12-Bit Parallel Read



NOTES: 1. Times t_{css1}, t_{rpw1}, t_{csh1}, t_{hrs} and t_{hrh} are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when FORMAT = -5 V
Noncontinuous when FORMAT = O V

Figure 2. Mode 1 Timing Diagram, Byte or Serial Read

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	B min	B typ	B max	T min	T typ	T max	Units
Specified Temperature Range		-40 to +85			-55 to +125			°C
Mode 2 Timing								
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{css2}	10	-	-	10	-	-	ns
$\overline{CS}$ to Busy Delay	t_{cbd}	-	-	75	-	-	75	ns
Data Setup Time	t_{ds}	50	-	-	50	-	-	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{csh2}	0	-	-	0	-	-	ns
Output Float Delay $\overline{RD}$ Rising to Hi-Z	t_{fd2}	5	-	50	5	-	50	ns
HBEN to $\overline{CS}$ Setup Time	t_{hs}	0	-	-	0	-	-	ns
HBEN to $\overline{CS}$ Hold Time	t_{hd}	0	-	-	0	-	-	ns
$\overline{RD}$ Pulse Width	t_{rpw2}	60	-	-	75	-	-	ns
Data Access Time After $\overline{RD}$ (Note 10)	t_{ra2}	-	-	57	-	-	70	ns
Serial Clock Timing								
Serial Clock Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK rising to Valid Data (Note 13)	t_{ss}	-	-	30	-	-	30	ns
SCLK rising to $\overline{SSTRB}$	t_{ssr}	10	-	25	10	-	25	ns
SCLK rising to SDATA Hold Time	t_{sh}	10	-	25	10	-	25	ns

*MCC = Master Clock Cycles, 1 MCC = t_{clk}

Notes: 10. Measured with the load circuits of Figure 5 and defined as the time required for an output to cross 0.8V or 2.4V.

13. CL = 35pF. SDATA will drive higher capacitive loads but this will add to t_{ss}.

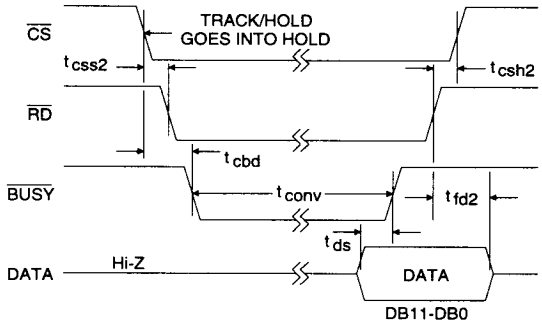
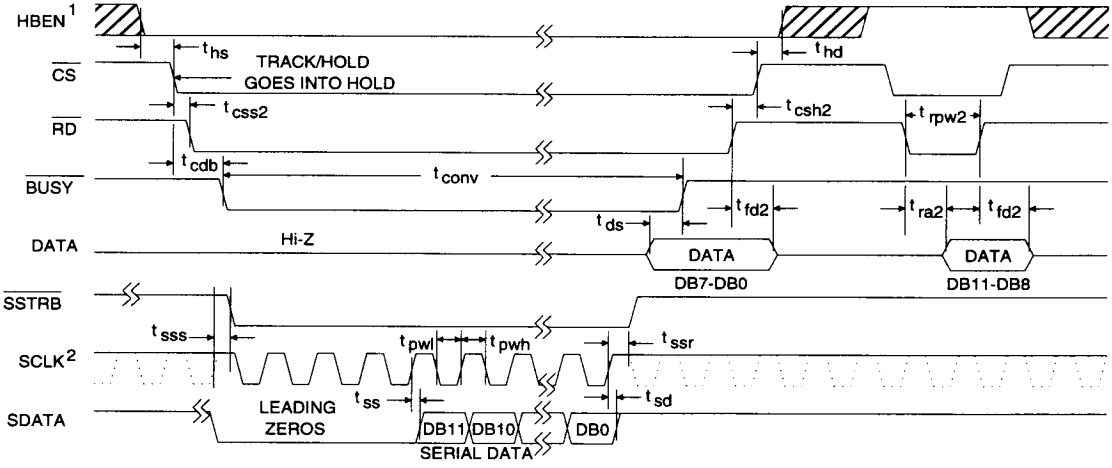


Figure 3. Mode 2 Timing Diagram, 12-Bit Parallel Read



NOTES: 1. Times t_{hs}, t_{sss}, and t_{hd} are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when FORMAT = -5 V
Noncontinuous when FORMAT = O V

Figure 4. Mode 2 Timing Diagram, Byte or Serial Read

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}: VA+ = 5V ± 10%; VA- = -5V ±10%)

Parameter		Symbols	Min	Typ	Max	Units
LOGIC INPUTS						
High-level Input Voltage		V_{IH}	2.0			V
Low-level Input Voltage		V_{IL}			0.8	V
Input leakage current		I_{in}			10	µA
Input Capacitance	(Note 7)	C_{in}			10	pF
LOGIC OUTPUTS						
High-level Output Voltage	(Note 14)	V_{OH}	4.0			V
Low-level Output Voltage	(Note 15)	V_{OL}			0.4	V
DB11-DB0 Floating State leakage Current		I_{OZ}			10	µA
DB11-DB0 Output Capacitance	(Note 7)	C_{out}			15	pF

Notes: 7. Guaranteed by design and/or characterization.
14. I_{source} = -40 µA
15. I_{sink} = 1.6 mA

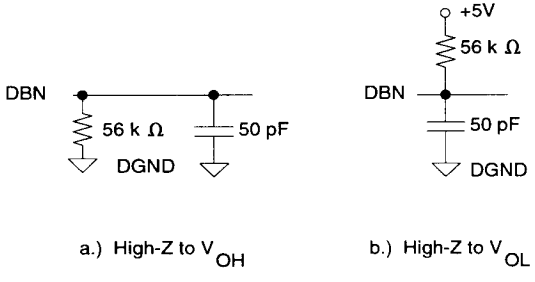


Figure 5. Load Circuits for Access Time

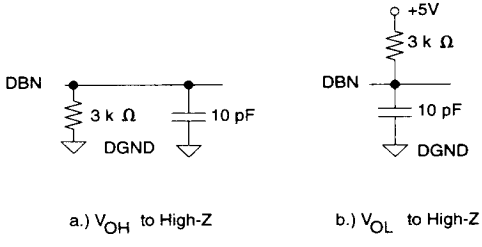


Figure 6. Load Circuits for Output Float Delay

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V. All voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VA+	4.5	5.0	5.5	V
Negative Analog Supply	VA-	-4.5	-5.0	-5.5	V
Analog Input Voltage	A_{in}				
CS5030		-2.5		+2.5	V
CS5031		AGND		5	V

ABSOLUTE MAXIMUM RATINGS* (AGND = 0V, All voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VA+	-0.3		6.0	V
Negative Analog Supply	VA-	0.3		-6.0	V

* WARNING: Operation beyond these limits may result in permanent damage to the device.

GENERAL DESCRIPTION

The CS5030/CS5031 are complete 12-bit 400 kHz sampling ADCs utilizing a successive approximation architecture. External calibration of the capacitive ladder network ensures 14-bit performance from the DAC. The capacitive DAC also acts as an inherent sample/hold while a low drift voltage reference (1ppm/°C) maintains 12-bit accuracy over the operating temperature range. The capacitive DAC calibration combined with the low drift reference ensure that the total unadjusted error from the converter (including reference error) is less than ±1 LSB for the full temperature range. The converters are differentiated by their analog input ranges; ±2.5V (CS5030) and 0V to +5V (CS5031). Output data from the devices is provided in parallel, byte and serial formats.

THEORY OF OPERATION

The CS5030/CS5031 use a charge redistribution architecture to implement the successive approximation algorithm. The DAC comprises an array of binary-weighted capacitors that are optimized during a factory calibration routine to achieve specified performance.

Track and Hold Operation

The track and hold operation in the CS5030/CS5031 is transparent to the user. The hold capacitor is made up of the total capacitive array that implements the switched-capacitive DAC. During tracking mode all the capacitive DAC elements are switched to the analog input which charges the capacitive array. The load capacitance of the entire array during tracking mode is typically 5pF. The input bandwidth of the track/hold is typically 2MHz.

Initiating a conversion causes the capacitor DAC array to behave like a hold capacitor in a sample/hold amplifier.

DAC Calibration

To achieve 12-bit accuracy from the DAC, the CS5030/CS5031 use a novel calibration scheme. Each bit capacitor consists of several capacitors that are manipulated to optimize the overall bit weighting with a resolution of 14-bits. Calibration resolution for the array is a small fraction of an LSB resulting in nearly ideal differential and integral linearity.

The calibration coefficients for the capacitive bit weights are stored in an on-chip EEPROM during factory calibration. When the devices are subsequently powered-up these coefficients are applied immediately to the capacitive DAC. Therefore, the 12-bit accuracy of the DAC is provided automatically on power-up making it unnecessary to calibrate the DAC before using the converter. Additionally, the low temperature coefficient of the capacitor array easily maintains 12-bit accuracy over the full temperature range without recalibration.

Reference Calibration

A first-order corrected bandgap reference, designed for low drift, is the foundation of the reference trim block (Figure 7).

During normal operation of the device, a 16-bit delta-sigma (Δ–Σ) ADC independently monitors the chip's temperature every 200ms. As the temperature varies a segment of the EEPROM is selected based on the Δ–Σ converter's output word. The EEPROM output is used to control the trim DAC which compensates the bandgap reference voltage. This trim circuit maintains the output reference voltage to the ADC and REF OUT pin to within ±200μV of 2.5V over the full temperature range.

During factory calibration the 16-bit Δ-Σ converter takes measurements at several temperature points to establish a profile of the bandgap reference temperature drift. At each

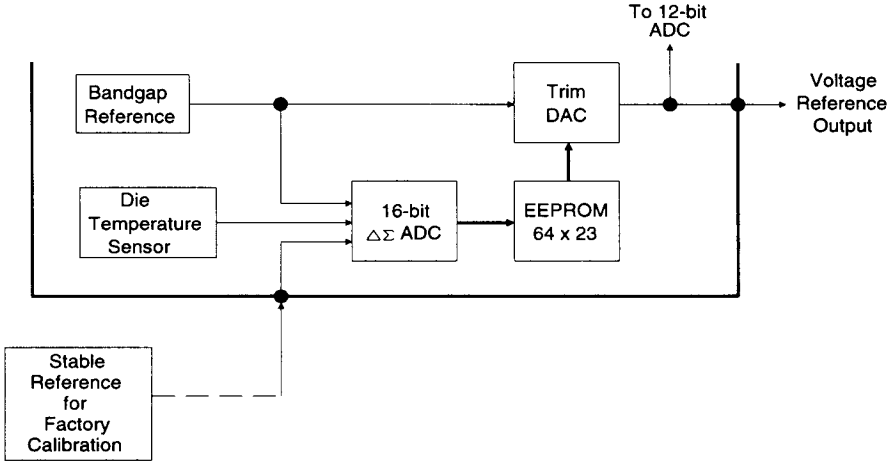


Figure 7. Reference Temperature Control Block

temperature point the Δ–Σ converter calculates the error voltage between an external stable 2.5V reference and the actual bandgap reference voltage (Figure 8a). Additionally, the Δ–Σ converter also measures the absolute temperature of the chip (from an on-chip sensor) as well as it's own offset and gain errors. All of these results are uniquely stored in the device EEPROM to be accessed during final test.

During final test the four 16-bit words associated with each temperature point are downloaded to the tester. The tester performs a trapezoidal approximation in software for each of the temperature segments. Digital words representing temperature, slope and intercept are then downloaded from the tester back into the EEPROM on the chip (Figure 8b).

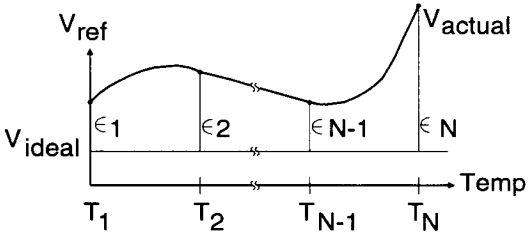


Figure 8a. Untrimmed Reference Voltage versus Temperature

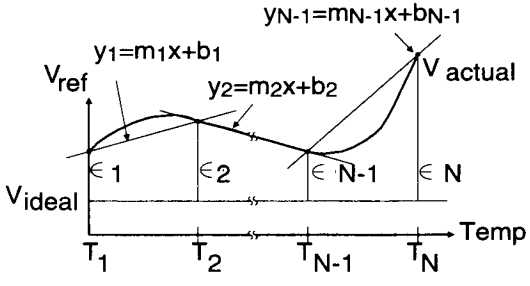


Figure 8b. Slopes and Intercepts are Calculated for the Intermediate Temperatures

In normal operation the reference trim circuit is adjusted with temperature. Depending on the temperature of the chip, the Δ–Σ converter selects the appropriate temperature segment stored in EEPROM. Using the corresponding slope and intercept data for the temperature in question, the appropriate correction factor is provided by the trim DAC to maintain the output voltage reference error within ±200μV of the ideal 2.5V (Figure 8c).

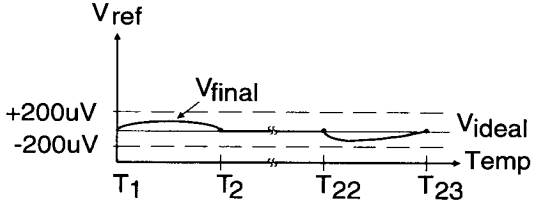


Figure 8c. The Adjusted Reference Error is Within 200μV of 2.5V

The reference voltage is available at the REF OUT pin and is capable of sourcing 500μA to peripheral devices. This pin must be decoupled with a parallel combination of a 10μF tantalum capacitor and a 0.1μF ceramic capacitor.

Upon power-up, the reference will be within 50 mV of the ideal 2.5 V. The full accuracy of the reference is subsequently achieved within 200 ms of power-up after the trim circuitry has completed the calibration of the reference.

OPERATION OVERVIEW

The CS5030/CS5031 family of data converters have different input structures to handle different analog input ranges.

The converters can be used either with an external clock or with the internal clock oscillator.

There are two modes of operation for each of the devices. Conversion can be initiated using $\overline{\text{CONVST}}$ (MODE 1) or by taking $\overline{\text{CS}}$ low while HBEN is low (MODE 2). Parallel, byte or serial data formats are available in both modes.

Analog Input Ranges and Output Coding

The CS5030 converts ± 2.5V input signals. The CS5031 converts a 0V to +5V signal range. The analog input of the CS5030/CS5031 can be modeled as illustrated in Figure 9. The figure shows the device in track mode. During hold mode the input impedance to the device is typically 10MΩ and the various elements of the capacitor DAC array are connected to either AGND or VREF. In switching back from hold mode to track mode some elements in the capacitive array will need to be charged from the analog input. The maximum charging required occurs during consecutive conversions where the analog input value has changed from it's maximum value to the minimum value. For the CS5030, the worst case occurs when the analog input changes from +2.5V to -2.5V. To ensure that the capacitive DAC array has settled to within 0.25 LSB during the allowed acquisition time the source resistance should be less than 4kohm.

The output coding for the CS5030 is 2's complement and is straight binary for CS5031.

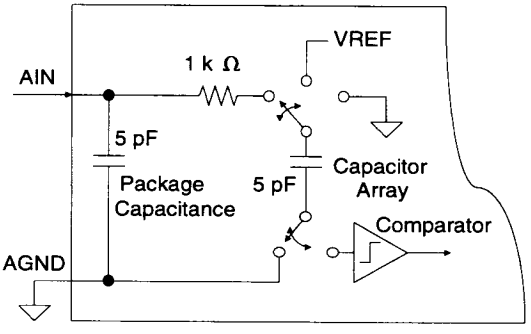


Figure 9. Analog Input Model.

Clock control

Connecting a TTL clock signal to the CLKIN pin allows the converter to work from an external clock. Alternatively, connecting the CLKIN pin to VA- activates an internal clock oscillator. In signal processing applications where precise timing is required it is recommended to run the device with an external clock.

Data Output Formats

The data output format depends on the signal applied to the FORMAT pin. Applying a +5V input selects 12-bit parallel format while a logic low or -5V selects byte and serial output format.

Figure 10a shows the system connection diagram for the converter in 12-bit parallel mode. The 12 bits of data are output simultaneously on DB11 (MSB) through DB0 (LSB).

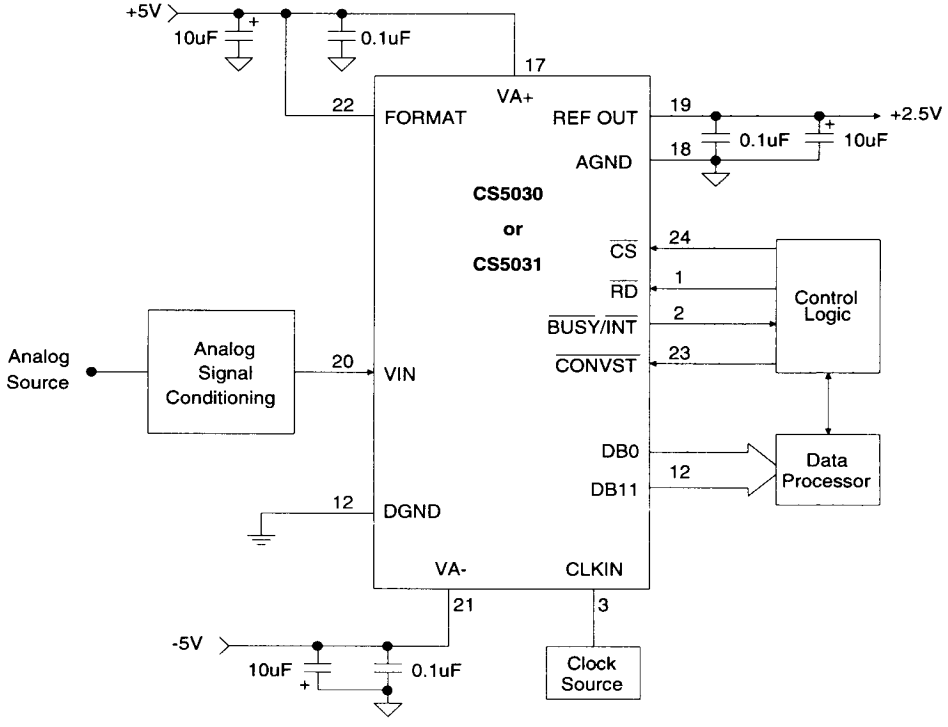


Figure 10a. System Connection Diagram: Parallel Data Format

In byte mode, two read operations (8 + 4) are required to collect the data as shown in figure 10b. For this format, the DB11/HBEN pin defers to the HBEN function to select which byte of data is read from the ADC. The lower 8 bits of data are placed on the databus when HBEN is held low. To access the 4 MSBs of data HBEN must be held high. The 4 MSBs of the 12-bit data word are right justified with zeros in the upper nibble of the high byte (Table 1).

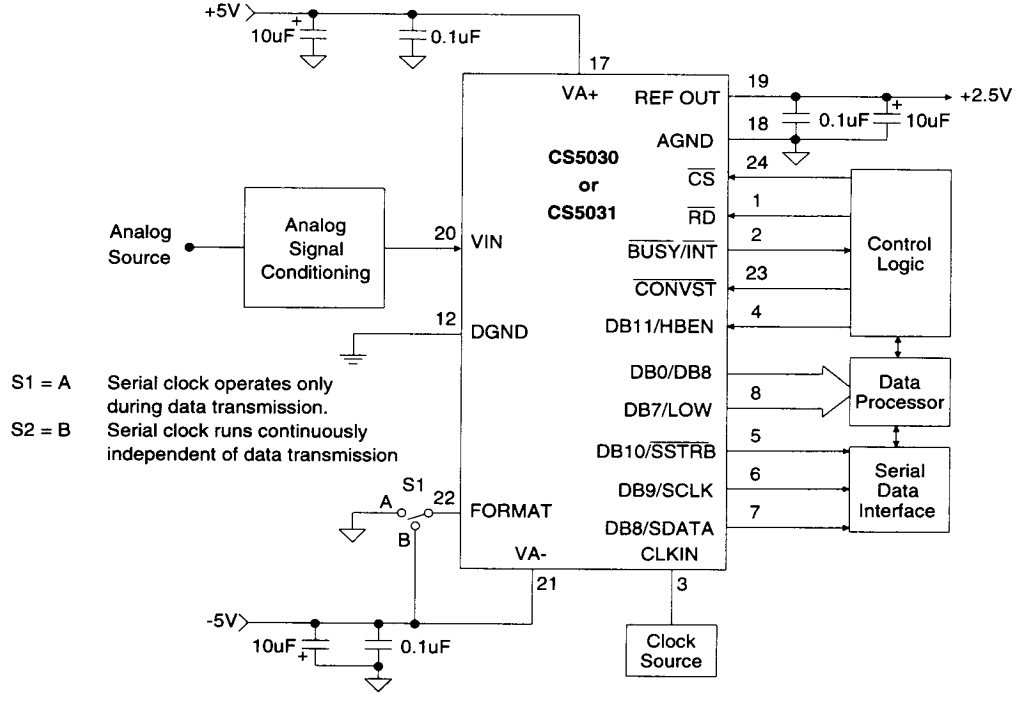


Figure 10b. System Connection Diagram: Serial and Byte Data format

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11/ (MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)

Table 1. Output Data for Byte Interfacing

For serial operation, 0V on the FORMAT input causes the serial clock to run only when data is being clocked out of the device. SCLK is turned off after transmission is completed. If -5V is connected to the FORMAT input SCLK will run continuously independent of data transmission. For serial operation, DB8/SDATA, DB9/SCLK and DB10/$\overline{\text{SSTRB}}$ defer to their serial functions. The serial strobe pin ($\overline{\text{SSTRB}}$) provides a framing signal for serial data. Serial data is available on the SDATA pin when $\overline{\text{SSTRB}}$ falls low (within three clock cycles of $\overline{\text{CONVST}}$). A total of 16 bits (four leading zeros and 12 data bits starting with the MSB) are clocked out on the SDATA pin with the rising edge of SCLK. The data bits become valid on the rising edge of SCLK while $\overline{\text{SSTRB}}$ is low. $\overline{\text{SSTRB}}$ is automatically goes high when the LSB has been clocked out on the SDATA line. Serial data operation is identical for MODE1 and MODE 2.

MODE 1 Operation

In this mode the $\overline{\text{CONVST}}$ signal is used to put the device into hold mode and initiate a conversion. At the end of conversion the device returns to it's tracking mode.

Conversion begins on the rising edge of $\overline{\text{CONVST}}$ provided that $\overline{\text{CS}}$ is high. The BUSY/$\overline{\text{INT}}$ line performs the $\overline{\text{INT}}$ function and can be used to interrupt the microprocessor. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. The ADC begins to acquire the analog input when $\overline{\text{INT}}$ goes low. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{INT}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low in this mode. Data cannot be read during a conversion cycle because the output data latches are disabled while a conversion is in progress.

Figure 11a shows the MODE 1 timing diagram for 12-bit parallel operation (FORMAT = +5V). A data read operation performed at the end of conversion will read all 12 bits of data at the same time.

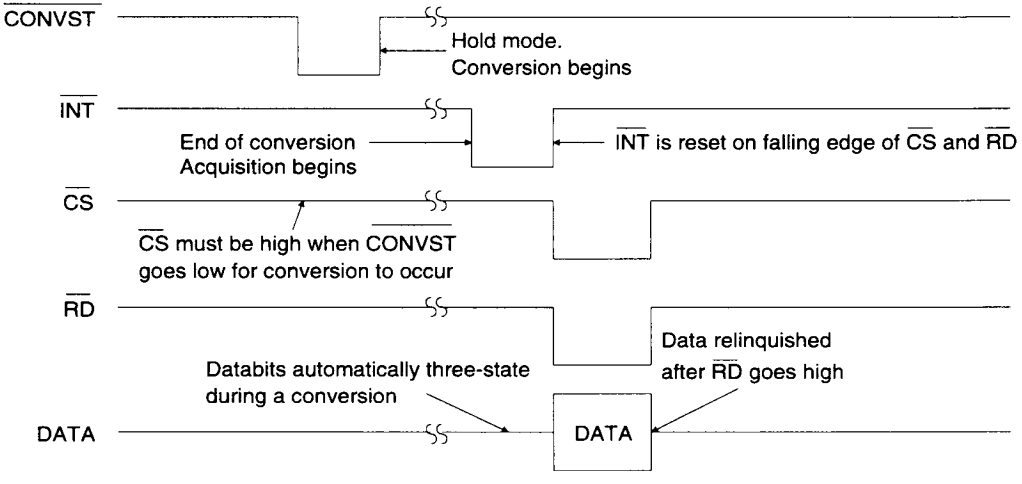
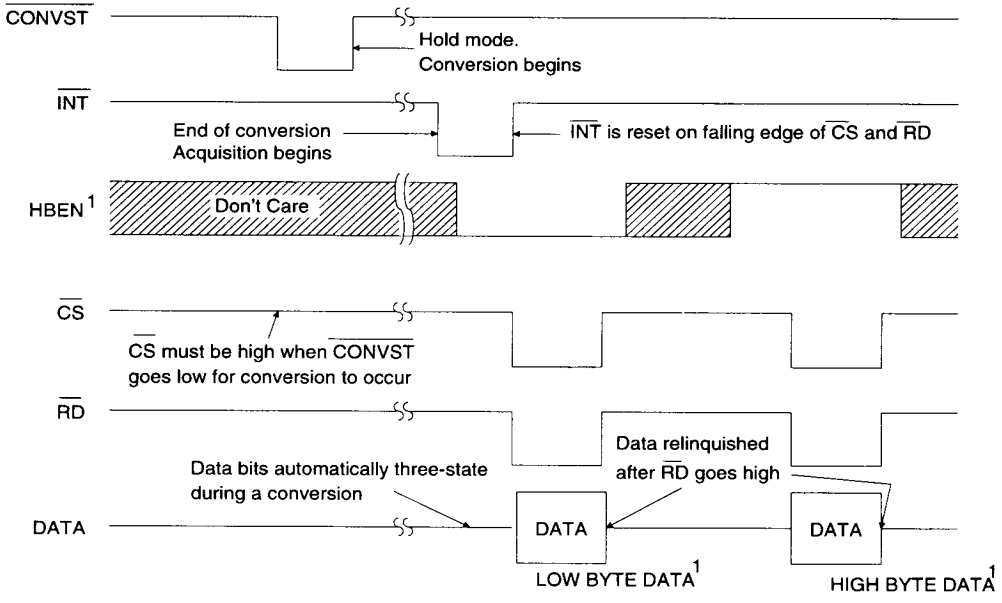


Figure 11a. Mode 1 Timing Diagram, 12-bit Parallel Read

Figure 11b shows the MODE 1 timing diagram for byte operation. At the end of conversion reading the first byte can access either the low byte or high byte of data. The order in which byte selection is made is dictated by the status of HBEN.

The MODE 1 timing diagram for serial operation is shown in figure 11c. Conversion begins on the rising edge of $\overline{\text{CONVST}}$ and data is clocked out immediately upon the falling edge of $\overline{\text{SSTRB}}$ and SDATA. The data is output as four leading zeroes followed by the twelve data bits. The first zero is latched on the first falling edge of SCLK after $\overline{\text{SSTRB}}$ goes low. A total of 16 falling SCLK edges will latch all 16 bits of output data. $\overline{\text{SSTRB}}$ automatically returns high after the last bit of data has been clocked out of the device.



NOTES: 1. In the above diagram HBEN is exercised to read the low byte first(DB7-DB0) and then the high byte (DB11-DB8). To change the order in which the bytes are read, simply invert the HBEN signal shown above.

Figure 11b. Mode 1 Timing Diagram, Byte Read

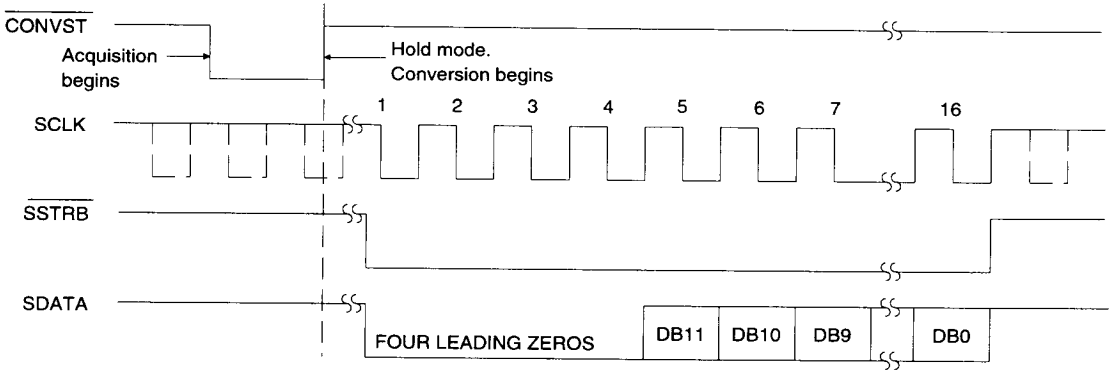


Figure 11c. Mode 1 Timing Diagram - Serial Read

MODE 2 Operation

To operate the device in this mode $\overline{\text{CONVST}}$ must be held permanently low. Bringing $\overline{\text{CS}}$ low (while HBEN is low) puts the device into hold mode and initiates a conversion. The $\overline{\text{BUSY/INT}}$ pin defers to the $\overline{\text{BUSY}}$ function such that $\overline{\text{BUSY}}$ goes low at the start of conversion and returns high at the end of conversion.

The MODE 2 timing diagrams for the parallel data output format are shown in figure 12a . This mode of operation forces the microprocessor to wait for the conversion to be completed before proceeding to other tasks. It removes the risk of inadvertently reading invalid data during a conversion before sufficient time for conversion has elapsed.

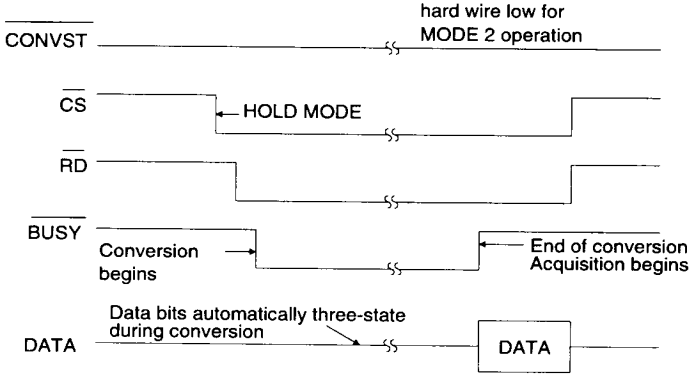


Figure 12a. Mode 2 Timing Diagram, 12-bit Parallel Read

Figure 12b shows the timing diagram for byte operation in MODE 2. Since HBEN must be low to initiate a conversion, the lower byte of data will be accessed first during the two-byte read operation.

The timing diagram for MODE 2 serial operation is shown in figure 12c. The device goes into hold mode on the falling edge of $\overline{CS}$ and conversion begins when $\overline{BUSY}$ goes low. The data is clocked out similarily as for MODE 1 serial operation. Upon clocking of the final data bit $\overline{BUSY}$ goes high indicating end of conversion.

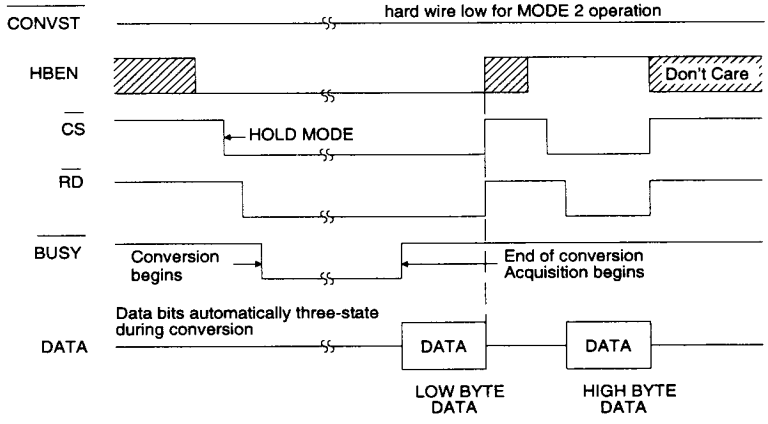


Figure 12b. Mode 2 Timing Diagram, 12-bit Byte Read

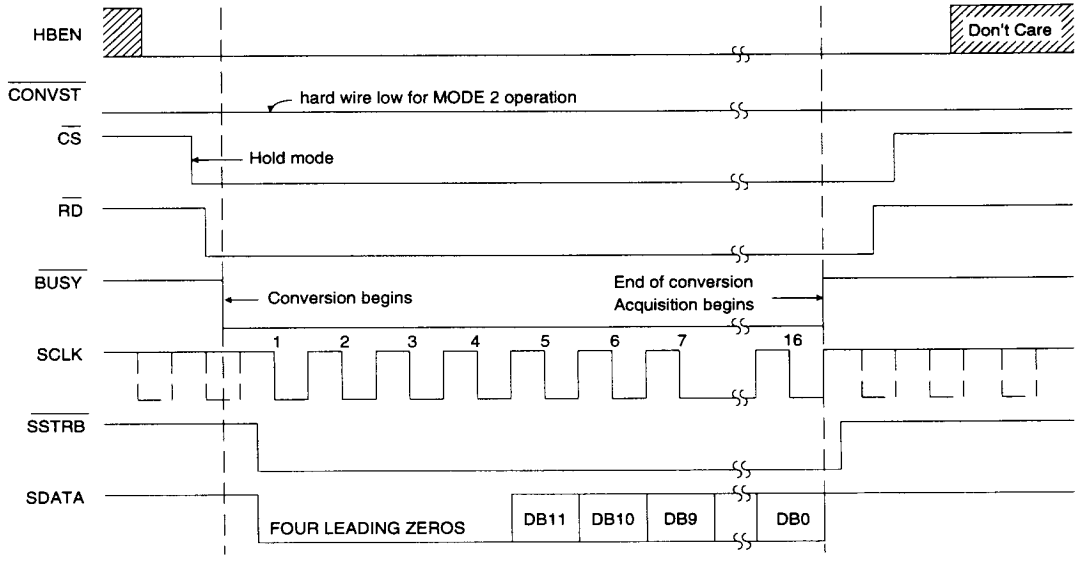


Figure 12c. Mode 2 Timing Diagram, Serial Read

STAND-ALONE OPERATION

The CS5030/5031 support stand-alone conversion when used in MODE 2 parallel interface operation as shown in Figure 13. Conversion is initiated by pulsing $\overline{CS}$ for the duration of the ADC conversion time. The $\overline{BUSY}$ output drives the $\overline{RD}$ input and data is latched on the rising edge of $\overline{BUSY}$ to an external latch.

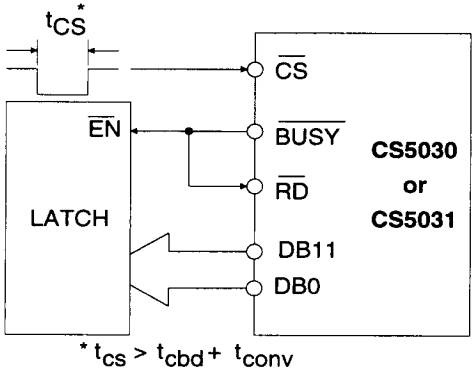
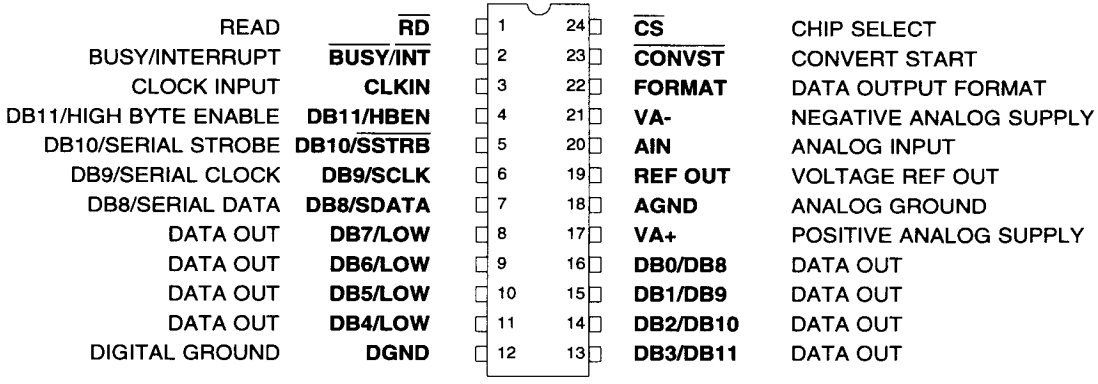


Figure 13. Stand-Alone Operation

PIN DESCRIPTIONS



Pinout applies to both DIP and SOIC packages.

Power Supply Connections

VA+ – Positive Supply, PIN 17.
+5V ±5%.

VA- – Negative Supply, PIN 21.
-5V ±5%.

DGND – Digital Ground, PIN 12.
Ground reference for digital circuitry.

AGND – Analog Ground, PIN 18.
Ground reference for track/hold, reference and DAC.

Oscillator

CLKIN – Clock Input, PIN 3.
An external 10 MHz (CMOS compatible) clock is applied at this pin. Connecting this pin to VA- enables the internal clock oscillator.

Digital Inputs

$\overline{CS}$ – Chip Select, PIN 24.
Active low logic input. The device is selected when this input is active.

$\overline{RD}$ – Read, PIN 1.

Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

FORMAT – Output Mode Selection, PIN 22.

Defines the data format and serial clock format. With FORMAT at +5V, the output data format is 12-bit parallel only. With FORMAT at 0V, either byte or serial data is available and SCLK is not continuous. With FORMAT at -5V, byte or serial data is again available but SCLK is now continuous.

$\overline{CONVST}$ – Convert Start, PIN 23.

A low to high transition on this input puts the track/hold into its hold mode and starts conversion. This input is asynchronous to the CLKIN and independent of $\overline{CS}$ and $\overline{RD}$.

Digital Outputs

$\overline{BUSY}/\overline{INT}$ – Busy/Interrupt, PIN 2.

Active low logic output indicating converter status. See timing diagrams.

DB11/HBEN – Data Bit 11/High Byte Enable, PIN 4.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table 1).

DB10/$\overline{SSTRB}$ – Data Bit 10/Serial Strobe, PIN 5.

When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{SSTRB}$ provides a strobe or framing pulse for serial data.

DB9/SCLK – Data Bit 9/Serial Clock, PIN 6.

When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If FORMAT is at -5V, then SCLK runs continuously. If FORMAT is at 0V, then SCLK is gated off after serial transmission is complete.

DB8/SDATA – Data Bit 8/Serial Data, PIN 7.

When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low.

DB7/LOW, DB6/LOW, DB5/LOW, DB4/LOW – Three-state data outputs, PINS 8, 9, 10, 11.

The outputs of these pins are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the FORMAT and HBEN inputs. With FORMAT high, they are always DB7-DB4. With FORMAT low or -5V, their function is controlled by HBEN (see Table 1).

DB3/DB11, DB2/DB10, DB1/DB9, DB0/DB8 – Three-state data outputs, PINS 13, 14, 15, 16.
The outputs of these pins are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the FORMAT and HBEN inputs. With FORMAT high, they are always DB3-DB0. With FORMAT low or -5V, their function is controlled by HBEN (see Table 1).

Analog Output

REF OUT - Voltage Reference Output, PIN 19.
The internal 2.5V reference is provided at this pin. The external load capability is 500µA.

Analog Input

AIN - Analog Input, PIN 20.
The analog input range for the CS5030 is ± 2.5V, and unipolar 0 to 5V for the CS5031.

Ordering Guide

Model Number	Throughput (kHz)	Input Range (V)	Total Unadjusted Error (LSB)	Temp. Range (°C)	Package
CS5030-BP	400	±2.5	±1	-40 to +85	24-Pin 0.3" PDIP
CS5030-BS	400	±2.5	±1	-40 to +85	24-Pin 0.3" SOIC
CS5030-TD	400	±2.5	±1	-55 to +125	24-Pin 0.3" CERDIP
CS5031-BP	400	+5	±1	-40 to +85	24-Pin 0.3" PDIP
CS5031-BS	400	+5	±1	-40 to +85	24-Pin 0.3" SOIC
CS5031-TD	400	+5	±1	-55 to +125	24-Pin 0.3" CERDIP

PARAMETER DEFINITIONS

Total Unadjusted Error

Total Unadjusted Error includes offset, gain, linearity, and reference errors.

REF OUT Tempco

REF OUT Tempco is the worst case slope that is calculated from the change in reference value at +25° C to the value at T_{MIN} or T_{MAX}
i.e. REF OUT Tempco = (V_{ref} @ 25° C - V_{ref} @ T_{MAX})/(T_{MAX} - 25) or
REF OUT Tempco = (V_{ref} @ 25° C - V_{ref} @ T_{MIN})/(25 - T_{MIN}).

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full-Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset (CS5031)

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in. Units in LSB's.

Bipolar Offset (CS5030)

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND). Units in LSB's.

Bipolar Negative Full-Scale Error (CS5030)

The deviation of the first code transition from the ideal. The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise)

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate(excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Units in percent.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels

Intermodulation Distortion

The ratio of the rms sum of the two test frequencies which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the bandwidth of dc to 200 kHz. Units in percent.

Aperture Time

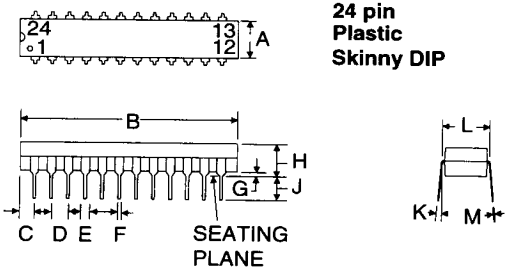
The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Unit in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

PACKAGE DIMENSIONS

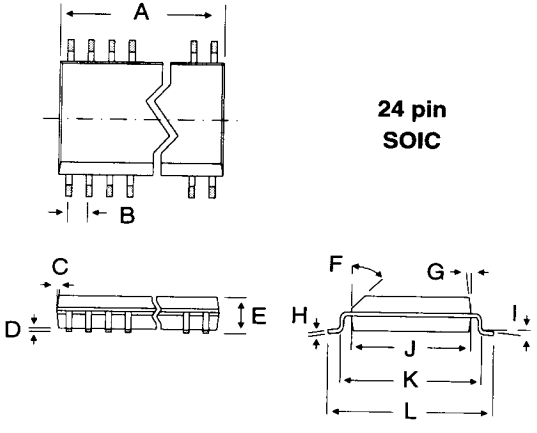


24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

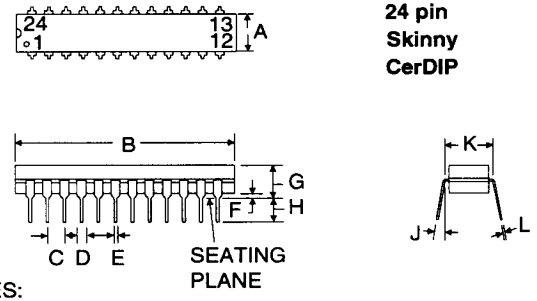
NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.50	0.590	0.610
B	1.27 BSC		0.050 BSC	
C	7° NOM		7° NOM	
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420



24 pin
Skinny
CerDIP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.59	7.87	0.220	0.310
B	-	32.51	-	1.280
C	2.54 BSC		0.100 BSC	
D	0.96	1.65	0.038	0.065
E	0.36	0.58	0.014	0.023
F	0.38	1.52	0.015	0.060
G	-	5.08	-	0.200
H	3.18	5.08	0.125	0.200
J	0°	15°	0°	15°
K	7.37	8.13	0.290	0.320
L	0.20	0.38	0.008	0.015

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.