54AC/74AC818 • 54ACT/74ACT818

8-Bit Diagnostic Register

Description

The 'AC/'ACT818 is a high-speed, general-purpose pipeline register with an on-board diagnostic register for performing serial diagnostics and/or writable control store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

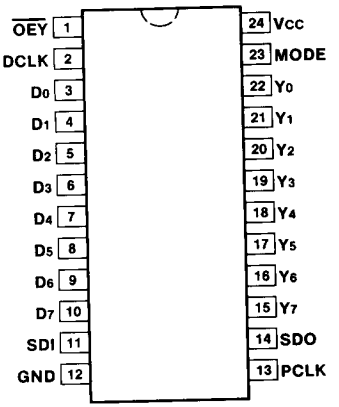
The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the diagnostic register to operate as a right-shift-only register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with 'AC/'ACT818 diagnostic pipeline registers. The loop can be used to scan in a complete test routine starting point (Data, Address, etc.). Then after a specified number of machine cycles it scans out the results to be inspected for the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

- **On-Line and Off-Line System Diagnostics**
- **Swaps the Contents of Diagnostic Register and Output Register**
- **Diagnostic Register and Diagnostic Testing**
- **Cascadable for Wide Control Words as Used in Microprogramming**
- **Edge-Triggered D Registers**
- **Outputs Source/Sink 24 mA**
- **'ACT818 has TTL-Compatible Inputs**
- **'ACT818 is Functionally- and Pin-Compatible to AMD 29818 and MMI 74S818**

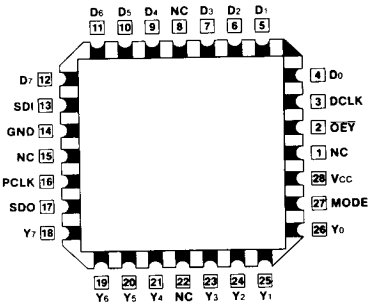
Applications

- **Register for Microprogram Control Store**
- **Status Register**
- **Data Register**
- **Instruction Register**
- **Interrupt Mask Register**
- **Pipeline Register**
- **General Purpose Register**
- **Parallel-Serial/Serial-Parallel Converter**

Connection Diagrams

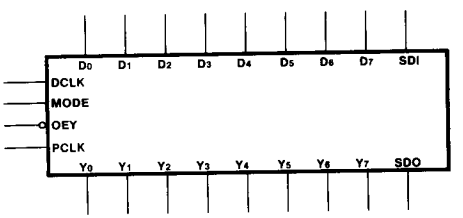


Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC and PCC

Logic Symbol

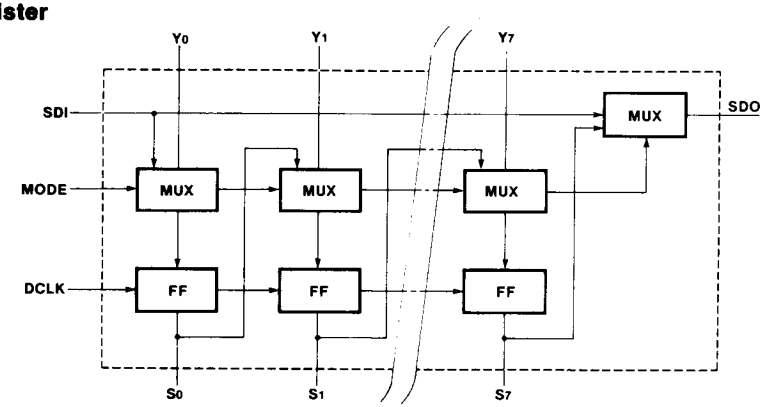


Pin Names

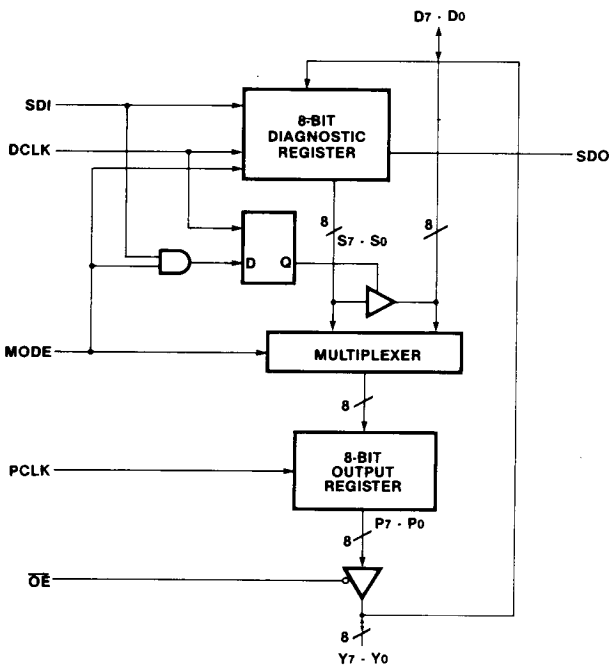
D_0 - D_7	Data Inputs
SDI	Serial Data Input
DCLK	Diagnostics Clock
MODE	Control Input
PCLK	Pipeline Register Clock
$\overline{OEY}$	Output Enable Input
SDO	Serial Data Output
Y_0 - Y_7	Data Outputs

Ordering Code: See Section 6

Diagnostic Register



Block Diagram



Functional Description

Data transfers into the diagnostic register occur on the LOW-to-HIGH transition of DCLK. Mode and SDI determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. Mode selects whether the data source is the data input or the diagnostic register output. Because of the independence of the clock inputs, data can be shifted in the diagnostic register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously, as long as no setup or hold times are violated. This simultaneous operation is legal.

Function Table

Inputs				Outputs			Operation
SDI	MODE	DCLK	PCLK	SDO	Diagnostic Reg.	Pipeline Reg.	
X	L	⌐	X	S7	SI<SI-1, SO<SDI	NA	Serial Shift; D_7 - D_0 disabled
X	L	X	⌐	S7	NA	PI<DI	Normal Load Pipeline Register
L	H	⌐	X	L	SI<YI	NA	Load Diagnostic Register from Y; DI disabled
X	H	X	⌐	SDI	NA	PI<SI	Load Pipeline Register from Diagnostic Register
H	H	⌐	X	H	Hold	NA	Hold Diagnostic Register; DI enabled

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT		54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit				
I_{IN}	Maximum Input Current		±0.1	±10.0	±1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		±0.5	±10.0	±5.0	μA	$\overline{OE}$ = V_{IH}, V_{CC} = Max V_{OUT} = 0, V_{CC}
I_{CC}	Maximum Quiescent Supply Current		1.0			mA	V_{CC} = Max
I_{CCT}	Maximum Additional Icc/Input ('ACT818)			1.6	1.5	mA	V_{IN} = V_{CC}-2.1 V V_{CC} = 5.5 V
V_{OH}	Minimum LOW Level Output Y_0 - Y_7 Outputs		3.86	3.70	3.76	V	I_{OH} = -24 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = -24 mA, V_{CC} = 5.5 V
	Minimum HIGH Level Output D_0 - D_7, SDO Outputs		3.86	3.70	3.76	V	I_{OH} = -8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = -8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum LOW Level Output Y_0 - Y_7 Outputs		0.32	0.40	0.37	V	I_{OL} = 24 mA, V_{CC} = 4.5 V
			0.32	0.40	0.37	V	I_{OL} = 24 mA, V_{CC} = 5.5 V
	Maximum HIGH Level Output D_0 - D_7, SDO Outputs		0.32	0.40	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.40	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current, Y_0 - Y_7 Outputs			57	86	mA	V_{CC} = 5.5 V V_{OLD} = 1.1 V
I_{OHD}	Minimum Dynamic Output Current, Y_0 - Y_7 Outputs			-50	-75	mA	V_{CC} = 5.5 V V_{OHD} = 3.85 V
I_{OLD}	Minimum Dynamic Output Current, D_0 - D_7, SDO Outputs. See Note.			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current, D_0 - D_7, SDO Outputs. See Note.			-32	-32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note: Test Load 50 pF, 500 ohm to Ground

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay PCLK to Y	3.3 5.0		6.5 4.5						ns	3-6
t_{PLH}	Propagation Delay PCLK to Y	3.3 5.0		6.5 5.0						ns	3-6
t_{PHL}	Propagation Delay MODE to SDO	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay MODE to SDO	3.3 5.0		10.0 7.5						ns	3-6
t_{PHL}	Propagation Delay SDI to SDO	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay SDI to SDO	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay DCLK to SDO	3.3 5.0		12.0 9.5						ns	3-6
t_{PLH}	Propagation Delay DCLK to SDO	3.3 5.0		12.5 9.0						ns	3-6
t_{PZL}	Output Enable Time $\overline{OEY}$ to Y(x)	3.3 5.0		6.0 4.0						ns	3-8
t_{PLZ}	Output Disable Time $\overline{OEY}$ to Y(x)	3.3 5.0		6.0 4.5						ns	3-8
t_{PZL}	Output Enable Time DCLK to D(x)	3.3 5.0		11.0 8.0						ns	3-8
t_{PLZ}	Output Disable Time DCLK to D(x)	3.3 5.0		8.5 6.5						ns	3-8
t_{PZH}	Output Enable Time $\overline{OEY}$ to Y(x)	3.3 5.0		7.0 5.0						ns	3-7
t_{PHZ}	Output Disable Time $\overline{OEY}$ to Y(x)	3.3 5.0		9.0 6.5						ns	3-7
t_{PZH}	Output Enable Time DCLK to D(x)	3.3 5.0		9.0 6.5						ns	3-7
t_{PHZ}	Output Disable Time DCLK to D(x)	3.3 5.0		9.0 6.5						ns	3-7

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time D to PCLK	3.3 5.0	5.0 3.5				ns	3-9
t_h	Hold Time D to PCLK	3.3 5.0	-1.5 -1.0				ns	3-9
t_s	Setup Time MODE to PCLK	3.3 5.0	5.5 4.0				ns	3-9
t_h	Hold Time MODE to PCLK	3.3 5.0	-1.5 -1.0				ns	3-9
t_s	Setup Time Y TO DCLK	3.3 5.0	1.5 1.0				ns	3-9
t_h	Holt time Y TO DCLK	3.3 5.0	0 0				ns	3-9
t_s	Setup Time MODE to DCLK	3.3 5.0	4.0 3.0				ns	3-9
t_h	Hold Time MODE to DCLK	3.3 5.0	-0.5 -0.5				ns	3-9
t_s	Setup Time SDI to DCLK	3.3 5.0	4.0 3.0				ns	3-9
t_h	Hold Time SDI to DCLK	3.3 5.0	-0.5 -0.5				ns	3-9
t_s	Setup Time DCLK to PCLK	3.3 5.0	9.5 7.0				ns	3-9
t_s	Setup Time PCLK to DCLK	3.3 5.0	11.0 8.0				ns	3-9
t_w	Pulse Width PCLK HIGH or LOW	3.3 5.0	5.5 4.0				ns	3-6
t_w	Pulse Width DCLK HIGH or LOW	3.3 5.0	11.0 8.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay PCLK to Y	5.0		6.5						ns	3-6
t_{PLH}	Propagation Delay PCLK to Y	5.0		6.5						ns	3-6
t_{PHL}	Propagation Delay MODE to SDO	5.0		8.5						ns	3-6
t_{PLH}	Propagation Delay MODE to SDO	5.0		9.5						ns	3-6
t_{PHL}	Propagation Delay SDI to SDO	5.0		8.0						ns	3-6
t_{PLH}	Propagation Delay SDI to SDO	5.0		8.0						ns	3-6
t_{PHL}	Propagation Delay DCLK to SDO	5.0		11.0						ns	3-6
t_{PLH}	Propagation Delay DCLK to SDO	5.0		11.0						ns	3-6
t_{PZL}	Output Enable Time $\overline{OEY}$ to Y(x)	5.0		6.5						ns	3-8
t_{PLZ}	Output Disable Time $\overline{OEY}$ to Y(x)	5.0		6.5						ns	3-8
t_{PZL}	Output Enable Time DCLK to D(x)	5.0		9.5						ns	3-8
t_{PLZ}	Output Disable Time DCLK to D(x)	5.0		9.0						ns	3-8
t_{PZH}	Output Enable Time $\overline{OEY}$ to Y(x)	5.0		7.5						ns	3-7
t_{PHZ}	Output Disable Time $\overline{OEY}$ to Y(x)	5.0		9.0						ns	3-7
t_{PZH}	Output Enable Time DCLK to D(x)	5.0		8.5						ns	3-7
t_{PHZ}	Output Disable Time DCLK to D(x)	5.0		9.5						ns	3-7

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time D to PCLK	5.0	3.0				ns	3-9
t_h	Hold Time D to PCLK	5.0	-1.0				ns	3-9
t_s	Setup Time MODE to PCLK	5.0	4.0				ns	3-9
t_h	Hold Time MODE to PCLK	5.0	-1.0				ns	3-9
t_s	Setup Time Y TO DCLK	5.0	1.0				ns	3-9
t_h	Hold time Y TO DCLK	5.0	0				ns	3-9
t_s	Setup Time MODE to DCLK	5.0	5.0				ns	3-9
t_h	Hold Time MODE to DCLK	5.0	-0.5				ns	3-9
t_s	Setup Time SDI to DCLK	5.0	4.0				ns	3-9
t_h	Hold Time SDI to DCLK	5.0	0				ns	3-9
t_s	Setup Time DCLK to PCLK	5.0	8.0				ns	3-9
t_s	Setup Time PCLK to DCLK	5.0	8.0				ns	3-9
t_w	Pulse Width PCLK HIGH or LOW	5.0	4.0				ns	3-6
t_w	Pulse Width DCLK HIGH or LOW	5.0	10.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V