VITESSE
SEMICONDUCTOR CORPORATION

Data Sheet
VSC830

2.7Gb/s Asynchronous
Dual 2x2 Crosspoint Switch

Features

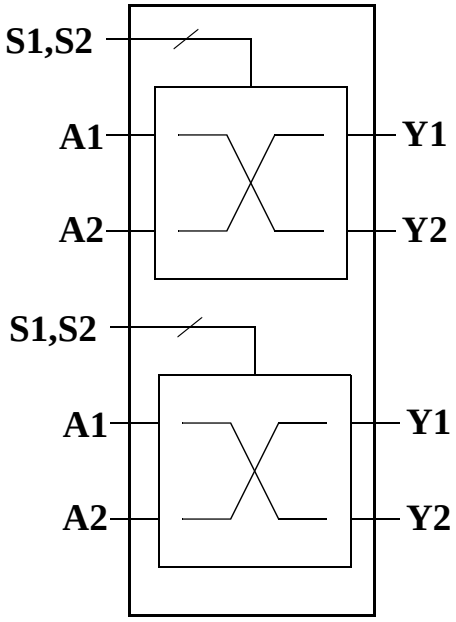
- Dual 2x2 Crosspoint Switch
- 2.7Gb/s NRZ Data Bandwidth, 2.7GHz Signal Bandwidth
- PECL/TTL-Compatible Control Inputs
- PECL-Compatible High-Speed I/O
- 50Ω Source Terminated Output Driver and Programmable Input Terminations
- Single 3.3V Supply, 1W Typical Dissipation
- Power-Down Capability for Unused Outputs
- Compact 44-Pin PQFP, 10x10mm Package

General Description

The VSC830 is a monolithic dual 2x2 asynchronous crosspoint switch, designed for critical signal path control and buffering applications, such as loop-back, protection switching, and multi-channel backplane driver/receivers. Signal path delay is tightly matched between each output channel to eliminate the need for delay path compensation when switching between signal sources.

The crosspoint function is based on a multiplexer tree architecture. Each 2x2 switch can be considered as a pair of 2:1 multiplexers that share the same inputs. The signal path through each switch is fully differential and delay matched. The signal path is unregistered, so there are no restrictions on the phase, frequency, or signal pattern at each input. Unused outputs can be independently powered off, thereby eliminating power on unused sections (see *Design Guide* section in this data sheet). The switch control inputs can be configured to be compatible with PECL or TTL levels. The high-speed input and output levels are nominally PECL compatible and capable of interfacing with a wide range of termination schemes.

VSC830 Symbol Diagram



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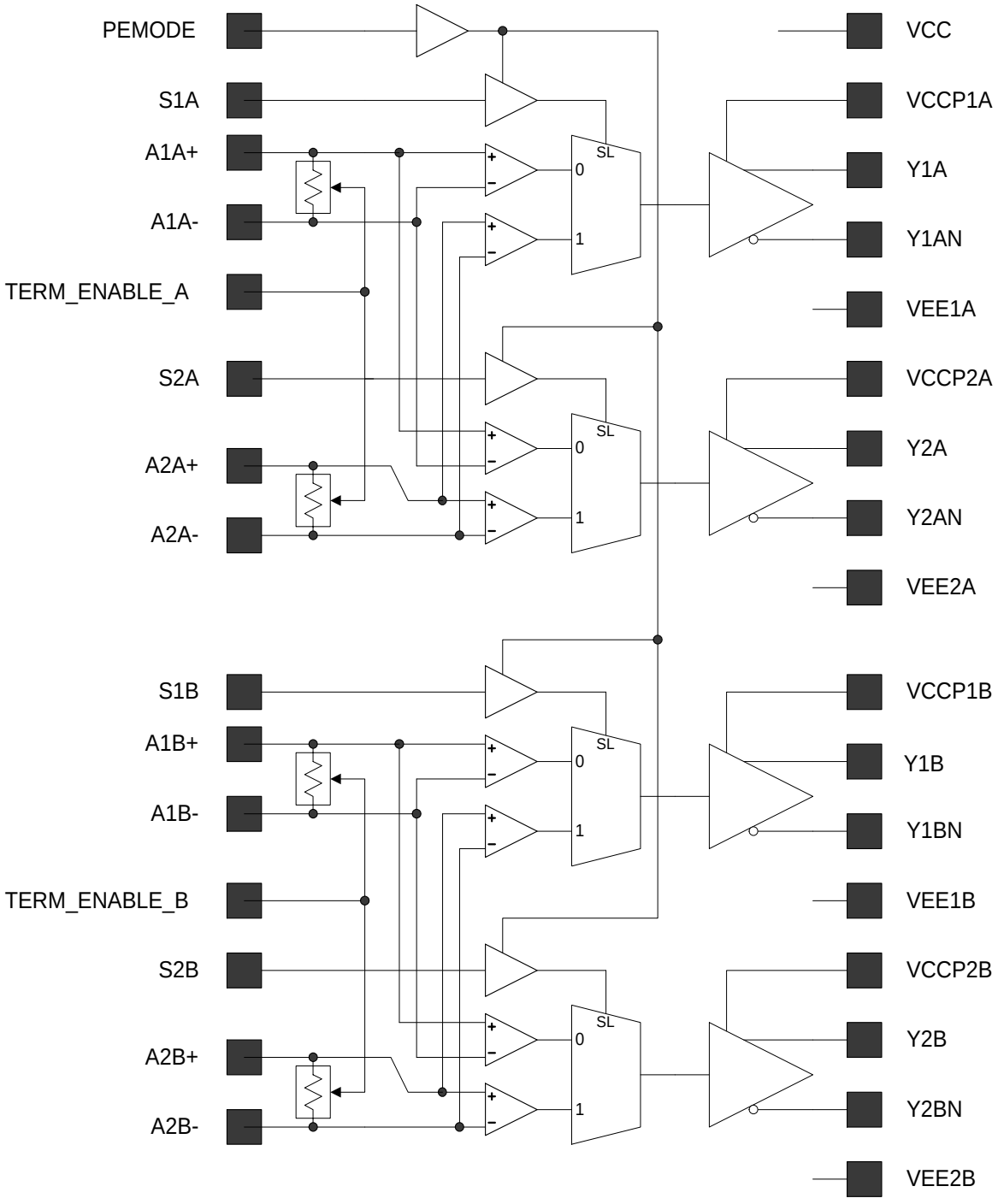
Functional Block Diagram



Functional Description

Select

As shown in Figure 1, each output can be treated as a 2:1 multiplexer, with the A1 and A2 inputs common to both multiplexers. The select input S1 independently controls the state of the multiplexer that drives output Y1, and select input S2 independently controls the output of Y2.

Figure 1: Select Functional Block Diagram

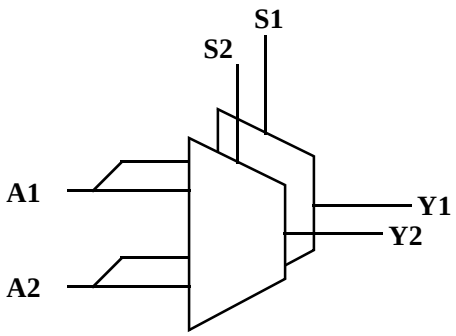


Table 1 specifies the function of the select inputs.

Table 1: Select Function

S1	*S2*	*Y1*	*Y2*
0	0	A1	A1
1	0	A2	A1
0	1	A1	A2
1	1	A2	A2

MODE

The interface level of the select pins, S1 and S2, can be programmed to either TTL or PECL levels by shorting the MODE pin to either V_{CC} or V_{EE}. Note that the MODE pin must be tied to either V_{CC} or V_{EE}. The function of MODE is specified in Table 2.

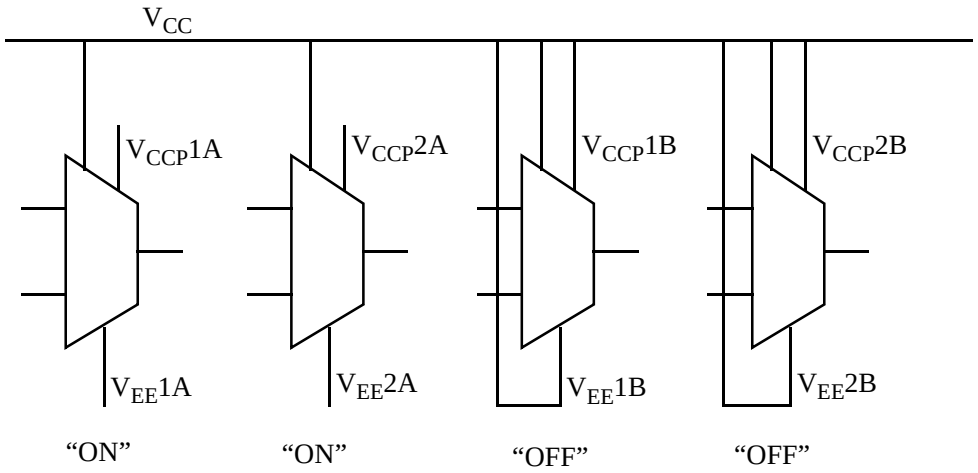
Table 2: MODE Function

MODE	*S1, S2*
V_{EE}	TTL
V_{CC}	PECL

Power-Down

Power to each output stage is provided through V_{CC}, V_{CCP}, and V_{EE}. V_{CC} is common to all outputs. To power off unused outputs, tie the respective V_{EE} and V_{CCP} pin to V_{CC}, as shown in Figure 2.

Figure 2: Power-Down Mode Example



Minimum power configuration requires output channel 1A active, so power must be applied to V_{CCP}1A and V_{EE}1A at all times.

Programmable input termination

Across each differential input (from the + input to the - input) of the VSC830 is a switched 100Ω termination resistor. Using the TERM_ENABLE pin, the termination can be optionally disabled. To enable the input termination, connect the respective TERM_ENABLE pin to V_{CC}. To disable the internal termination, connect TERM_ENABLE to V_{EE}. If unconnected, the TERM_ENABLE pin will self-bias to V_{EE} and disable the internal termination. Independent termination controls are provided for the "A" and "B" switches.

AC Characteristics

Table 3: AC Timing

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*
F_{RATE}	Signal path data rate			2.7	Gb/s
F_{BW}	Signal path bandwidth (-3dB)			2.7	GHz
T_{SKW}	Channel to channel delay skew		50		ps
T_{CON}	Switch configuration setup time(1)			1	ns
t_R, t_F	High-speed output rise/fall times, 20% to 80%(2)			150	ps
t_{jP}	Signal path added jitter, peak-peak(1)			40	ps

NOTES: (1) Tested on a sample basis only, with 2^{23}-1 PRBS data, input signal rise/fall time < 150ps. Value stated in table is added to measurement system jitter. (2) Input signal rise/fall time < 150ps, measured using an alternating 1, 0 pattern.

DC Characteristics (*All characteristics are over the specified operating conditions)*

Table 4: Power Supply

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{CC}	Total $V_{CC(P)}$ supply current			350	mA	
P_D	Power dissipation per output (Y1A±, Y2A±, Y1B±, Y2B±)			300	mW	
P_T	Total chip power (all outputs powered on)			1.2	W	

NOTE: Specified with outputs terminated, 100Ω between true and complement, V_{CC} = 3.45V.

Table 5: Select Input Levels—TTL Mode

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage (TTL)	2.0			V	
V_{IL}	Input LOW voltage (TTL)			0.8	V	
I_{IH}	Input HIGH current (TTL)			500	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current (TTL)			-500	µA	V_{IN} = 0.5V

Table 6: Select Input Levels—PECL Mode

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage (PECL)	V_{CC}-1.0			V	
V_{IL}	Input LOW voltage (PECL)			V_{CC}-1.6	V	
I_{IH}	Input HIGH current (PECL)			500	µA	V_{IN} = 2.5V
I_{IL}	Input LOW current (PECL)			-500	µA	V_{IN} = 1.5V

Table 7: Control Inputs

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
R_{PEMODE}	PEMODE pin impedance		3100		Ω	

Table 8: "A" Input Levels (Differential PECL)

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{ID}	Input differential voltage	200		1000	mV	See Note 1
V_{ICM}	Input common-mode voltage	V_{CC}-1.7		V_{CC}-0.9	V	

NOTE: (1) Peak-to-peak swing of each side of the differential input.

Table 9: "Y" Output Levels (Differential PECL)

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OD1}	Output differential voltage (Data)	400	700	1000	mV	See Note 1
V_{OD2}	Output differential voltage (Clock)	400	550	850	mV	See Note 2
V_{OCM}	Output common-mode voltage	V_{CC}-1.6		V_{CC}-1.0	V	

NOTES: (1) Peak-peak swing of each side of the differential output. 2^{23}-1 PRBS data. (2) Peak-to-peak swing of each side of the differential output. Alternating 1, 0 pattern.

Absolute Maximum Ratings

Power Supply Voltage (V_{CC}) Potential to GND .....-0.5V to +4.0V
TTL Input Voltage Applied ..... -0.5V to V_{CC} +0.5V
ECL Input Voltage Applied .....-0.5V to V_{CC} +0.5V
Output Current (I_{OUT}) 50mA
Case Temperature Under Bias (T_C) .....-55°C to + 125°C
Storage Temperature (T_{STG}).....-65°C to + 150°C

NOTE: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Operating Conditions

Supply voltage (V_{EE}) 0V
Supply voltage (V_{CC})..... +3.3V ±5%
Supply voltage (V_{CCP}) ..... +3.3V ±5%
Operating Range(1) (T) ..... 0°C to +85°C

NOTE: (1) Lower limit of specification is ambient temperature and upper limit is case temperature.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC830 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

Package Pin Descriptions

Figure 3: Pin Diagram

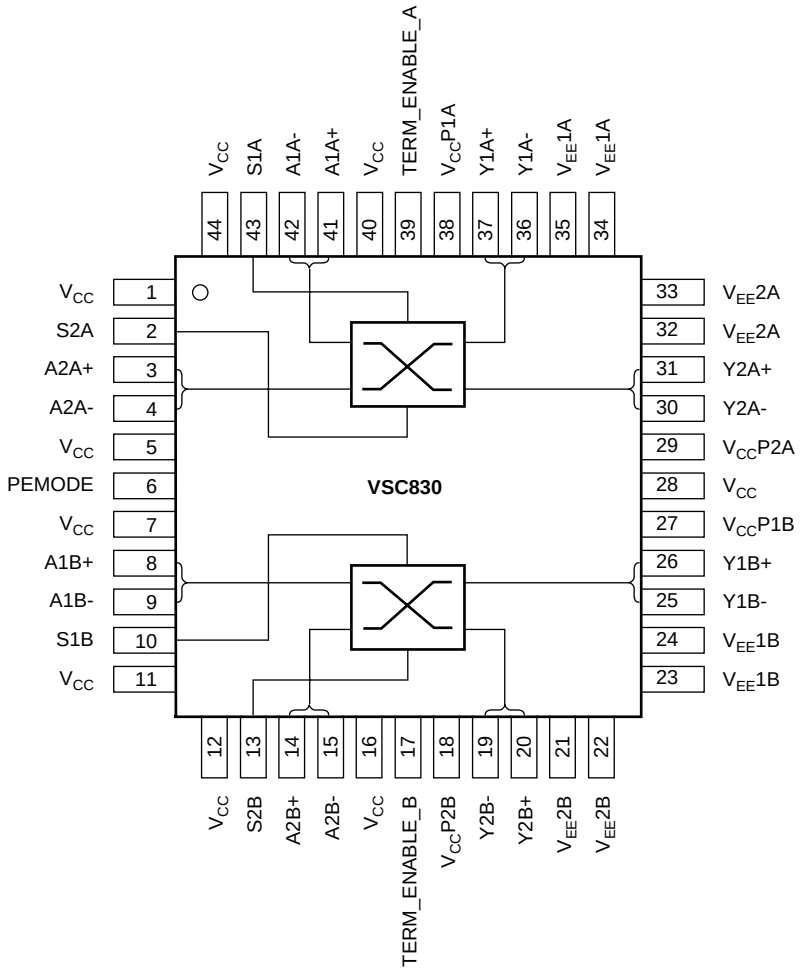


Table 10: Pin Identification

Signal Name	*Pin(s)*	*Function*	*Description*
V_{CC}	1, 5, 7, 11, 12, 16, 28, 40, 44	Positive Supply	Global supply for chip
V_{EE}1A	34, 35	Negative Supply	For channel output 1A. Must always be powered on.
V_{EE}2A	32, 33	Negative Supply	For output 2A. Connect to VCC to power-off.
V_{EE}1B	23, 24	Negative Supply	For output 1B. Connect to VCC to power-off.
V_{EE}2B	21, 22	Negative Supply	For output 2B. Connect to VCC to power-off.
V_{CC}P1A	38	Positive Supply	Output driver supply for channel 1A
V_{CC}P2A	29	Positive Supply	Output driver supply for channel 2A
V_{CC}P1B	27	Positive Supply	Output driver supply for channel 1B
V_{CC}P2B	18	Positive Supply	Output driver supply for channel 2B
TERM_ENABLE_A	39	Termination Enable	Input termination enable for the “A” switch. Normally low (VEE). Connect to VCC to enable internal 100 ohm termination between AxA± inputs.
TERM_ENABLE_B	17	Termination Enable	Input termination enable for the “B” switch. Normally low (VEE). Connect to VCC to enable internal 100Ω termination between AxA± inputs.
PEMODE	6	Control	PECL/TTL interface control
A1A±	41, 42	PECL Input	Channel 1A differential signal input
S1A	43	PECL/TTL Input	Channel 1A input selector
Y1A±	37, 36	PECL Output	Channel 1A differential output
A2A±	3, 4	PECL Input	Channel 2A differential signal input
S2A	2	PECL/TTL Input	Channel 2A input selector
Y2A±	31, 30	PECL Output	Channel 2A differential output
A1B±	8, 9	PECL Input	Channel 1B differential signal input
S1B	10	PECL/TTL Input	Channel 1B input selector
Y1B±	26, 25	PECL Output	Channel 1B differential output
A2B±	14, 15	PECL Input	Channel 2B differential signal input
S2B	13	PECL/TTL Input	Channel 2B input selector
Y2B±	20, 19	PECL Output	Channel 2B differential output

Package Thermal Characteristics

The VSC830 is packaged into a standard plastic quad flatpack with an embedded, but unexposed thermal slug. This package adheres to industry-standard EIAJ footprints for a 10x10mm body, 44 lead PQFP. The package construction is as shown in Figure 4. The 44-pin PQFP with embedded slug has the thermal properties shown in Table 11. This package allows the VSC830 to operate with ambient temperatures up to 70^{o}C in still air.

Figure 4: Package Cross Reference

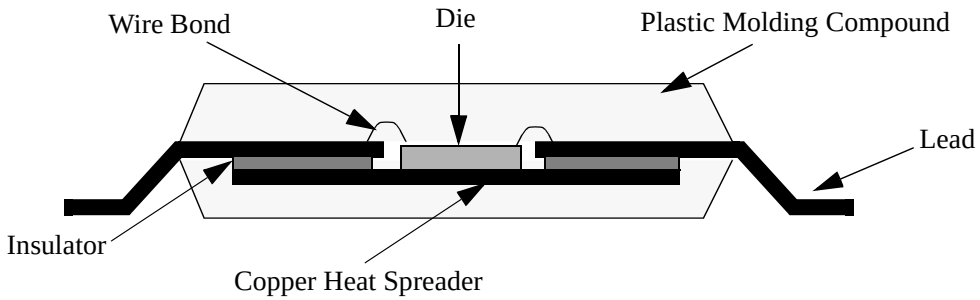


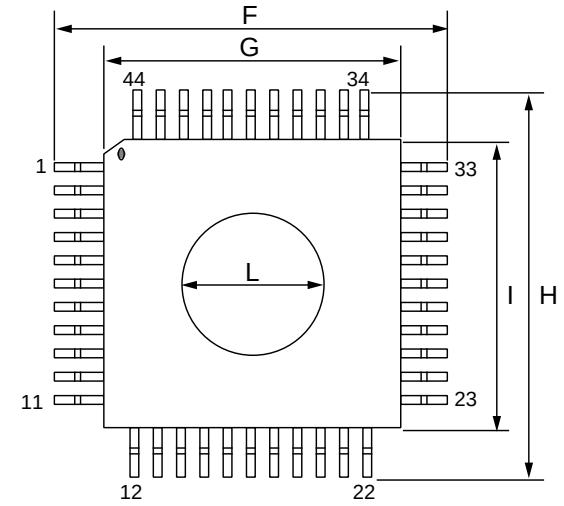
Table 11: 44-Pin PQFP Thermal Resistance

Symbol	*Description*	*Value (^{o}C/W)*	*$T_{A(MAX)}$ (^{o}C)*
θ_{CA-0}	Thermal resistance from case-to-ambient, still air	28.4	50.9
θ_{CA-100}	Thermal resistance from case-to-ambient, 100 LFPM air	22.7	57.8
θ_{CA-200}	Thermal resistance from case-to-ambient, 200 LFPM air	19.9	61.1
θ_{CA-400}	Thermal resistance from case-to-ambient, 400 LFPM air	16.2	65.6
θ_{CA-600}	Thermal resistance from case-to-ambient, 600 LFPM air	13.9	68.3

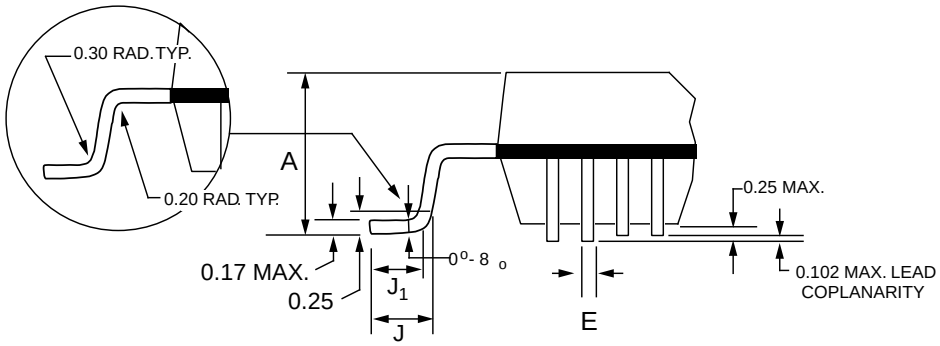
NOTE: $T_{A(MAX)}$ = max case temperature - (max power dissipation • $\theta_{CA\ AIRFLOW}$).

Package Information

44-Pin PQFP, 10mm x 10mm Package Drawing



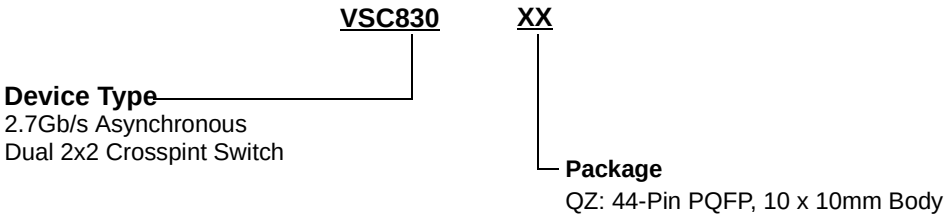
Item	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+.10 / -.05
E	0.35	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
J1	0.80	+.15 / -.10
K	0.80	BASIC
L	3.56	±.50 DIA.



NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.
Package #: 101-299-1
Issue #: 1

Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



Evaluation Boards

An evaluation board for the VSC830 is available. Please contact your local sales representative.

Design Guide

Introduction

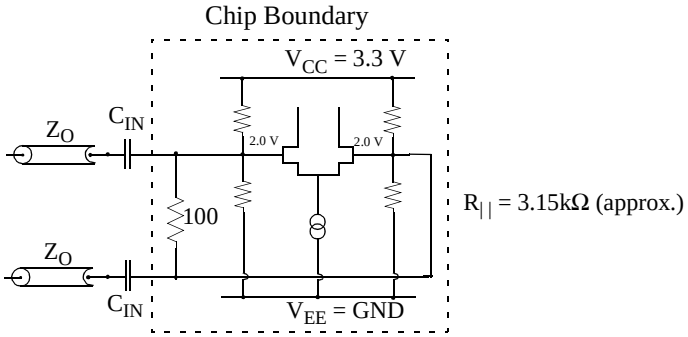
The purpose of this document is to make it easier for system designers to use the VSC830 2.7Gb/s dual 2x2 crosspoint switch. This guide provides guidelines for I/O terminations, power supply decoupling and board lay-out.

Signal Terminations

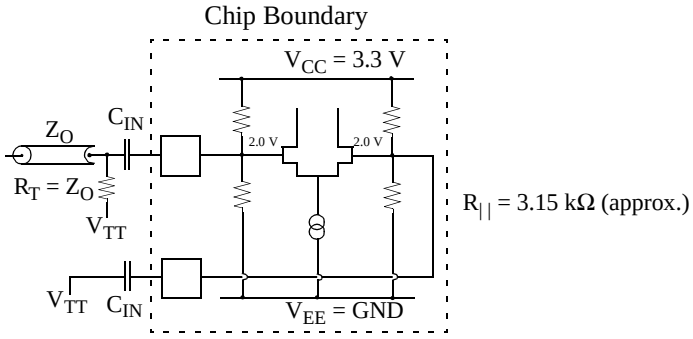
The high-speed inputs (A1A+/-, A1B+/-, A2A+/- and A2B+/-) on the VSC830 are internally terminated with a programmable 100Ω termination between the true and complement input. The input termination can be disabled by connecting the TERM_ENABLE pin to VEE. High impedance internal biasing resistors provide the correct bias voltage at the inputs for AC-coupled applications (Figure 5).

Figure 5: High-Speed Input Termination

a) Termination Enabled



b) Termination Disabled

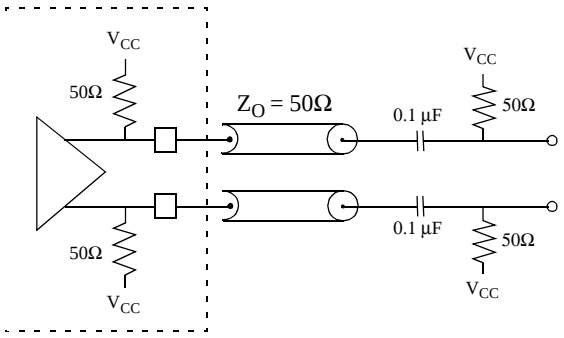


C_{IN} TYP = 0.1µF (capacitor value is selected for data input = 2.7Gb/s)
$V_{TT} = V_{CC}$ - 1.3V

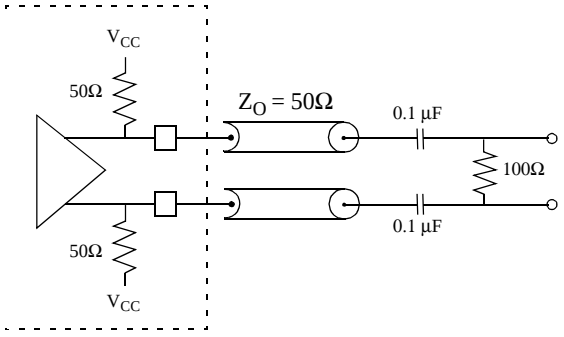
The high-speed outputs (Y1A+/-, Y1B+/-, Y2A+/- and Y2B+/-) each consist of a differential pair designed to drive a 50Ω transmission line. The transmission line should be terminated with a 100Ω resistor at the receiver of the downstream device between the true and complement outputs. No connection to a termination voltage is required. The output driver is source terminated to 50Ω on-chip, providing a snubbing of any reflections. Output power can be cut by tying V_{EE} to V_{CC}. In single ended mode, the unused output must be terminated with 50Ω. Some output termination examples are shown in Figures 6 and 7.

Figure 6: Examples of High-Speed Output I/O Termination for VSC830

a) AC Termination #1



b) AC Termination #2 (Internal biasing required for Receiver)



c) AC Termination #3

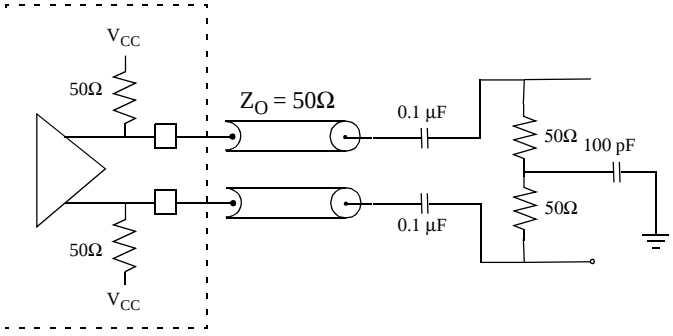
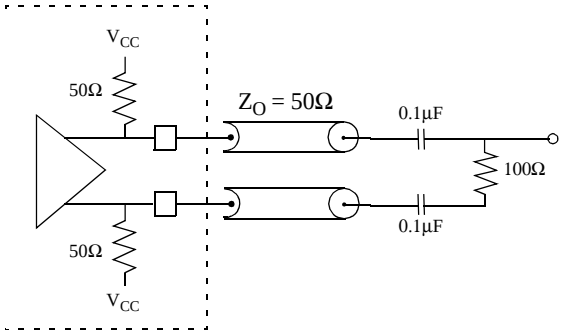
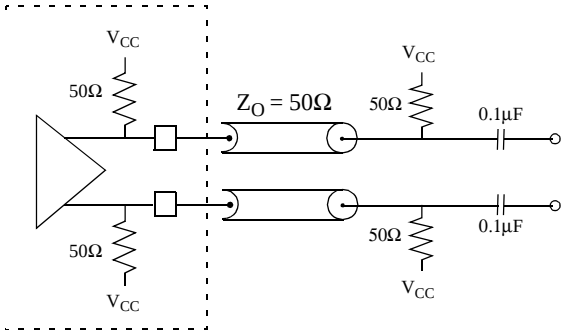


Figure 7: Examples of High-Speed Output I/O Termination for VSC830

a) Single-Ended AC Termination (Receiver internal biasing required)



b) DC Termination

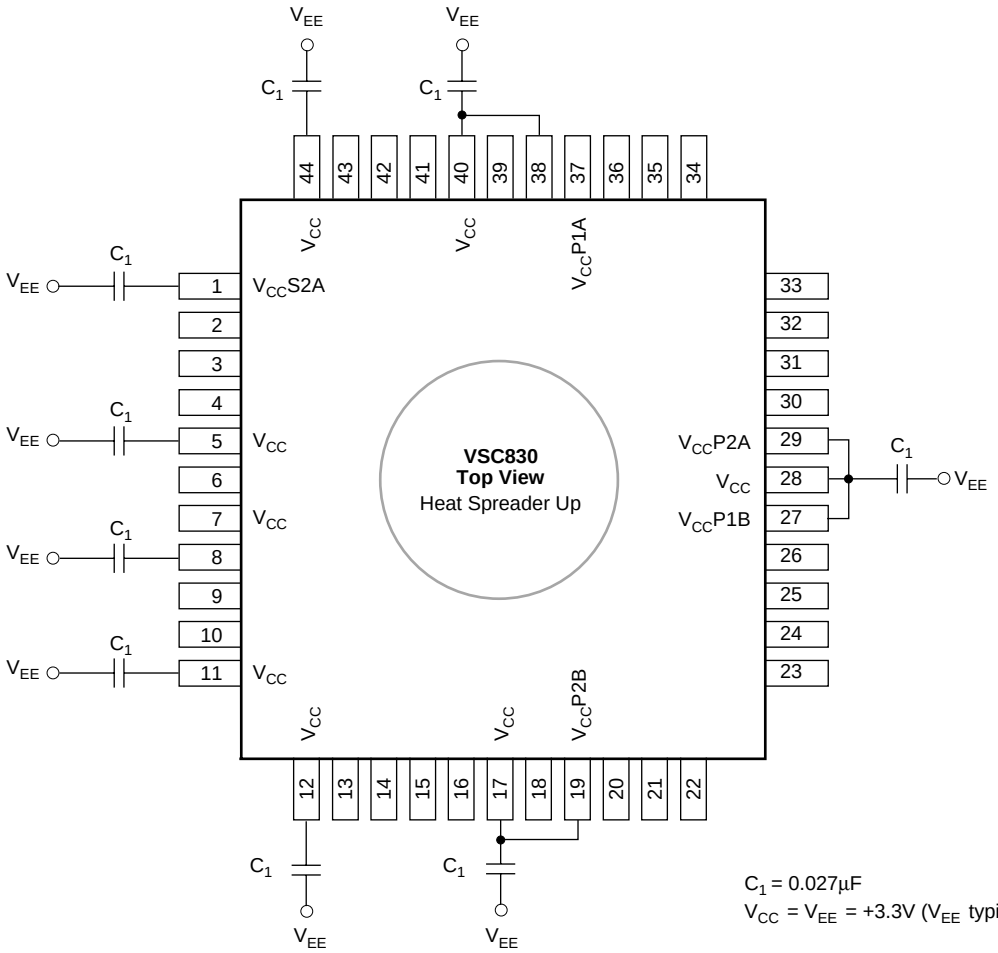


Power Supply and Layout Considerations

The VSC830 is a single supply part, requiring only a 3.3V supply. The location and hook-up of the bypass capacitors is critical to providing the VSC830 with a clean 3.3V power supply. V_{CC} that are adjacent can share a 0.027µF capacitor connected to V_{EE}.

Normally the four channel specific V_{CC} pins (V_{CC}P1A, V_{CC}P1B, V_{CC}P2A, V_{CC}P2B) are connected to one common V_{CC} plane. In the same way the four channel specific V_{EE} pins are connected to the common V_{EE} plane. A suggested decoupling schematic for this configuration is shown in Figure 7a. However, a slightly higher signal integrity can be achieved if these pins are treated as different power supplies. In this case, V_{CC}P1A should then be decoupled to V_{EE}1A etc, as shown in Figure 7b.

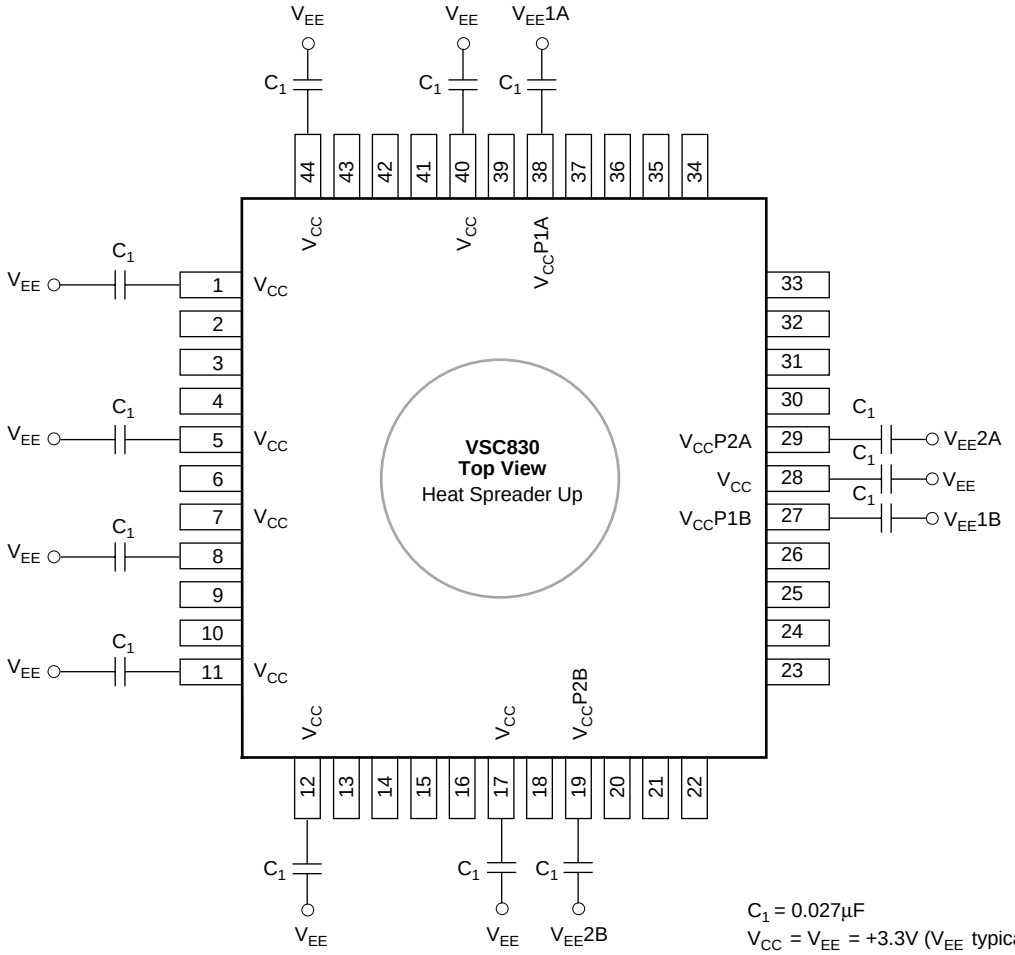
Figure 8: Decoupling Example: Common V_{CC} and V_{EE} Planes



C_1 = 0.027µF
V_{CC} = V_{EE} = +3.3V (V_{EE} typically ground)

Recommended resistor and capacitor is size 805

Figure 9: Decoupling Example: Separate V_{CC} and V_{EE} Planes



C_1 = 0.027µF
V_{CC} = V_{EE} = +3.3V (V_{EE} typically ground)

Recommended resistor and capacitor is size 805

High-Speed Serial I/O Layout Considerations

The high-speed serial signals contain digital data at fundamental frequencies up to 2.488GHz clock rate. Given that, in order to preserve the edges of such data sequences, it is necessary to have excellent frequency and phase response up to at least the 3rd harmonic, if not the 7th harmonic. Improved signal quality will result should the reader follow the general design rules below:

1. Keep traces as short as possible. Initial component placement should be very carefully considered.
2. The impedance of the traces must match that of the terminations, connectors and cable(s) in order to reduce reflections and impedance mismatches. Reflections can create standing waves that will increase the signal jitter.
3. Differential transmission line impedance must be maintained at 100Ω.
4. When routing differential pairs, keep the lengths identical for both traces. Differences in trace length translate directly into signal skew and can add to the signal jitter. Remember also that the differential impedance is affected by the separation between the traces.
5. Keep differential pair traces on the same side of the PCB to minimize impedance discontinuity, such as the one caused when using printed-circuit board vias.
6. Eliminate or reduce stubs.
7. Use rounded corners rather than 45° or 90° corners.
8. Keep signal traces far from other signals which might capacitively couple noise into the signals. This includes the other trace of a differential pair or the traces of the parallel PECL or TTL interface.
9. Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less.