SIEMENS

Audio Ringing Codec Filter Featuring Speakerphone Function (ARCOFI®-SP)

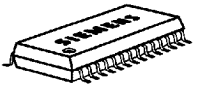
PSB 2163

Preliminary Data

BICMOS-IC

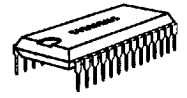
1 Features

- Applications in digital terminal equipment featuring voice functions
- Digital signal processing performs all CODEC functions
- Fully compatible to the G. 714 CCITT and ETSI (NET33) specification
- PCM A-Law/μ-Law (G. 711 CCITT) and 16-bit linear data
- Flexible configuration of all internal functions
- IOM-2 interface (TE- and non-TE-mode), Serial Control Interface (SCI) and Serial Data Interface (SDI)
- Three analog inputs for the microphone in the handset, the speakerphone and the headset
- Two differential outputs for a handset earpiece (200 Ω) and a loudspeaker (50 Ω)
- 100-mW sine wave and 200-mW square wave loudspeaker driver capability
- Separate digital output for a piezo ringer
- Flexible Peripheral Control Interface (PCI) in IOM-2 TE-mode
- Flexible test and maintenance loopbacks in the analog front end and the digital signal processor
- Independent gain programmable amplifiers for all analog inputs and outputs
- Full digital speakerphone and monitoring support without any external components (speakerphone test and optimization function is available)
- Two transducer correction filters
- Side tone gain adjustment
- Flexible DTMF, tone and ringing generator
- Single 5-V power supply
- Low power consumption: standby 1 mW, operating consumption is dependent on the selected operating mode
- Advanced 1-μ BICMOS technology



P-DSO-28

P-LCC-28-R

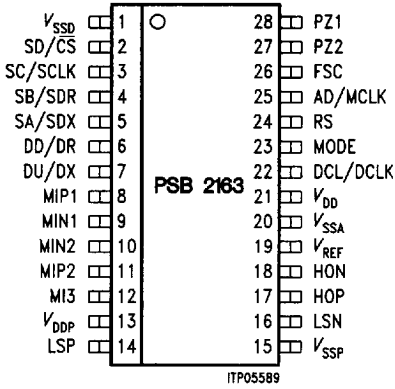


P-DIP-28

Type	Ordering Code	Package
PSB 2163	Q67100-H6458	P-DSO-28 (SMD)
PSB 2163	Q67100-H6348	P-LCC-28-R (SMD)
PSB 2163	Q67100-H6460	P-DIP-28

Pin Configurations
(top view)

P-DSO-28



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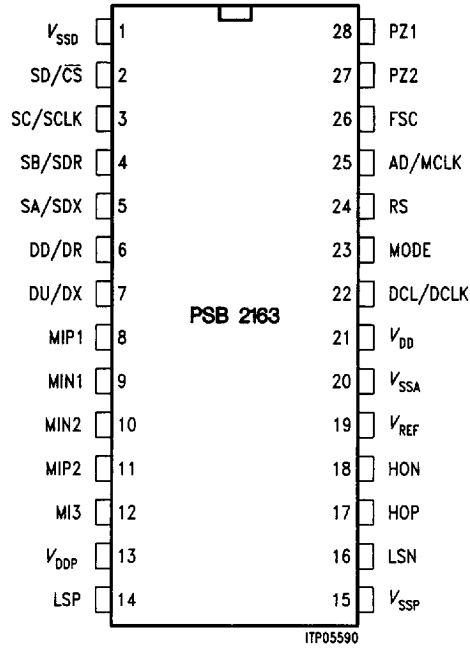
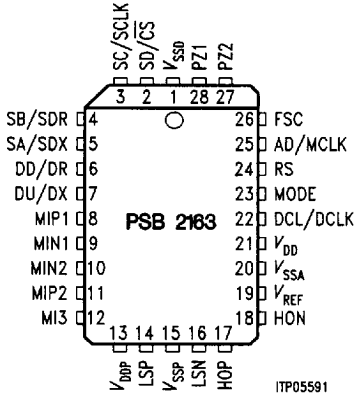


P-LCC-28-R



1.1 Pin Definitions and Functions

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
21	V_{DD}	—	Power supply (5 V ± 5 %)
13	V_{DDP}	—	Power supply (5 V ± 5 %)
1	V_{SSD}	—	Digital Ground (0 V)
20	V_{SSA}	—	Analog Ground (0 V)
15	V_{SSP}	—	Analog Ground (0 V)
23	MODE	I	**Mode Selection:** IOM-2 or serial control/data interface
25	AD	I	**IOM Address:** Chip address in IOM-2 two chip mode
	MCLK	I	**Master Clock:** Synchronous system clock when serial control/data interface is selected
24	RS	I	**Reset:** A high signal on this pin forces the ARCOFI into reset state
26	FSC	I	**Frame Sync:** 8-kHz frame synchronization signal (IOM-2 and SDI-mode)
22	DCL	I	**DCL-System Clock:** 1.536 MHz supplied by the application system clock when IOM-2 mode is selected
	DCLK	I	**DCLK Data Clock:** Data clock of the serial data interface (SDI)
6	DD	I/(OD) [1]	**Data Downstream:** Receive data from layer-1 IOM-2 controlling device
	DR	I	**Data Receive:** Receive data of the serial data interface (SDI)
28	PZ1	O	**Digital Piezo Ringer Output:**
27	PZ2	O	When selected the tone ringer is routed to this output (PZ1 & PZ2 are in opposite phases)

[1] see DD/DU-voice channel swapping (XOP_D)

1.1 Pin Definitions and Functions (cont'd)

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
7	DU	OD/I [1]	**Data Upstream:** Transmit data to the layer-1 IOM-2 controlling device
	DX	OD/O [2]	**Data Transmit:** Transmit data of the serial data interface (SDI)
2	SD	IO	**Programmable I/O PCI Pin SD:** This port pin is only available in IOM-2 TE-mode
	$\overline{CS}$	I	**Chip Select:** A low level indicates a microprocessor access to the ARCOFI-serial control interface (SCI)
3	SC	IO	**Programmable I/O PCI Pin SC:** This port pin is only available in IOM-2 TE-mode
	SCLK	I	**Serial Clock:** Clock signal of the serial control interface (SCI)
4	SB	IO	**Programmable I/O PCI Pin SB:** This port pin is only available in IOM-2 TE-mode
	SDR	I	**Serial Data Receive:** Receive data line of the serial control interface (SCI)
5	SA	IO	**Programmable I/O PCI Pin SA:** This port pin is only available in IOM-2 TE-mode
	SDX	OD/O [3]	**Serial Data Transmit:** Transmit data line of the serial control interface (SCI)
19	V_{REF}	O	**2.4 V Output:** Output for biasing analog single ended inputs
8	MIP1	I	**Microphone Input 1:** This highly symmetrical differential input has been designed for commonly used telephone microphones
9	MIN1	I	

[1] see DD/DU-voice channel swapping (XOP_D)
[2] programmable via bit SDICR.EPP0
[3] programmable via bit SDICR.EPP1

1.1 Pin Definitions and Functions (cont'd)

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
11 10	MIP2 MIN2	I I	**Microphone Input 2:** This highly symmetrical differential input has been designed for commonly used telephone microphones
12	MI3	I	**Microphone Input 3:** This single-ended input has been designed for commonly used telephone microphones
14 16	LSP LSN	O O	**Loudspeaker Output:** LSP & LSN are differential output pins which can drive a 50-Ω loudspeaker directly; a piezo transducer can also be used for ringing signal instead of the loudspeaker
17 18	HOP HON	O O	**Handset Earpiece Output:** HOP & HON are differential output pins which can drive handset earpiece transducers directly

1.2 Logic Symbol

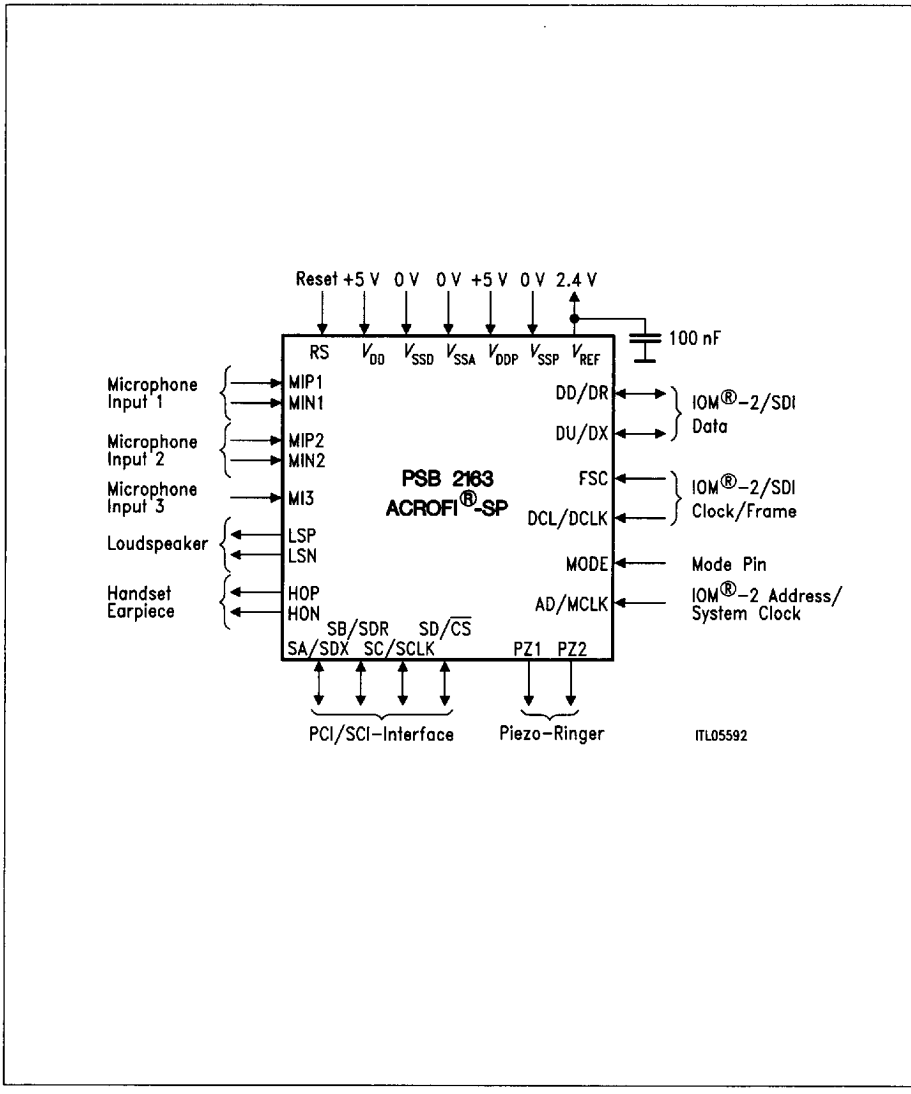


Figure 1
Logic Symbol of the ARCOFI®

1.3 Functional Block Diagram

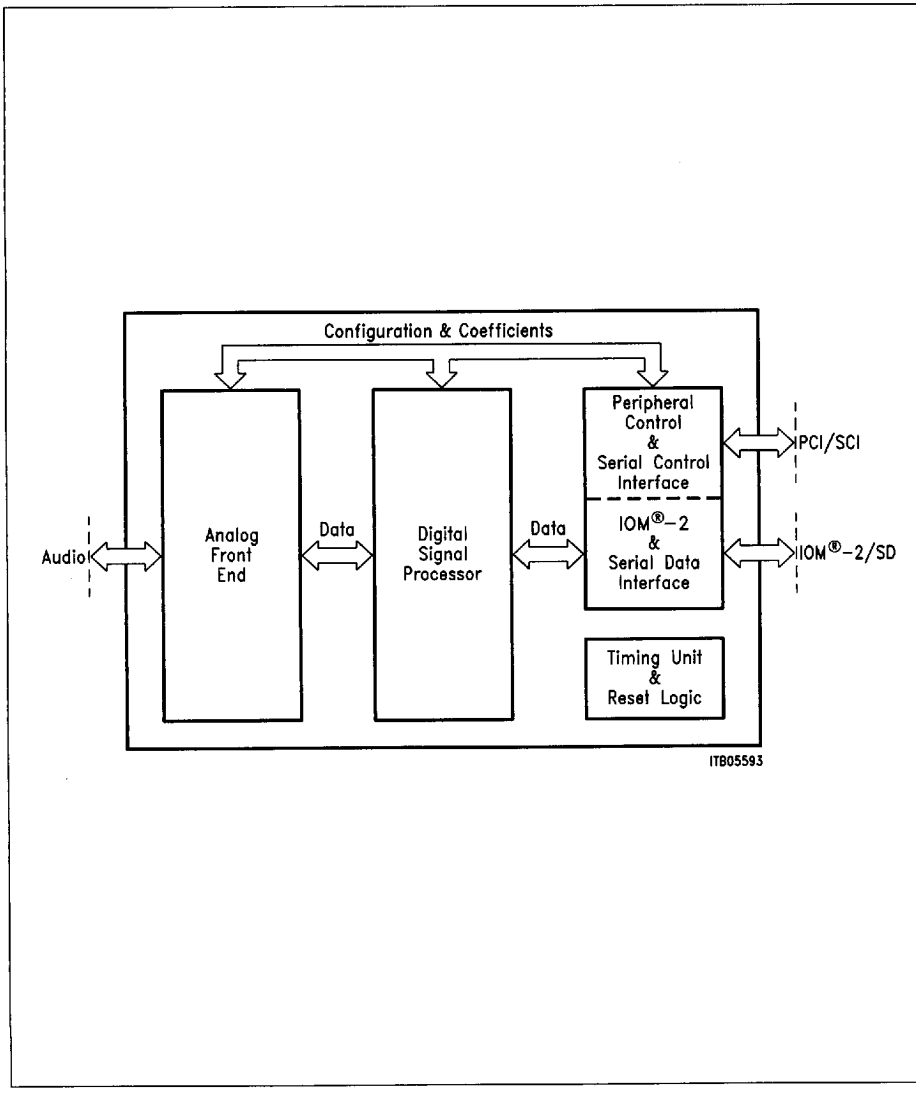


Figure 2
Block Diagram of the ARCOFI®

1.4 System Integration

The complete family of ICs for digital terminals offered by Siemens simplifies the development of these devices and gives a cost-effective solution to the design engineer. The architecture of these terminals is based on a modular interface especially conceived for ISDN and named IOM-2.

Figure 3 shows an example of an integrated multifunctional ISDN-S terminal using the ISAC®-S TE. The ISAC-S TE (ISAC-S: ISDN S-Access controller PSB 2186) provides the S interface and separates the B and D channels.

In this example one ICC (ICC: ISDN Communication Controller PEB 2070) is used to handle data packets on the D-channel. A voice processor is connected to a programmable digital signal processing codec filter (ARCOFI) via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication and B2 for data communication.

Typical terminal applications are described in the next sections.

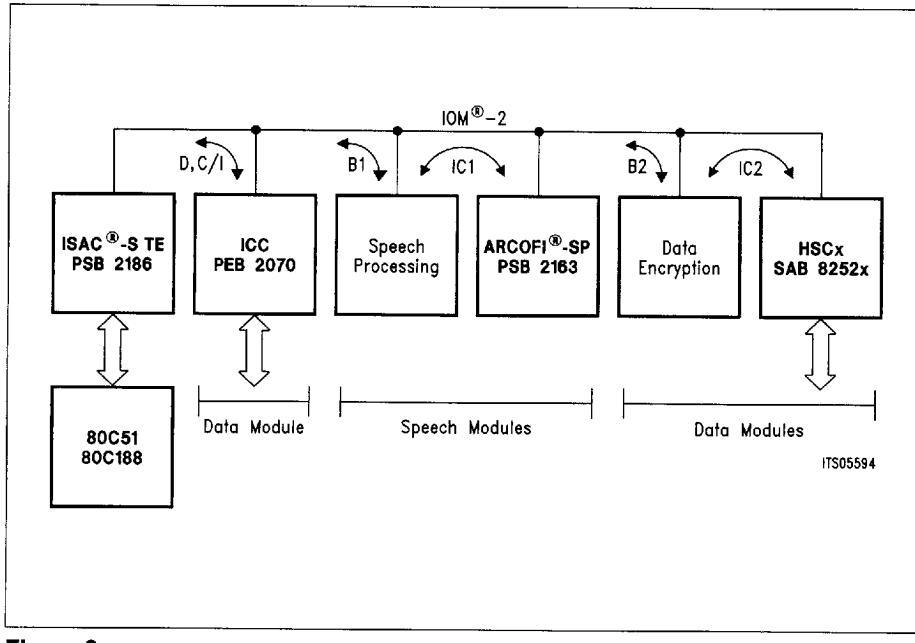


Figure 3
Example of ISDN-S Voice/Data Terminal

1.4.1 ISDN-Voice Terminal

Figure 4 shows a typical solution for a voice terminal for S interface.

The ARCOFI offers the functions of CODEC, filtering and speakerphone. It also carries out the functions of tone ringing, DTMF, and A/D- and D/A-conversions. The ARCOFI permits the direct connection of a handset and a speakerphone/loudspeaker.

The ARCOFI can be programmed and read out by the µC via the IOM-2-interface and the ISAC-S TE. The same µC supervises the keyboard functions and the function hook-on/off.

The S-interface functions such as activation/deactivation, clock recovery, clock resynchronization as well as the layer-2 functions like LAPD-protocol handling are executed by the ISDN-Subscriber Access Controller, also called ISAC-S TE PSB 2186.

A U_{K0}-interface telephone can easily be derived from the voice terminal shown on **figure 4** by replacing the ISAC-S with the ISDN-Communication Controller ICC PEB 2070 and the ISDN-Echo Cancellation Unit IEC PEB 2091.

A U_{P0}-interface telephone is obtained by interchanging the IEC with the ISDN-Burst Controller IBC PEB 2095. In this configuration the ICC PEB 2070 and the IBC PEB 2095 can be replaced by the ISAC-P TE PSB 2196.

Figure 5 shows a typical solution for a voice terminal for U_{K0}- or U_{P0}-interface.

In any case the whole terminal is power supplied either by the ISDN-Remote Power Controller IRPC PSB 2120 or by the General Purpose Power Controller GPPC PSB 2121.

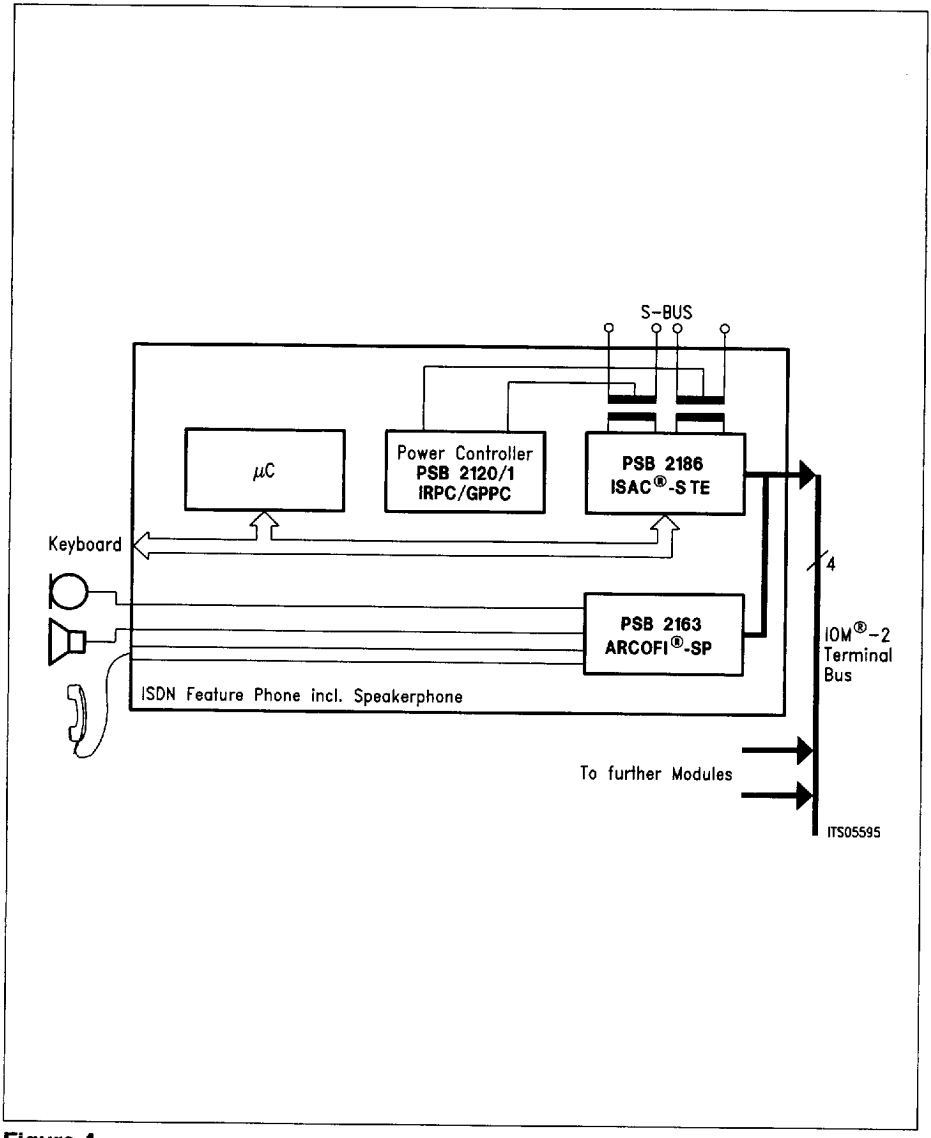
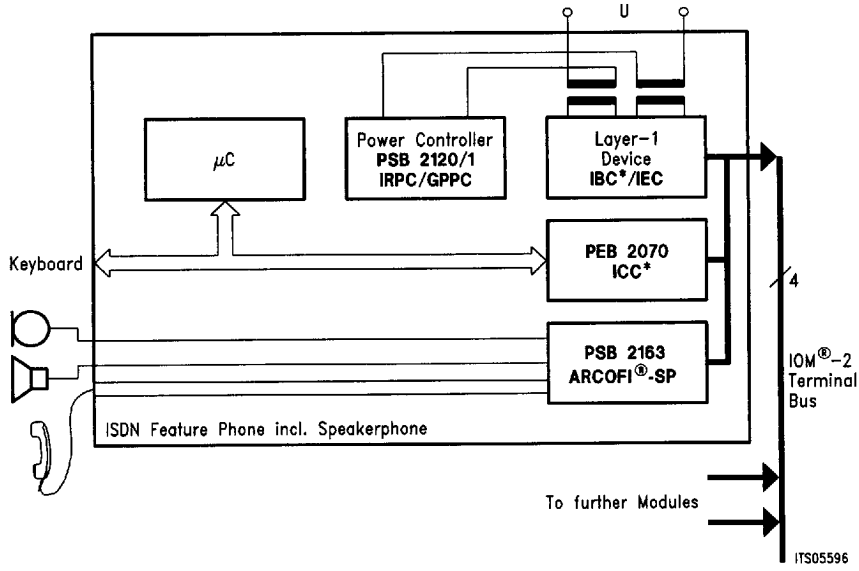


Figure 4
Basic ISDN S-Voice Terminal



* ICC and IBC can be replaced by the ISAC®-P TE PSB 2196

Figure 5
Basic ISDN U-Voice Terminal

1.4.2 Terminal Adapter a, b for Analog Telephones

Figure 6 shows how to implement a terminal adapter (a, b) connecting analog telephones to the ISDN-world. A SLIC can be connected to the ARCOFI.

The tip and ring information is transmitted transparently through the ARCOFI via the C/I-channel of the IOM-channel 1, through the ISAC-S TE to the µC.

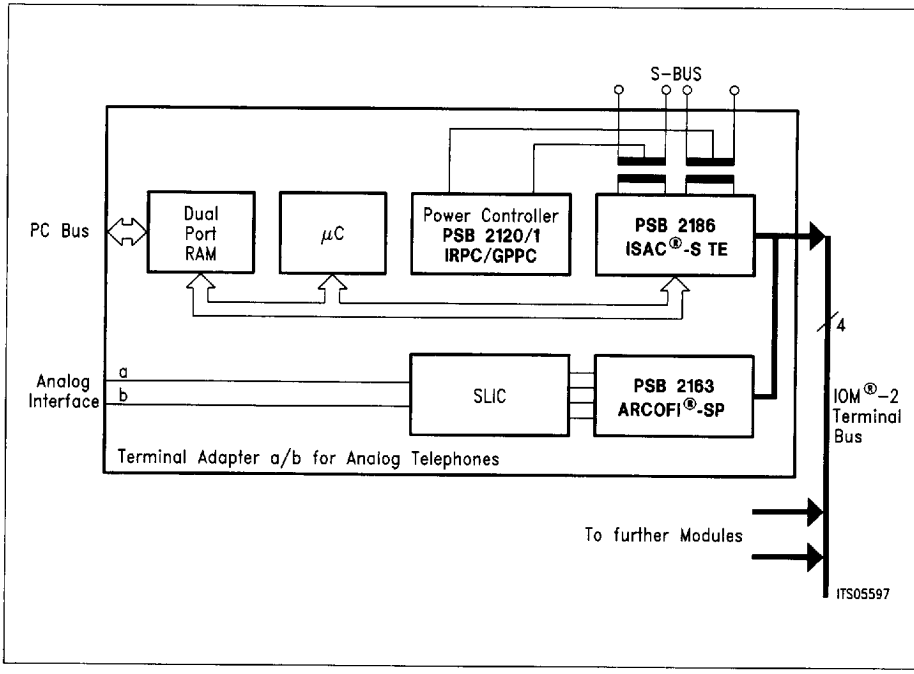


Figure 6
Terminal Adapter a, b for Analog Telephones

1.4.3 Voice/Data Terminal (PC-Card)

Figure 7 shows a voice/data terminal developed on a PC-card. The ITAC PSB 2110 (ITAC: ISDN-Terminal Adapter Circuit) ensures the bit rate adaptation necessary to connect a non ISDN-terminal (V.24) to the ISDN-world.

The COM-IC is an UART (type: 8250 or 16450) which is necessary for modem applications.

The Dual Port RAM is used for data transfer between the terminal processor and the PC. The card is powered by the PC, and thus no power controller is necessary.

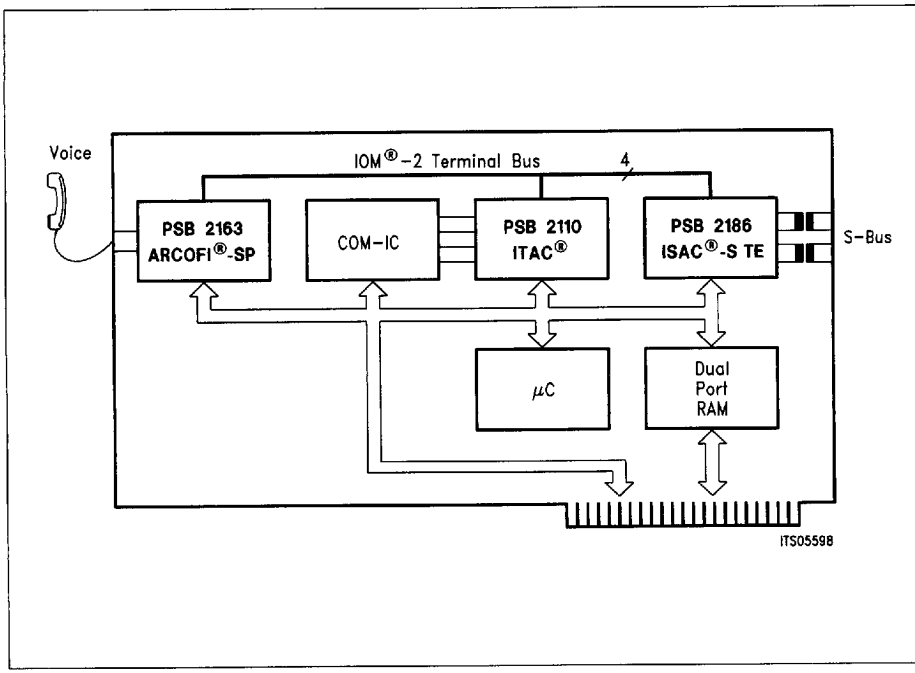


Figure 7
PC-Card as an ISDN-Voice/Data Terminal

1.4.4 Multifunctional ISDN-Terminal

Figure 8 gives an example of a multifunctional terminal. The HSCX SAB 82525 (HSCX: High-Level Serial Communications Controller Extended) simplifies the realization of an intelligent X.25 terminal adapter module whereas the ITAC PSB 2110 offers X.21, V.24, V.110 or V.120 interfaces for non ISDN-terminals.

The µC connected to the ISAC-S TE PSB 2186 is the system master. The two other µCs are the slaves. When a slave µC wants to intervene, it informs the master via the C/I-channel of IOM-2 channel 1.

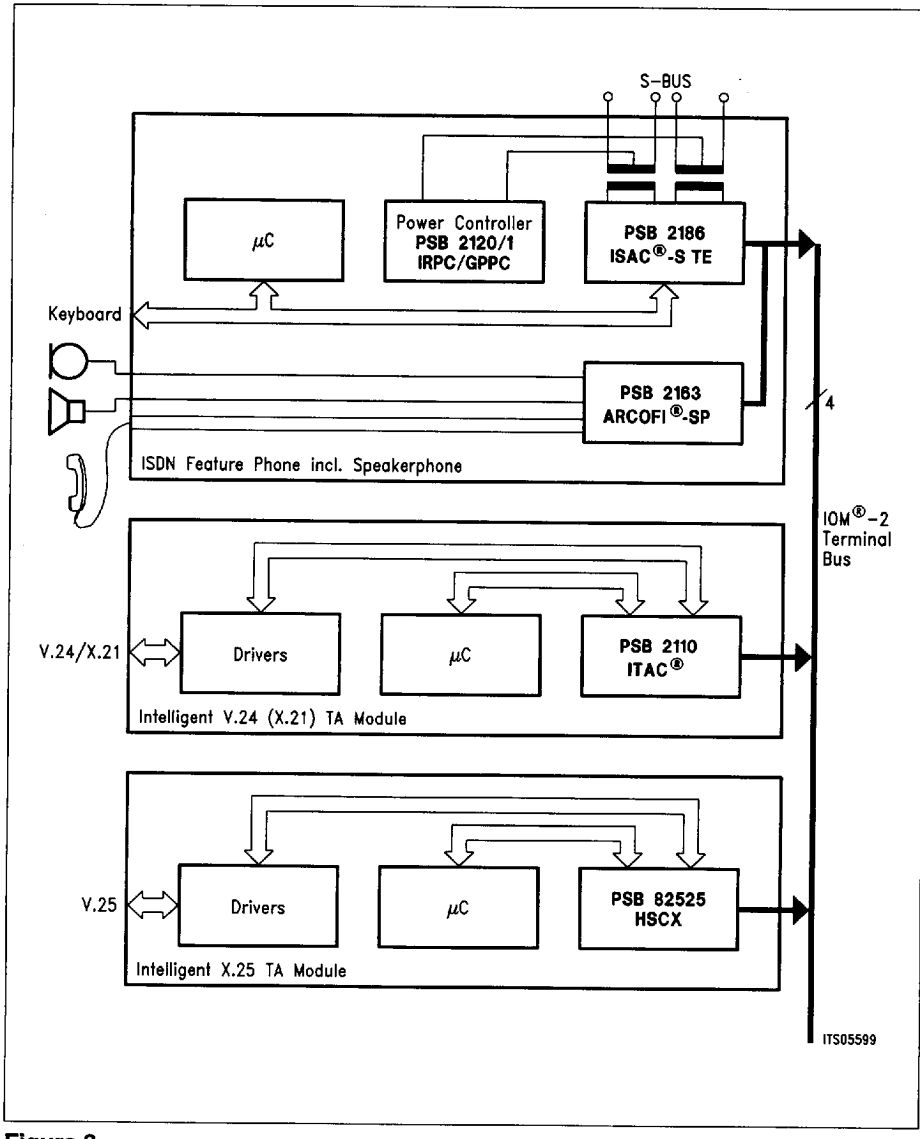


Figure 8
Multifunctional ISDN-Terminal

1.4.5 Digital Voice Terminal

The Serial Control Interface allows the ARCOFI to be programmed directly from a serial port of a microcontroller.

The voice data may be transmitted via the IOM-2 interface or on a PCM-interface provided from other transceiver devices. If the Serial Data Interface (SDI) is selected the PCM-data rate can vary from 64 kbit/s up to 4096 kbit/s.

Figure 9 shows a PABX-voice terminal using the ISAC-P TE PSB 2196 together with a Motorola type microcontroller. **Figure 10** shows a PABX-voice terminal using a transceiver device without IOM-2 interface.

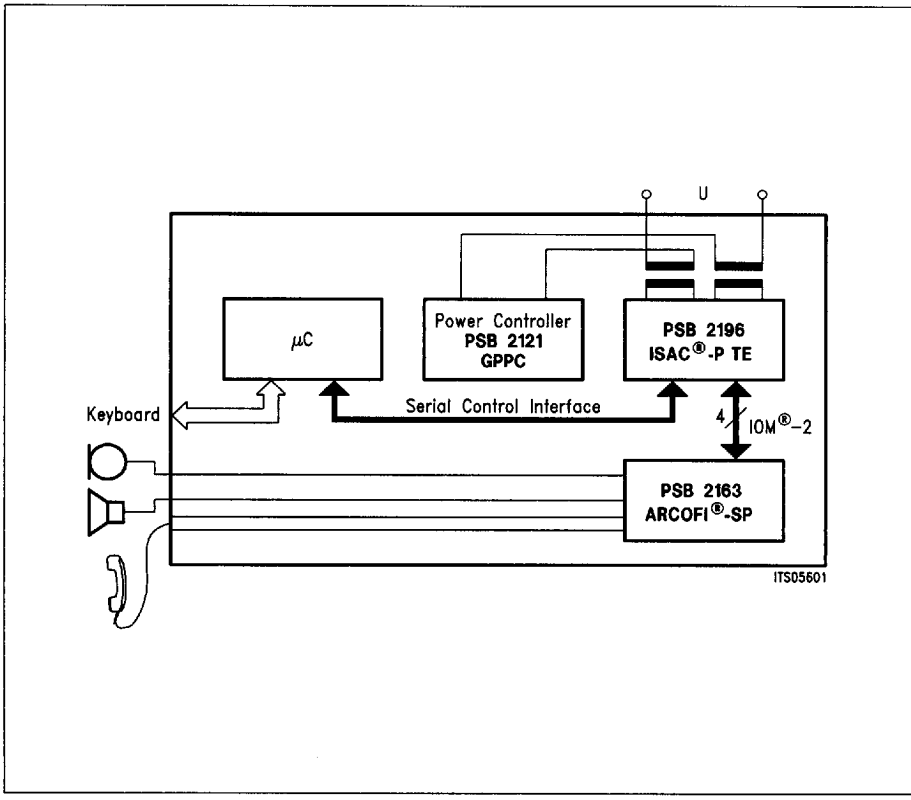


Figure 9
U_{P0} PABX-Voice Terminal

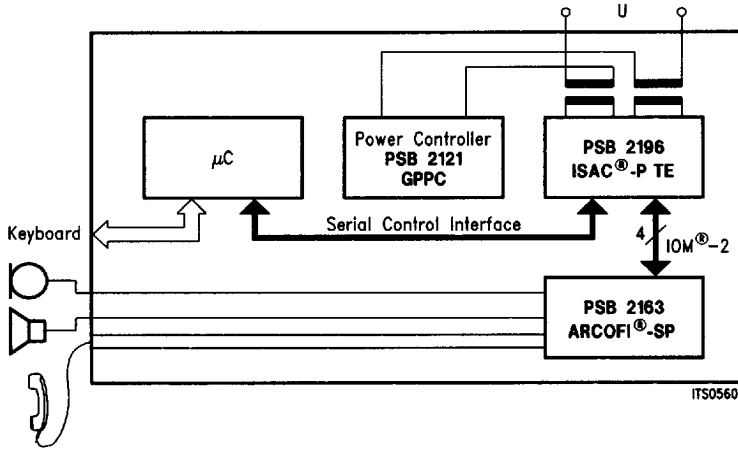


Figure 10
PABX-Voice Terminal in Non-IOM®-2 Architecture

1.4.6 IOM®-2 Line Card Application

Some applications require the ARCOFI to connect directly to the IOM-2 interface of a line card. The IOM-channel is selected via pin-strapping. The ARCOFI is programmed via the MONITOR channel of the selected IOM-channel. Up to two ARCOFIs can be distinguished via AD input on the same IOM-channel.

This configuration allows control of up to 16 ARCOFIs on one IOM-2 interface of a line card controller.

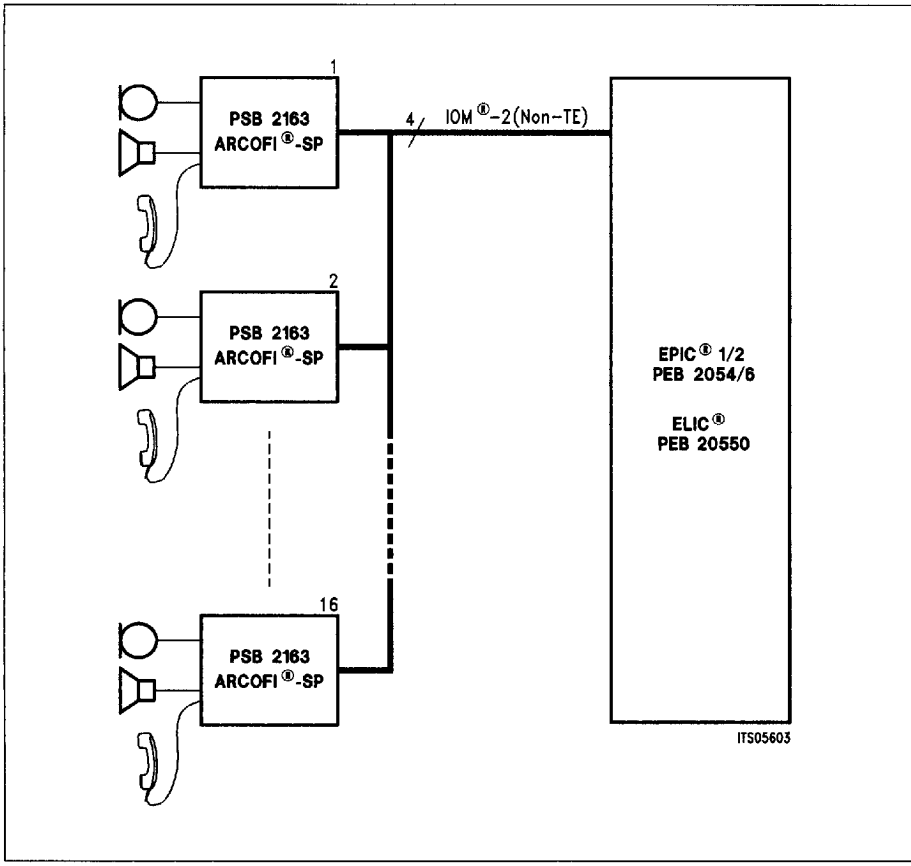


Figure 11
ARCOFI® Line-Card Application

1.4.7 Primary Rate Application

The ARCOFI is designed to be connected to a 24 or 32 time-slot PCM-interface used e.g. on primary rate equipment. The PCM-data is transmitted via the serial data interface while programming of the ARCOFI is done on the serial control interface.

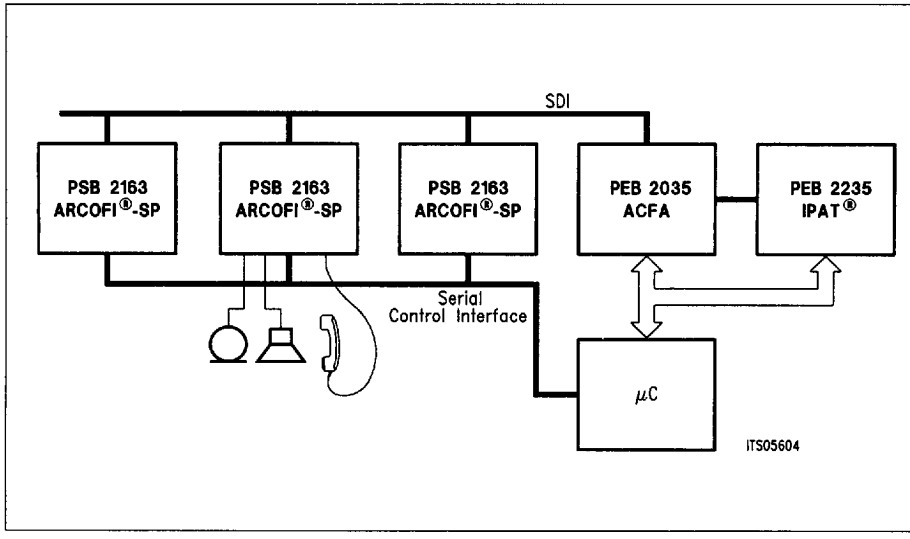


Figure 12
Primary Rate Application

1.4.8 Group 3 Fax / Modem Adapter

The ARCOFI can be connected to a standard fax or modem chip set designed for analog networks. The ARCOFI converts the analog signal to PCM-data which are transmitted over the digital network.

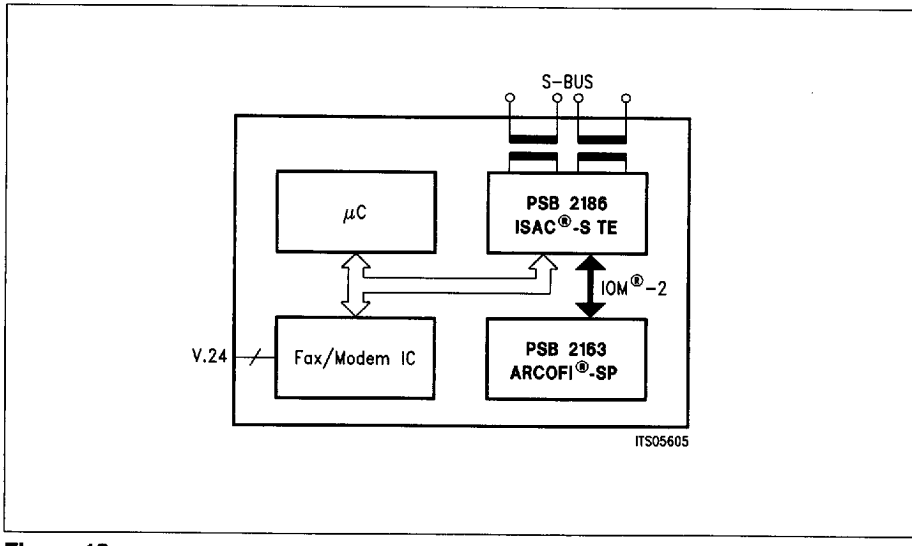


Figure 13
Group 3 Fax/Modem Adapter

2 Functional Description

The ARCOFI bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM-digital world by providing a full PCM-CODEC with all the necessary transmit and receive filters. A block diagram of the ARCOFI is shown in **figure 14.**

The ARCOFI can be subdivided in three main blocks:

- The ARCOFI Analog Front End (AFE)
- The ARCOFI Signal Processor (ASP)
- The ARCOFI Digital Interface (ADI)

A detailed description can be found in the following chapters.

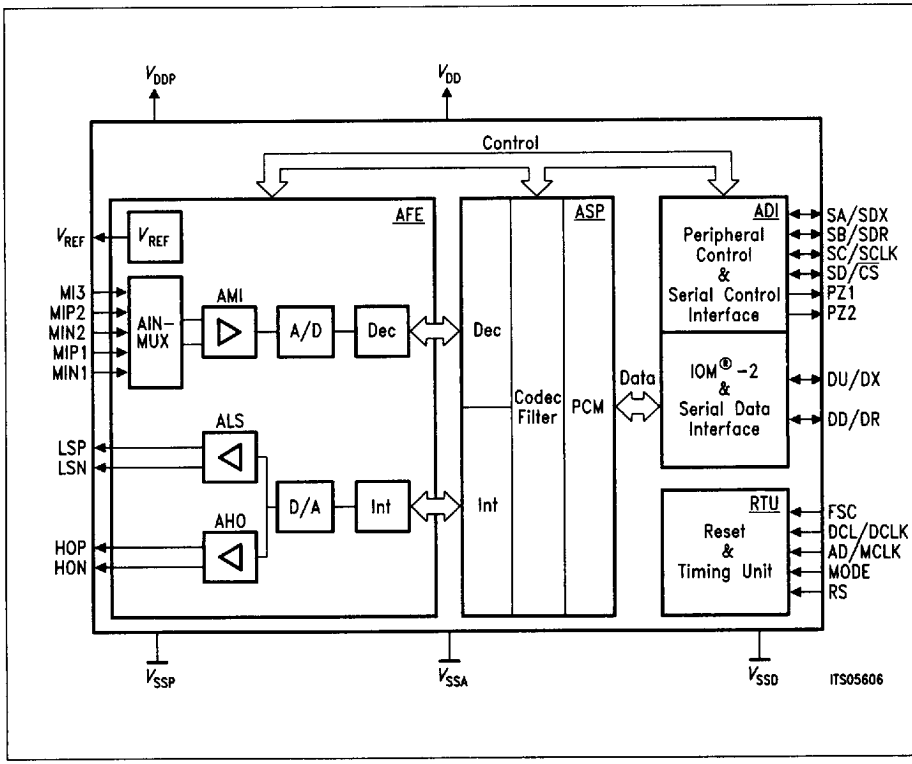


Figure 14
Architecture of the ARCOFI®

2.1 Analog Front End (AFE) Description

The Analog Front End section of the ARCOFI is the interface between the analog transducers and the digital signal processor. In the transmit direction, the AFE-function is to amplify the transducer input signals (microphones) and to convert them into digital signals. In the AFE-receive section, the incoming digital signal is converted to an analog signal which is output to an earpiece and/or a loudspeaker.

A block diagram of the AFE is shown in **figure 15.**

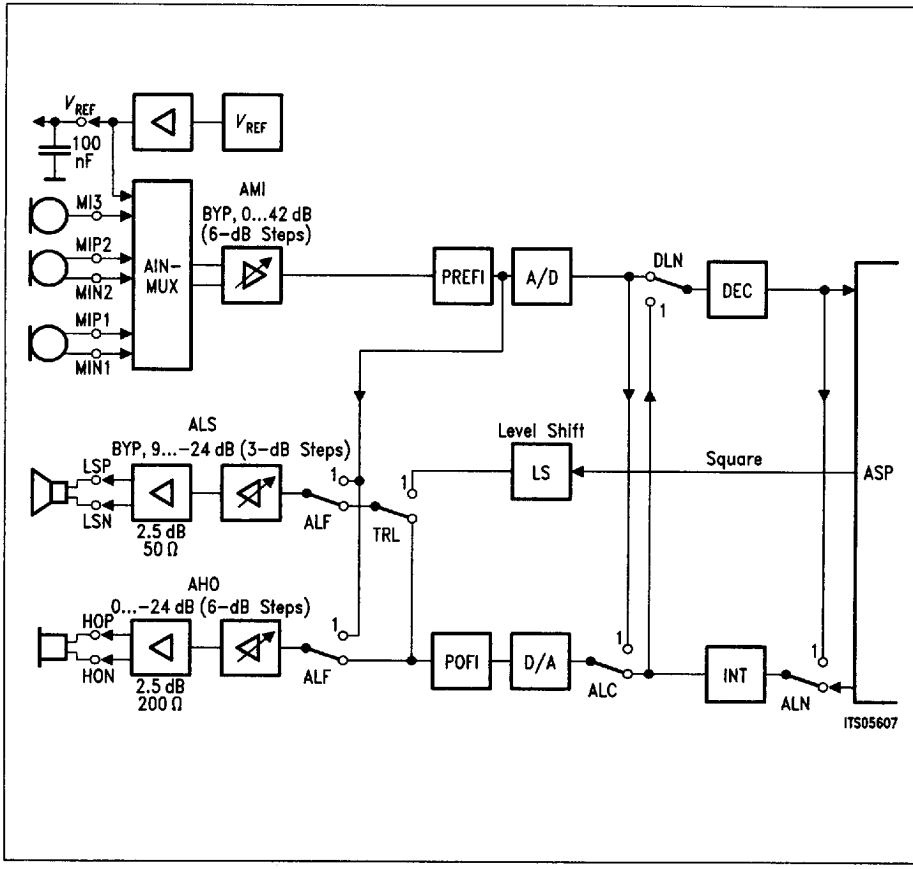


Figure 15
Signal Flow Graph of the AFE

2.1.1 Description of the Analog I/O

Two differential inputs (MIP1/MIN1 and MIP2/MIN2) and one single-ended input (MI3) are connected to the amplifier AMI via an analog input multiplexer. The programmable amplifier AMI provides a coarse gain adjustment range. Fine gain adjustment is performed in the digital domain via the programmable gain adjustment stage GX (see signal processor section). This allows a perfect level adaptation to various types of microphone transducers without loss in the signal to noise performance.

Fully differential output HOP/HON connects the amplifier AHO to a handset earpiece. Differential output LSP/LSN is provided for use with a 50-Ω loudspeaker. Up to 100 mW (sine wave) of power can be delivered to the loudspeaker via the amplifier ALS. The programmable amplifiers AHO and ALS provide a coarse gain adjustment range. Fine gain adjustment is performed in the digital domain via the programmable adjustment stage GR.

Two implemented AFE-configuration registers (ATCR & ARCR) provide a high flexibility to accommodate an extensive set of user procedures and terminal attributes.

2.1.2 AFE-Attenuation Plan

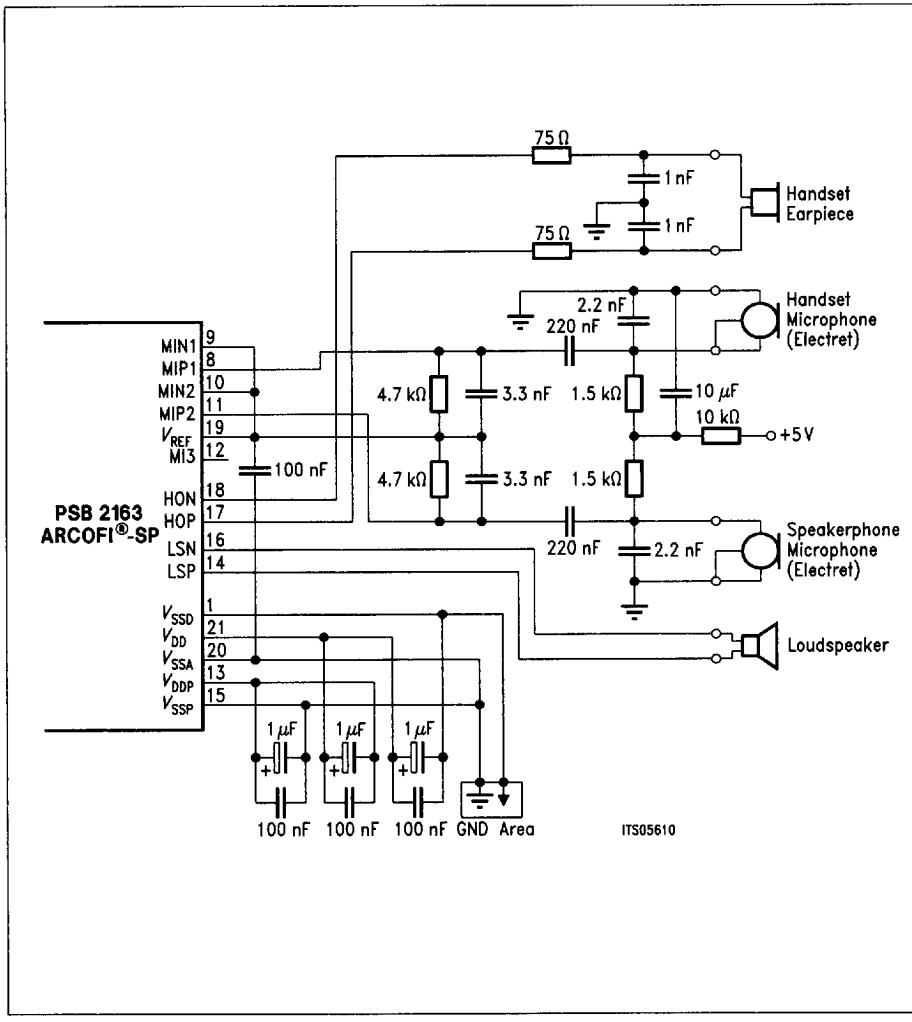
Transmit Direction

Parameter Transmit	Limit Values		Unit	Reference
	0dBm0	max.		
MIP1/MIN1	1.33E-02	1.91E-02	Vp	V
MIP2/MIN2	9.38E-03	1.35E-02	Vrms	V
Microphone input level at max gain	– 42	– 38.86	dBm0	1.2 V
AMI = 42 dB	– 38.33	– 35.19	dBm	0.775 V
MIP1/MIN1	1.67E-00	2.40E-00	Vp	V
MIP2/MIN2	1.18E-00	1.70E-00	Vrms	V
Microphone input level at min gain	0	3.14	dBm0	1.2 V
AMI = 0 dB	3.67	6.81	dBm	0.775 V
MI3	1.06E-01	1.51E-01	Vp	V
Input level at max gain	7.46E-02	1.07E-01	Vrms	V
AMI = 24 dB	– 24	– 20.86	dBm0	1.2 V
	– 20.37	– 17.19	dBm	0.775 V
MI3	8.36E-01	1.20E-00	Vp	V
Input level at min gain	5.91E-01	8.49E-01	Vrms	V
AMI = 0 dB	– 6	– 2.86	dBm0	1.2 V
	– 2.33	0.81	dBm	0.775 V

Receive Direction

Parameter Receive	Limit Values		Unit	Reference
	0dBm0	max.		
LSP/LSN	2.23E-00	3.20E-00	Vp	V
Output level symmetrical	1.58E-00	2.26E-00	Vrms	V
in a 50-Ω load	2.5	5.64	dBm0	1.2 V
ALS = 2.5 dB	6.17	9.31	dBm	0.775 V
LSP/LSN	1.41E-01	2.02E-01	Vp	V
Output level symmetrical	9.95E-02	1.43E-01	Vrms	V
in a 50-Ω load	– 21.5	– 18.36	dBm0	1.2 V
ALS = – 21.5 dB	– 17.83	– 14.69	dBm	0.775 V
HOP/HON	2.23E-00	3.20E-00	Vp	V
Output level symmetrical	1.58E-00	2.26E-00	Vrms	V
in a 200-Ω load	2.5	5.64	dBm0	1.2 V
AHO = 2.5 dB	6.17	9.31	dBm	0.775 V
HOP/HON	2.81E-01	4.03E-01	Vp	V
Output level symmetrical	1.99E-01	2.85E-01	Vrms	V
in a 200-Ω load	– 15.5	– 12.36	dBm0	1.2 V
AHO = – 15.5 dB	– 11.83	– 8.69	dBm	0.775 V

2.1.3 Interface to Acoustic Transducers



Note: ESD and EMV requirements are not included.

Figure 16
Example to Connect the AFE to Acoustic Transducers

2.2 ARCOFI® Signal Processor (ASP) Description

The ARCOFI signal processor (ASP) has been conceived to perform all CCITT and ETSI (NET33) recommended filtering in transmit and receive paths and is therefore fully compatible to the G.714 CCITT and ETSI (NET33) specifications. The data processed by the ASP is provided in the transmit direction by an oversampling A/D-converter situated in the analog front end (AFE). Once processed, the speech signal is converted into an 8 bit A-law or μ-law PCM-format or remains as a 16-bit linear word (2s complement) if the compander is by-passed. The by-passing of the companding depends on the bit setting in the configuration register DFICR (VDM-bits).

In the receive direction, the incoming PCM-stream is expanded into a linear format (if the linear mode is selected, the expansion logic is by-passed) and subsequently processed until it is passed to the oversampling D/A-converter.

Additionally to these standard codec functions, the ARCOFI provides a universal tone generation unit and a high quality speakerphone function.

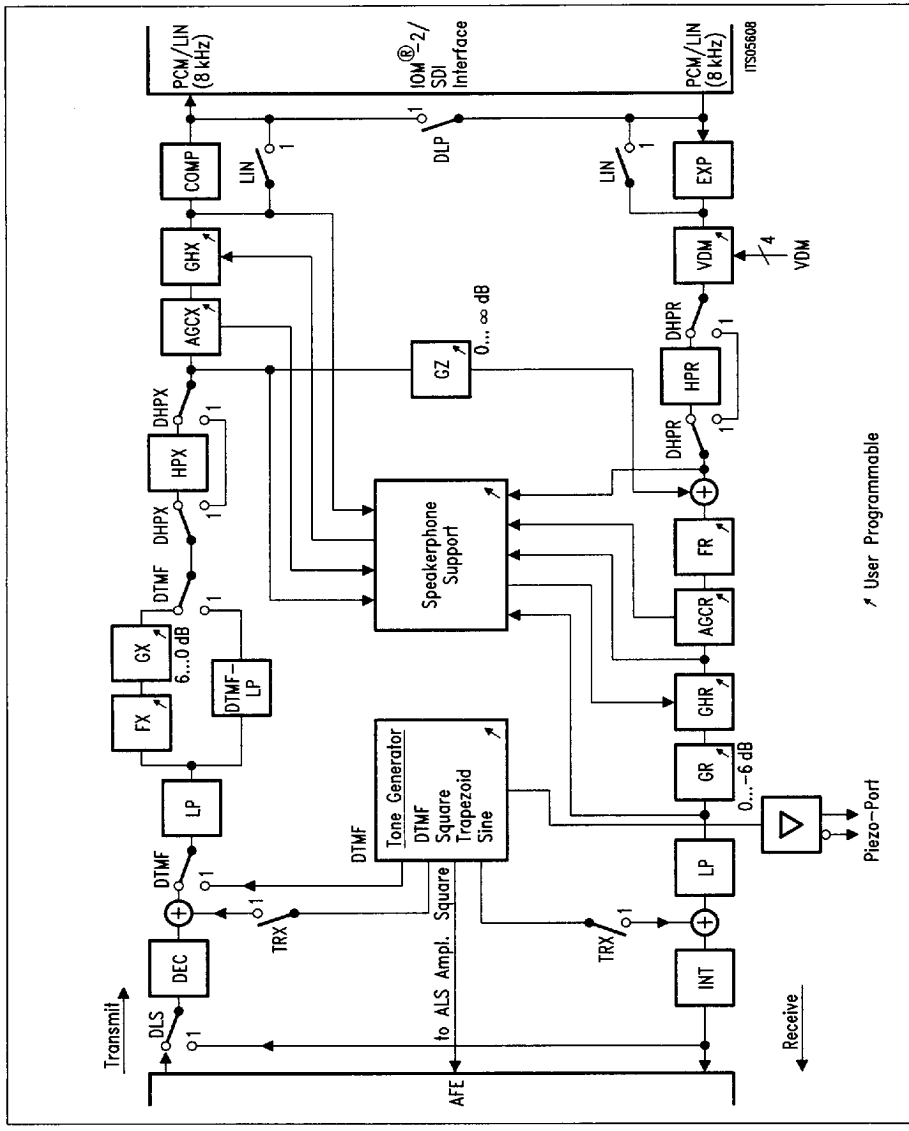


Figure 17
Processor Signal Flow Graph

2.2.1 Transmit Signal Processing

In the transmit direction a series of decimation filters reduces the sampling rate down to the 8-kHz PCM-rate. These filters attenuate the out-of-band noise by limiting the transmit signal to the voice band.

The decimation stages end with a EWDF low-pass filter which band-limits the voice signal to the CCITT G.714 and ETSI (NET33) recommendations. The ARCOFI meets or exceeds all the CCITT and ETSI (NET33) recommendations on attenuation distortion and group delay distortion.

If the tone generation unit is connected to the transmit direction (TGSR.DTMF = 1), a special 2-kHz DTMF-low-pass filter is placed in the transmit path. This filter guarantees an attenuation of all unwanted frequency components, if DTMF-signals are transmitted. Additionally, it is possible to add a programmable tone signal to the transmit voice signal (TGSR.TRX = 1).

The GX-gain adjustment stage is digitally programmable allowing the gain to be programmed from + 6 to 0 dB in steps of ≤ 0.25 dB (– ∞ dB and others are also possible). Two bytes are necessary to set GX to the desired value. On reset, the GX-gain stage is by-passed.

The transmit path contains a programmable high performance frequency response correction filter FX allowing an optimum adaptation to different types of microphones (dynamic, piezoelectric or electret). Twelve bytes are necessary to set FX to the desired frequency correction function. On reset, the FX-frequency correction filter is by-passed. **Figure 18** shows the architecture of the FX/FR-filter.

A high-pass filter (HPX) is also provided to remove power line frequencies.

The voice signal, after being linearly processed, can be output as an 8-bit PCM-word according to the CCITT G.711 A-law or the North-American μ-law format. If desired the companding stage can be by-passed, a 16-bit linear word (2s complement) is then output to the IOM-2 or SDI-interface.

2.2.2 Receive Signal Processing

In the receive path the incoming PCM-signal is expanded into a linear code according to the selected A-law or μ-law. If the linear mode is chosen, the PCM-expander circuit is by-passed and a 16-bit linear word (2s complement) has to be provided to the processor.

The block VDM offers several possibilities of voice/data manipulation for special applications.

A programmable sidetone gain stage GZ adds a sidetone signal to the incoming voice signal. The sidetone gain can be programmed from – 54 to 0 dB within a ± 1 dB tolerance

range (– ∞ dB and others are also possible). Respectively two bytes are coded in the CRAM to set GZ to the desired value. On reset, the GZ-gain stage is disabled (– ∞ dB).

A high-pass filter (HPR) is also provided to remove disturbances from 0 to 50/60 Hz due to the telecommunication network.

The FR-frequency correction response filter is similar to the FX-filter allowing an optimum adaptation to different types of loudspeakers or earpieces. Twelve bytes are necessary to set FR to the desired frequency correction function. On reset, the FR-frequency correction filter is by-passed.

The GR-gain adjustment stage is digitally programmable from – 6 to 0 dB in steps ≤ 0.25 dB (– ∞ dB and others are also possible). Respectively two bytes are coded in the CRAM to set GR to the desired value. On reset, the GR-gain stage is by-passed.

A low-pass EWDF-filter limits the signal bandwidth in the receive direction according to CCITT and ETSI (NET33) recommendations.

A series of low-pass interpolation filters increases the sampling frequency up to the desired value.The last interpolator feeds the D/A-converter.

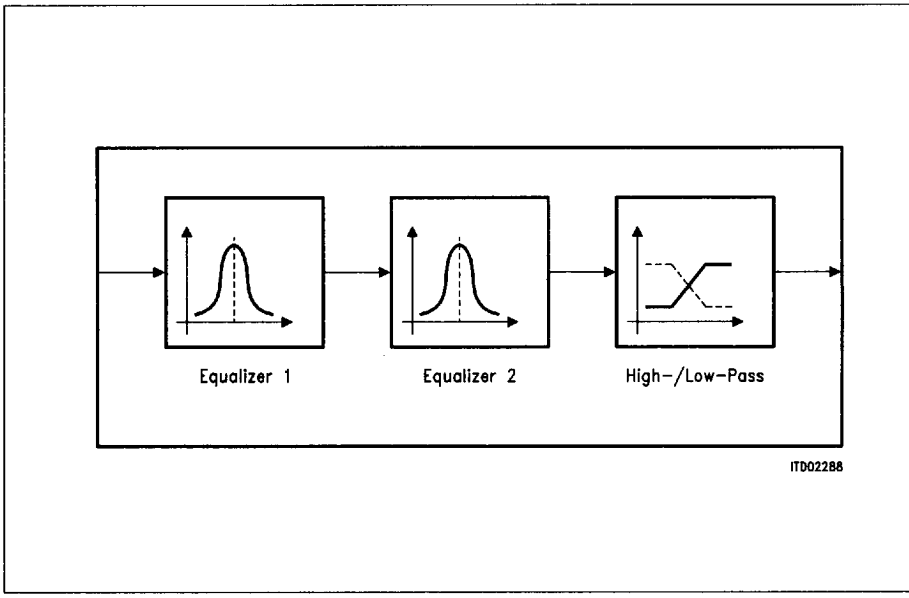


Figure 18
Architecture of the FX- and FR-Correction Filter

2.2.3 Programmable Coefficients

This section gives a short overview of important programmable coefficients. For more detailed information and about special applications, a special coefficient software package is available (ARCOS-SP PLUS SIPO 2163).

Description of the programmable level adjustment parameters:

Parameter	# of CRAM Bytes	Range	Comment
GX	2	12 to $-\infty$ dB **6 to 0 dB**	Transmit gain adjustment Transmission characteristics guaranteed
GR	2	12 to $-\infty$ dB **0 to – 6 dB**	Receive gain adjustment Transmission characteristics guaranteed
GZ	2	12 to $-\infty$ dB	Sidetone gain adjustment

Coefficients for GX, GR and GZ:

Gain [dB]	MSB	LSB	Gain [dB]	MSB	LSB	Gain [dB]	MSB	LSB
12.0	10_H	01_H	0	$A0_H$	01_H	– 12.0	$A9_H$	01_H
11.0	10_H	31_H	– 0.5	$B3_H$	42_H	– 13.0	$9C_H$	51_H
10.0	10_H	13_H	– 1.0	$A3_H$	$2B_H$	– 14.0	99_H	13_H
9.0	01_H	$4B_H$	– 1.5	$A2_H$	32_H	– 15.0	$8C_H$	$1B_H$
8.0	20_H	94_H	– 2.0	BB_H	$4A_H$	– 16.0	82_H	$7B_H$
7.0	30_H	94_H	– 2.5	BB_H	13_H	– 17.0	84_H	$4B_H$
6.0	13_H	51_H	– 3.0	BA_H	29_H	– 18.0	89_H	$6A_H$
5.5	$B0_H$	39_H	– 3.5	BA_H	$5B_H$	– 19.0	$8B_H$	$0C_H$
5.0	$A0_H$	49_H	– 4.0	$A2_H$	01_H	– 20.0	84_H	$1C_H$
4.5	23_H	01_H	– 4.5	AA_H	$1B_H$	– 21.0	$8C_H$	$1C_H$
4.0	22_H	$B4_H$	– 5.0	$9B_H$	$3A_H$	– 22.0	82_H	$7C_H$
3.5	23_H	12_H	– 5.5	AA_H	33_H	– 23.0	84_H	$4C_H$
3.0	32_H	$A4_H$	– 6.0	AA_H	22_H	– 24.0	89_H	$6B_H$
2.5	$B1_H$	BC_H	– 7.0	$B9_H$	$2C_H$	– 25.0	$8B_H$	$0D_H$
2.0	$B1_H$	03_H	– 8.0	$9A_H$	BC_H	– 26.0	84_H	$1D_H$
1.5	33_H	39_H	– 9.0	$9B_H$	13_H	$-\infty$	88_H	01_H
1.0	$B2_H$	$5A_H$	– 10.0	$9B_H$	32_H			
0.5	$B3_H$	49_H	– 11.0	93_H	02_H			

2.2.4 Tone Generation

2.2.4.1 Tone Generation Architecture

The ASP contains a universal tone generator which can be used for tone alerting, call progress tones, DTMF-signals or other audible feedback tones.

For the receive channel, a universal switching to each signal path (earpiece, loudspeaker and piezo ringer) is implemented. In the earpiece and loudspeaker direction, an addition of the programmed tone sequence (sine-wave, trapezoid, square-wave and DTMF) with the incoming voice signal is possible.

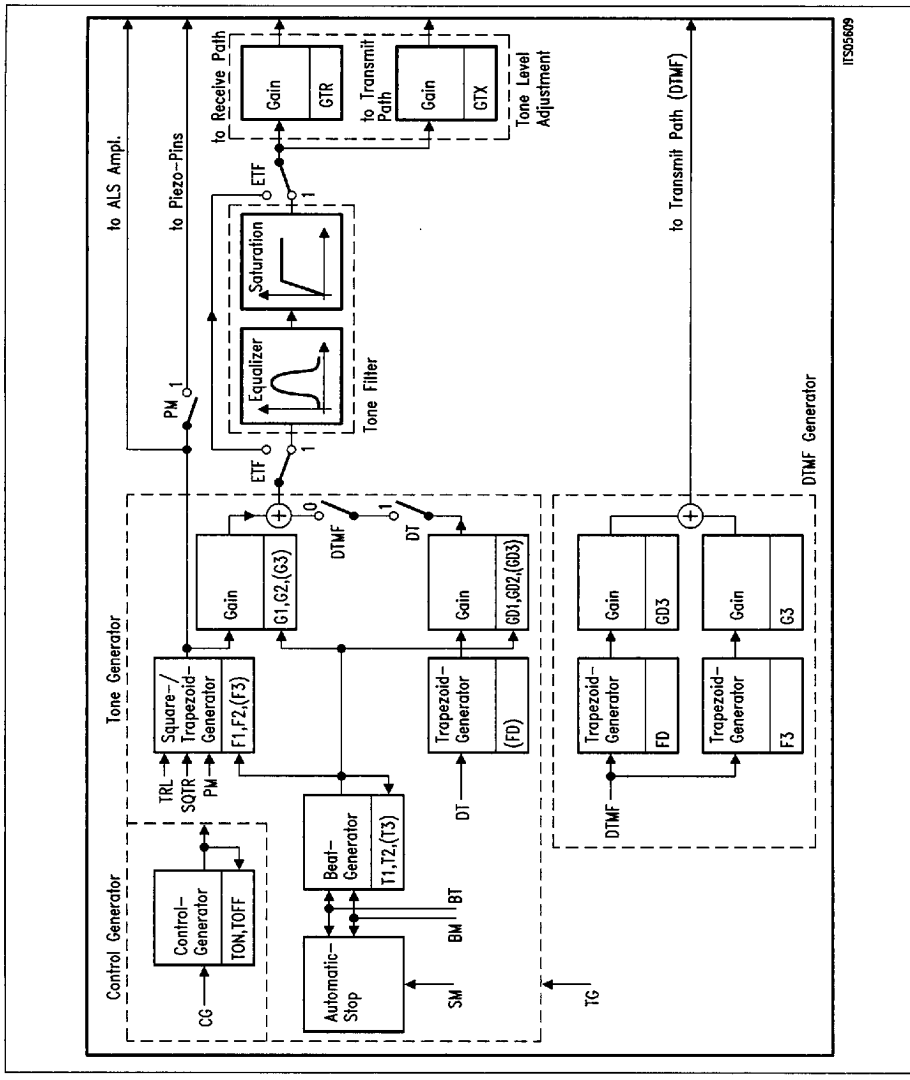
For the transmit direction, a supplementary DTMF-generator is implemented. If the DTMF-generator is active (TGSR.DTMF = 1), only a part of the tone generator (TG) is available for the receive direction (one or two tone sequences). In addition, a universal switching to the transmit path is also possible (TGSR.TRX).

All the tone generation configurations are programmable in the registers TGCR and TGSR (see description in chapter 4). A signal flow graph of the ARCOFI-tone generation unit is shown in **figure 19**.

The tone generation can be subdivided into five main blocks:

- Control Generator (CG)
- Tone Generator (TG)
- Tone Filter (TF)
- Tone Level Adjustment (TLA)
- DTMF-Generator (DTG)

A detailed description of the five main tone generation blocks follows in the next sub-sections.



Note: Adjustments in brackets are only available if the DTMF-generator is switched off (TGCR.DTMF = 0).

Figure 19
Signal Flow Graph of the Tone Generation Unit

2.2.4.2 Control Generator

In conjunction with the control generator it is possible to generate very complex signal sequences without reprogramming the necessary parameters (e.g. pulsed three tone calls). Four typical applications for the control generator programming are shown in **figure 20**.

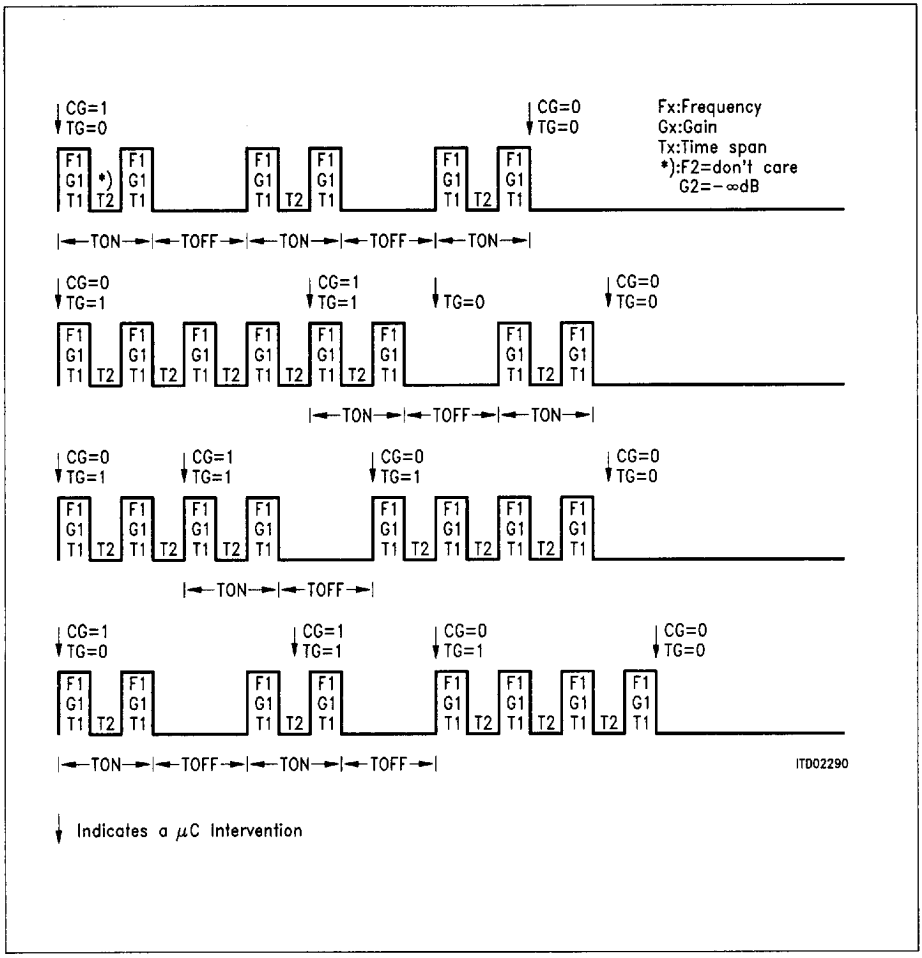


Figure 20
Typical Control Generator Application

Function table of CG/TG-bit setting in TGCR:

TON/TOFF	CG	TG	Generator Output
X	0	0	No tone
X	0	1	Ringing sequence F1, F2, F3 without break
TOFF	1	X	Break between two ringing sequences of F1, F2, F3
TON	1	X	Ringing sequence until next break

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
TON	2	20 ms to 16 min	Period while the tone generator is turned on
TOFF	2	20 ms to 16 min	Period while the tone generator is turned off

2.2.4.3 Tone Generator

The tone generator contains a beat generator, a Square/Trapezoid generator, a second trapezoid generator and an automatic stop for two and three tone ringing signals. With the automatic stop function (SM-bit setting in TGCR) the multitone generation can be stopped after a defined frequency. This avoids unpleasant sounds when stopping the tone generator.

If the control generator is activated (TGCR.CG = 1) the bit setting of TG is insignificant. Otherwise (TGCR.CG = 0) the TG-bit setting controls the activities of the tone generator.

A functional diagram of the tone generator is shown in **figure 21**.

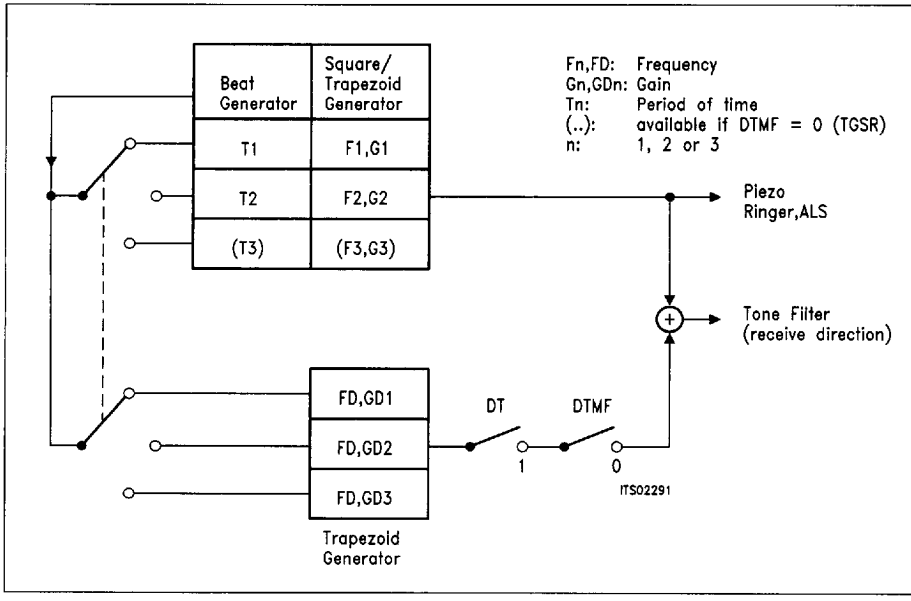


Figure 21
Functional Diagram of the Tone Generator

Distinctive alerting signals, allowing for example the use of different multitone ringing patterns, are all programmable using the beat tone generator in conjunction with the square/trapezoid generator. In the case of two or three tone ringing signals, the square/ trapezoid generator controls the output frequency pitch whilst the beat generator controls the repetition rate. Either square or trapezoid shaped tones can be generated depending on the TGCR.SQTR bit setting. If the piezo mode (PM or TRL in TGSR) is chosen, only a square-wave is available (fixed amplitude of V_{DD}). In this case the SQTR bit in TGCR has no effect.

A secondary trapezoid generator is also built into the ARCOFI. Depending on the DT-bit setting in the TGCR, the output signal of this generator is added to the output signal of the Square/Trapezoid (S/T) generator. In conjunction with the S/T generator, a wide variety of different dual tone signals can be programmed.

If the beat generator (TGCR.BT = 1) is enabled, the automatic stop function (SM-bit setting in TGCR) can be activated. This prevents an uncontrolled turn-off of the tone generator. Only when the generation of the frequency F2 or F3 (depending on the BM-bit setting in TGCR) has been completed, the tone generator will switch off.

Beat generator programming:

BT	BM	DT	Generator Output	
0	0	0	Continuous signal	F1, G1
0	0	1	Continuous signal	F1, G1 + FD, GD1
0	1	0	Continuous signal	F2, G2
0	1	1	Continuous signal	F2, G2 + FD, GD2
1	0	0	Alternating signal	F1, G1, T1; F2, G2, T2
1	0	1	Alternating signal	F1, G1, T1; F2, G2, T2 + FD, GD1, T1; FD, GD2, T2
1	1	0	Alternating signal	F1, G1, T1; F2, G2, T2; F3, G3, T3
1	1	1	Alternating signal	F1, G1, T1; F2, G2, T2; F3, G3, T3 + FD, GD1, T1; FD, GD2, T2; FD, GD3, T3

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
Fn	2/2/2	50 Hz to 4 kHz	Trapezoid shaped tone
		16 kHz/m; ($m \geq 3$)	Square-wave signal
Gn	1/1/1	0 dB to – 48 dB	Gain adjustment for square/trapezoid generator
Tn	2/2/2	10 ms to 8 s	Period of time for two or three tone sequences
FD	2	50 Hz to 4 kHz	Trapezoid shaped tone
GDn	1/1/1	0 dB to – 48 dB	Gain adjustment for trapezoid generator

n is either 1, 2 or 3

Note: 0-dB gain setting of G1, G2 or G3 and GD1, GD2 or GD3 corresponds to the maximum PCM-level (A-Law: + 3.14 dB)

2.2.4.4 Tone Filter

The tone filter contains a programmable equalizer and a saturation amplifier (**see figure 19**). If no filter function is necessary, a by-pass mode can be used (TGCR.ETF = 0). A brief description of the tone filter follows below.

The equalizer is realized as a band-pass filter. The filter parameters (center frequency, bandwidth, and attenuation of the stop-band) are programmable.

A generated square-wave or trapezoid signal can be converted by the equalizer into a sine-wave signal. A maximum attenuation of the first harmonic frequency of 50 dB is possible.

By programming the equalizer as a broadband filter, the quality of the DTMF-signal (receive direction) is improved. A level balancing of the two frequency components can be made with G1, G2, G3 and GD1, GD2, GD3.

The two main purposes of the programmable saturation amplification are:

- Level balancing of the filtered signal (avoidance of overload effects).
- Amplification up to + 12 dB followed by a saturation of the incoming signal. This saturation amplification converts a sine-wave signal into a square-wave or a trapezoid signal where their edges are eliminated. This method produces pleasant ringing tones.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
A1	1	200 Hz to 4 kHz	Center frequency
A2	1	0 to – 1	Bandwidth (strongly dependent on A1 and K)
K	1	0 to 54 dB	Attenuation of the stop-band
GE	1	+ 12 to – 12 dB	Saturation amplification

2.2.4.5 Tone Level Adjustment

The two level adjustment stages GTR and GTX determines the output levels of the tone generation (**see figure 19**).

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
GTX	1	0 dB to – 50 dB (also – ∞ dB)	Level adjustment for the output which is connected to the transmit channel
GTR	1	0 dB to – 50 dB (also – ∞ dB)	Level adjustment for the output which is connected to the receive channel

2.2.4.6 DTMF-Generator (transmit)

The DTMF-generator contains two independent trapezoid generators which can be programmed in a wide frequency and gain range. If the DTMF-generator is active (TGSR.DTMF = 1), the output signal is automatically switched to the transmit direction. In this case the attenuation of the unwanted frequency components is executed by a special DTMF-low-pass filter to the following limits:

Frequency Band	Min. Attenuation
0 – 300 Hz	33 dB
300 – 3400 Hz	20 dB
3400 – 4000 Hz	33 dB

The pre-emphasis of 2 dB between the high and the low DTMF-frequency groups has to be set with the independent gain stages for the two trapezoid generators (G3 and GD3). All generated DTMF-frequencies are guaranteed within a ± 1 % deviation.

DTMF-frequency (F3, FD) programming:

CCITT Q.23	ARCOFI® Nominal	Relative Deviation from CCITT	Coefficients	
			high	low
Low Group				
697	697.1	+ 143 ppm	4F	16
770	770.3	+ 390 ppm	A6	18
852	852.2	+ 235 ppm	45	1B
941	941.4	+ 425 ppm	20	1E
High Group				
1209	1209.5	+ 414 ppm	B4	26
1336	1336.9	+ 674 ppm	C8	2A
1477	1477.7	+ 474 ppm	49	2F
1633	1632.8	– 122 ppm	40	34

Note: The deviations due to the inaccuracy of the incoming clock DCL/MCLK, when added to the nominal deviations tabulated above give the total absolute deviation from the CCITT-recommended frequencies.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
F3	2	50 Hz to 4 kHz	Trapezoid shaped tone 1
G3	1	0 dB to – 48 dB	Gain adjustment for trapezoid generator 1
FD	2	50 Hz to 4 kHz	Trapezoid shaped tone 2
GD3	1	0 dB to – 48 dB	Gain adjustment for trapezoid generator 2

2.2.5 ARCOFI® Speakerphone Support

The speakerphone option of the ARCOFI-SP PSB 2163 performs all voice switching functions without any external components, just by software. All these operational functions realized by the signal processor are completely parameterized. This technique offers a high level of flexibility and reproducibility.

There are three modes of operation: "speech mode", "listen mode", and "idle mode". In the speech mode the receive path is attenuated while in listen mode the attenuation is switched to the transmit path. In the idle mode the attenuation is halved between transmit and receive paths. The switching is mainly controlled by the speech comparators while speech activity is recognized by the speech detectors.

As the signal flow graph of the speakerphone option shows (**figure 22**), the complete operational algorithm is situated between the Analog Front End/Signal Processing and the compression/expansion logic. This has the advantage that the speakerphone function is independent of any country specific transmission characteristics. Thus telephone sets can be optimized and adjusted to the particular geometrical and acoustic environment.

The main features of the speakerphone signal processing are:

- Two separate attenuation stages activated by voice, one for the transmit and one for the receive path. They are controlled by the current and past speech activities.
- Immediate mode switching mainly controlled by two comparators, one at the acoustic side and one at the line side.
- Speech detection by special speech detectors in the respective transmit and receive directions. Different time constants are separately programmable for signal and noise.
- Background noise monitoring to eliminate continuous background noise from speech control. All time constants are user programmable.

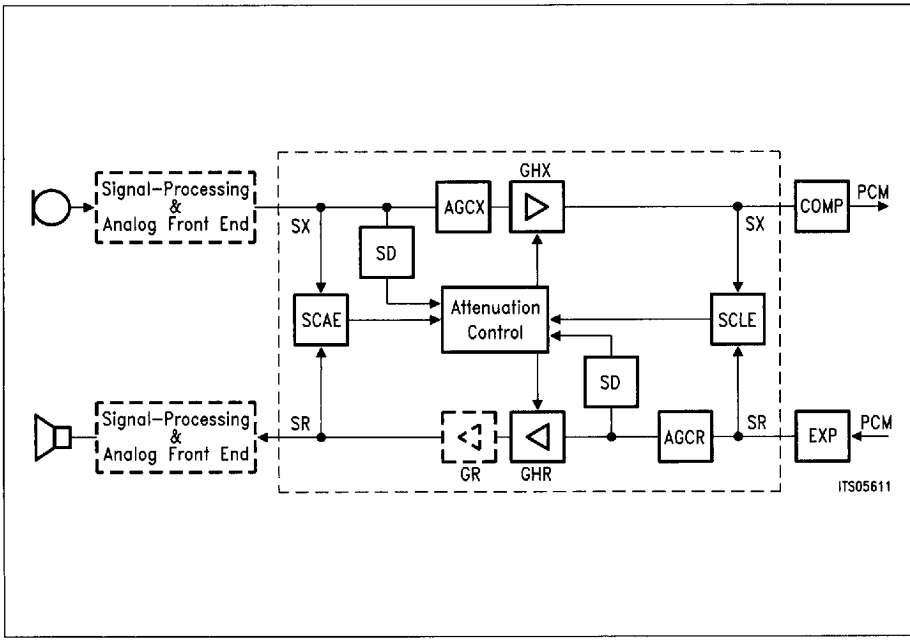


Figure 22
Speakerphone Signal Flow Graph of the ARCOFI®

2.2.5.1 Speech Detector

The speech detectors (**figure 23**) contained in both transmit and receive directions consist of two main blocks:

- Background Noise Monitor (BNM) and
- Signal Processing

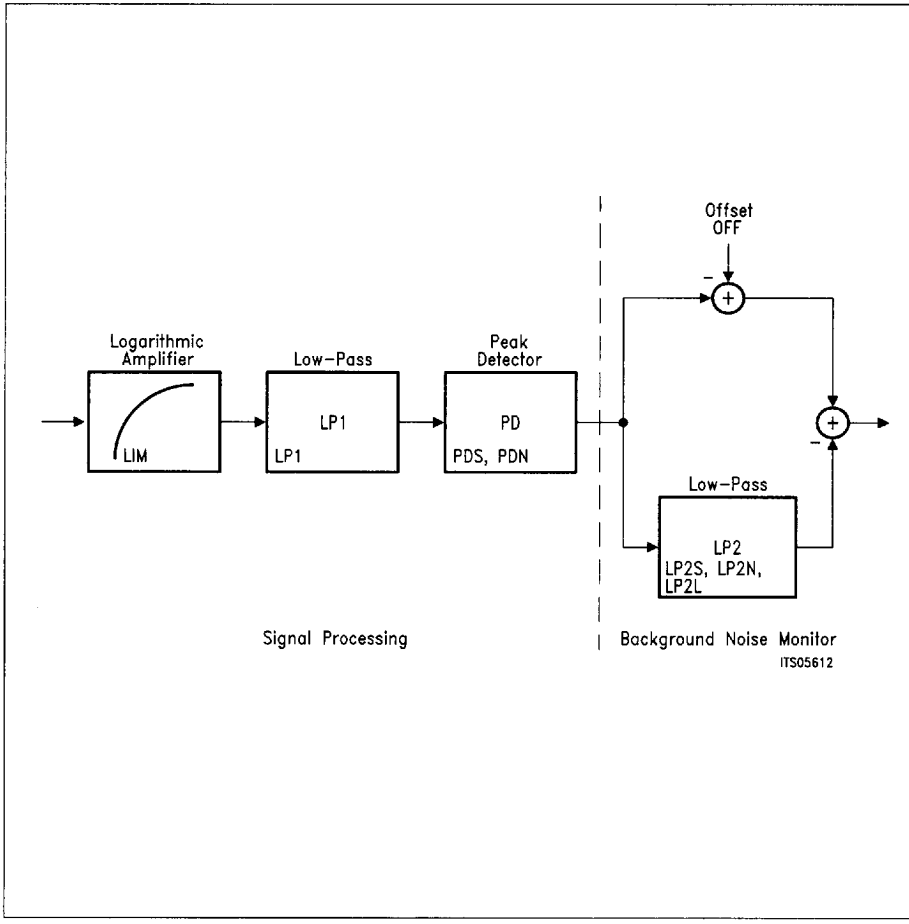


Figure 23
Speech Detector Signal Flow Graph

Background Noise Monitor

The tasks of the noise monitor are to differentiate voice signals from background noise, even if it exceeds the voice level, and to recognize voice signals without any delay. Therefore the Background Noise Monitor consists of the Low-Pass Filter 2 (LP2) and the offset in two separate branches. Basically it works on the burst-characteristic of the speech: voice signals consist of short peaks with high power (bursts). In contrast, background noise can be regarded approximately stationary from its average power.

Low-Pass Filter 2 provides different time constants for noise (non-detected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of LP2 is approximately the level of the input. Due to the offset OFF the comparator remains in the initial state. In case of speech at the comparator input the difference between the signal levels of the offset branch and of the LP2-branch increases and the comparator changes state. At speech bursts the digital signals arriving at the comparator via the offset branch change faster than those via the LP2-branch so that the comparator changes its polarity. Hence two logical levels are generated: one for speech and one for noise.

A small fade constant (LP2N) enables fast settling down the LP2 to the average noise level after the end of speech recognition. However, a too small time constant for LP2N can cause rapid charging to such a high level that after recognizing speech the danger of an unwanted switching back to noise exists. It is recommended to choose a large rising constant (LP2S) so that speech itself charges the LP2 very slowly. Generally, it is not recommended to choose an infinite LP2S because then approaching the noise level is disabled. During continuous speech or tones the LP2 will be charged until the limitation LP2L is reached. Then the value of LP2 is frozen until a break discharges the LP2. This limitation LP2L of this charging especially on the RX-path permits transmission of continuous tones and "music on hold".

The offset stage represents the exact level threshold in [dB] between the speech signal and averaged noise.

Signal Processing

As described in the preceding chapter, the Background Noise Monitor is able to discriminate between speech and noise. In very short speech pauses e.g. between two words, however, it changes immediately to non-speech, which is equal to noise. Therefore a peak detection is required in front of the Noise Monitor.

The main task of the Peak Detector is to bridge the very short speech pauses during a monolog so that this time constant has to be long. Furthermore, the speech bursts are stored so that a sure speech detection is guaranteed. But if no speech is recognized the noise low-pass LP2 must be charged rapidly to the average noise level. Additionally the noise edges are to be smoothed. Therefore two time constants are necessary and are

separately programmable: PDS for speech and PDN for space (background noise) signals.

The Peak Detector is very sensitive to spikes. The LP1 filters the incoming signal containing noise in a way that main spikes are eliminated. Due to the programmable time constant it is possible to refuse high-energy sibilants and noise edges.

To compress the speech signals in their amplitudes and to ease the detection of speech, the signals have to be companded logarithmically. Hereby, the speech detector should not be influenced by the system noise which is always present but should discriminate between speech and background noise. The limitation of the logarithmic amplifier can be programmed via the parameter LIM, where the upper half-byte features LIMX and the lower half-byte LIMR. LIM is related to the maximum PCM level. A signal exceeding the limitation defined by LIM is getting amplified logarithmically, while very smooth system noise below is neglected. It should be the level of the minimum system noise which is always existing; in the transmit path the noise generated by the telephone circuitry itself and in receive direction the level of the first bit which is stable without any speech signal at the receive path.

Description of the programmable speech detector parameters:

Parameter	# of CRAM Bytes	Range	Comment
LP1	1	1 to 512 ms	Time constant LP1
OFF	1	0 to 50 dB	Level offset up to detected noise
PDS	1	1 to 512 ms	Time constant PD (signal)
PDN	1	1 to 512 ms	Time constant PD (noise)
LP2S	1	4 to 2000 s	Time constant LP2 (signal)
LP2N	1	1 to 512 ms	Time constant LP2 (noise)
LP2L	1	0 to 95 dB	Limitation of LP2, related to LIM
LIMX, LIMR	1	– 36 to – 78 dB	Limitation of logarithmic amplifier

2.2.5.2 Speech Comparators (SC)

Switching from one active mode to another one is mainly controlled by the speech comparators. There are two Speech Comparators, one at the acoustic (AE) and one at the line side (LE). This offers a different programming of the sensitivity of the speech detectors and avoids clipping due to echoes. These comparators continuously compare the signal levels of both signal paths and control the effect of the echos at the acoustic side and the line side. Once speech activity has been detected, the comparator switches at once in that direction in which the speech signal is stronger. For this purpose each signal is compared to the sum of the other and the returned echo.

Speech Comparator at the Acoustic Side (SCAE)

In principle, the SCAE works according to the following equation:

if SX > SR + VAE then TX
else RX

Being in RX-mode, the speech comparator at the acoustic side controls the switching to TX-mode. Only if the SX-signal is higher than the SR-signal plus the expected/measured acoustic level enhancement (VAE), the comparator switches immediately to TX-mode. Physically the level enhancement (VAE) is divided into two parts: GAE and GDAE.

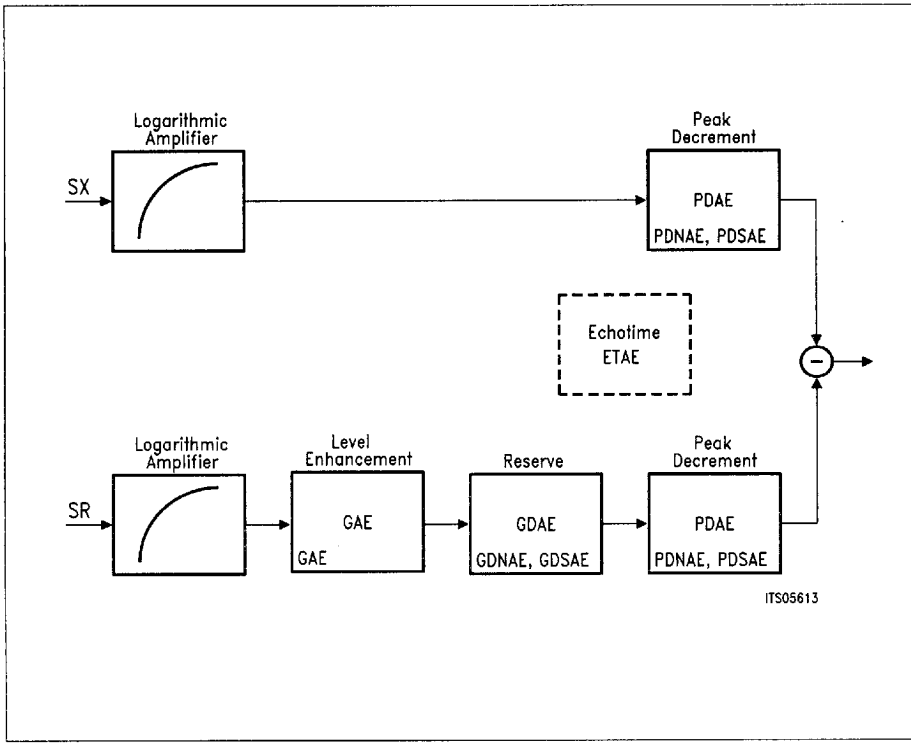


Figure 24
Speech Comparator at the Acoustic Side

At the SCAE-input, logarithmic amplifiers compress the signal range. Hence after the required signal processing for controlling the acoustic echo, pure logarithmic levels on both paths are compared.

Principally, the main task of the comparator is to control the echo. The internal coupling due to the direct sound and mechanical resonances are covered by GAE. The external coupling, mainly caused by the acoustic feedback, is controlled by GDAE/PDAE.

The Gain of the Acoustic Echo (GAE) corresponds to the terminal couplings of the complete telephone: GAE is the measured or calculated level enhancement between both receive and transmit inputs of the SCAE (**refer to figure 22**). It equals the sum of the amplification of ALS plus the gain due to the loudspeaker/microphone coupling plus the TX-amplification of AMI and GX. To succeed in a sure differentiation between original speech and echo, it must be guaranteed that the TX-signal does not run into saturation due to the loudspeaker/microphone coupling. Therefore, it is recommended to reduce the TX-gain by 10 dB in front of the SCAE at least in the loudest loudspeaker volume step. To fulfill the sending loudness rating, this gain is realized by the LGAX/ AGCX which follows the SCAE. Of course, the GAE has to be reduced by the same amount.

To control the acoustic feedback two parameters are necessary: GDAE-features the actual reserve on the measured GAE. Together with the Peak Decrement (PDAE) it simulates the echo behaviour at the acoustic side: After RX-speech has ended there is a short time during which hard couplings through the mechanics and resonances and the direct echo are present. Till the end of that time (Δt) the level enhancement VAE must be at least equal to GAE to prevent clipping caused by these internal couplings. Then, only the acoustic feedback is present. This coupling, however, is reduced by air attenuation. For this in general the longer the delay, the smaller the echo being valid. This echo behaviour is featured by the decrement PDAE.

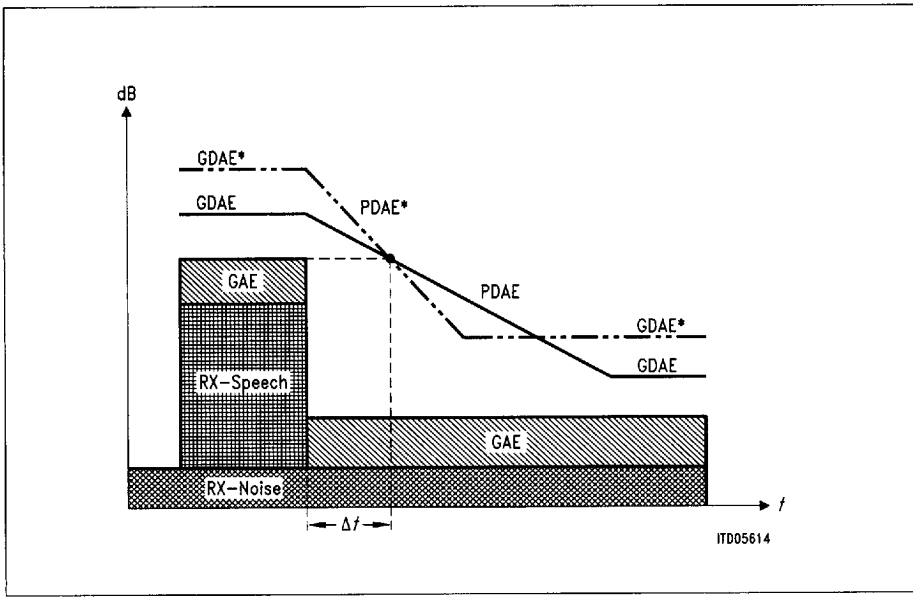


Figure 25
Interdependence of GDAE and PDAE

According to **figure 25**, a compromise between the reserve GDAE and the decrement PDAE has to be made: a smaller reserve (GDAE) above the level enhancement GAE requires a longer time to decrease (PDAE). It is easy to overshout the other side but the intercommunication is harder because after the end of the speech, the level of the estimated echo has to be exceeded. In contrary, with a higher reserve (GDAE*) it is harder to overshout continuous speech or tones, but it enables a faster intercommunication because of a stronger decrement (PDAE*).

Two pairs of coefficients, GDSAE/PDSAE when speech is detected, and GDNAE/PDNAE in case of noise, offer a different echo handling for speech and non-speech.

With speech, even if very strong resonances are present, the performance will not be worsened by the high GDSAE needed. Only when speech is detected, a high reserve prevents clipping. A time period ETAE [ms] after speech end, the parameters of the comparator are switched to the "noise" values. If both sets of the parameters are equal, ETAE has no function.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
GAE	1	– 48 to + 48 dB	Gain of Acoustic Echo
GDSAE	1	0 to 48 dB	Reserve when speech is detected
PDSAE	1	0.16 to 42 ms/dB	Peak Decrement when speech is detected
GDNAE	1	0 to 48 dB	Reserve when noise is detected
PDNAE	1	0.16 to 42 ms/dB	Peak Decrement when noise is detected
ETAE	1	0 to 1020 ms	Echo time

Speech Comparator at the Line Side (SCLE)

Principally, the SCLE works similarly to the SCAE. The formula of SCLE is the following:

$$\text{if} \quad SR > SX + VLE \text{ then RX}$$
$$\text{else TX}$$

Being in TX-mode, the speech comparator at the line side controls the switching to RX-mode. When the SR-signal is higher than the SX-signal plus the expected/measured echo return loss (VLE) and if SDR has detected speech, the comparator switches immediately to RX-mode.

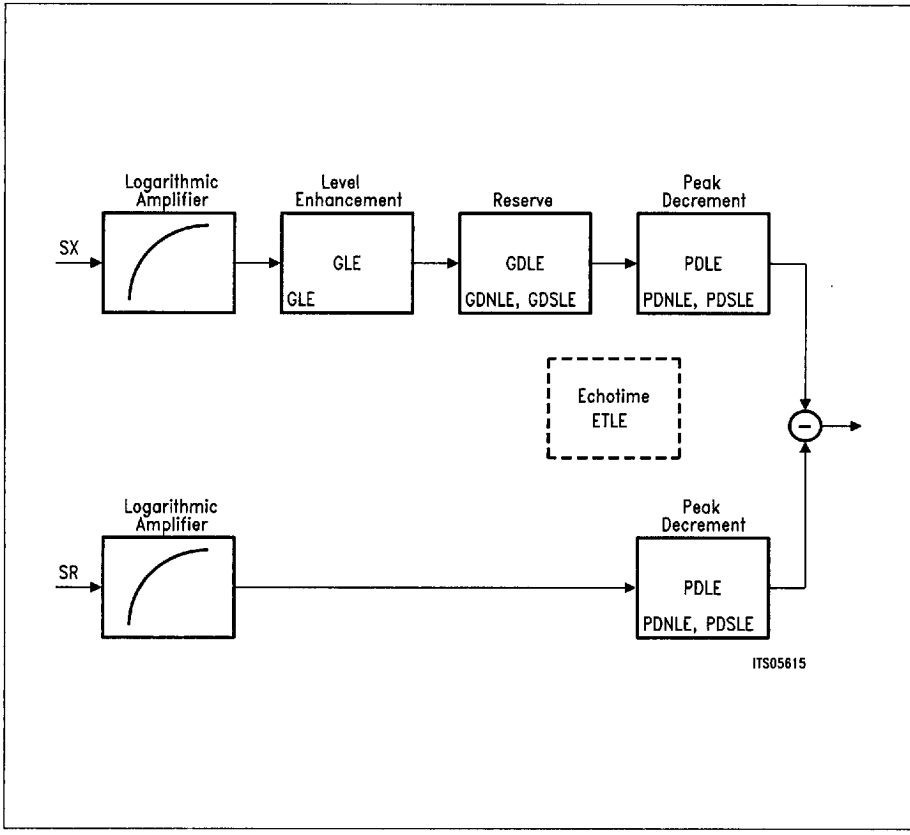


Figure 26
Speech Comparator at the Line Side

The Gain of the Line Echo (GLE) directly corresponds to the echo return loss of the link. Generally, it is specified to 27 dB. However, the worst case loss can be estimated to 10 dB. This means, the echo returns at least attenuated by 10 dB. The coefficient GLE should be programmed with an extra reserve of 2 dB so that very smooth noise is processed correctly.

Similarly to the acoustic side, GDLE at the line side features the reserve above GLE which is necessary to control the echo via the decrement PDLE. GDLE and PDLE are interdependent. Exactly Δt [ms] after the end of RX-speech the level enhancement VLE must be at least GLE to prevent clipping.

Two pairs of coefficients are available: GDSLE/PDSLE while speech is detected and GDNLE/PDNLE in case of noise. This offers the possibility to control separately the far-end echo during speech and the near-end echo while noise is detected. However, this requires an attenuation between the speech detectors SDX and SDR: If the SDX does not recognize any speech, the SDR must not detect speech due to the far-end echo. Note, that LIMX and LIMR are also influencing the sensitivity of the speech detection. ETLE [ms] after the final speech detection the parameter sets are switched. If both sets are equal, ETLE has no meaning.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
GLE	1	– 48 to + 48 dB	Gain of Line Echo
GDSLE	1	0 to 48 dB	Reserve when speech is detected
PDSLE	1	0.16 to 42 ms/dB	Peak Decrement when speech is detected
GDNLE	1	0 to 48 dB	Reserve when noise is detected
PDNLE	1	0.16 to 42 ms/dB	Peak Decrement when noise is detected
ETLE	1	0 to 1020 ms	Echo time

2.2.5.3 Attenuation Control Unit

The Attenuation Control unit controls the attenuation stages GHX of the transmit and GHR of the receive directions respectively. The programmable loss is switched either completely to a single path or, in the "IDLE" mode, is halved to each direction.

In addition, attenuation is also influenced by the Automatic Gain Control stages (AGCX and AGCR): For the total loop gain never to exceed 1, the sweep range (of ATT) is automatically enlarged with high-gain amplification of the AGCs while it will be accordingly reduced with low-gain.

Changing from one speakerphone mode into another one depends on the determinations of one comparator plus the corresponding speech detector. Hence attenuation is influenced by the current and past speech activities. Also rate of change varies: changing from "speech mode" or "listen mode" to "idle mode" is programmable by the rate factor DS. Direct changes from "speech mode" to "listen mode" or vice-versa and changes from "idle mode" to "speech mode" or "listen mode" can be programmed via the factor SW in a large range.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
TW	1	16 ms to 4 s	Wait time
ATT	1	0 dB to 95 dB	Attenuation programmed in GHR or GHX if speech activity for the other side was detected
DS	1	0.6 to 680 ms/dB	Decay Speed (Decay Time TD = DS × ATT/2)
SW	1	0.0052 to 10 ms/dB	Switching time (dependent on ATT)

2.2.5.4 Speakerphone Test Function

The ARCOFI offers a test mode to ease the optimization of the switching behaviour (TFCR.EPZST = 1). This function can also be used for signalling e.g. the speech mode during a normal telephone conversation. This mode uses the piezo pins PZ1 and PZ2.

The PZ1 pin forced to a high level indicates that neither of the speech detectors recognizes speech (refer to TW, DS, and idle state); when any speech activity is detected, this pin is at a low level. At the PZ2 pin a logical "1" indicates the speech mode (TX-mode) while a "0" signals listen mode (RX mode).

2.2.5.5 Automatic Gain Control of the Transmit Direction (AGCX)

An AGCX is inserted into the transmit path (**figure 27**) to reach nearly constant loudness ratings independent of the varying distance between the speaker and the microphone. Regulation range is between 0 dB and + 12 dB which must be enabled by setting TGSR.PM1 = 1 (Piezo-Mode).

Operation of the AGCX depends on a threshold level. Its value (via parameter COMX) corresponds to a signal level relative to the maximum PCM-value at which the microphone signal is to become amplified. Regulation follows two time constants: TMHX, which limits the signal amplitude, is shorter because the signal has to be reduced before it goes into saturation. TMLX, which amplifies the signal if it falls below the reference level, is greater because this threshold effect should hardly be perceptible.

For reasons of physiological acceptance the AGCX is automatically reduced in case of continuous background noise e.g. by ventilators. The reduction is programmed via the NOISX-parameter. When the noise level increases the threshold determined by NOISX, the amplification AGX will be reduced by the same amount the noise level is above the threshold.

A programmable Loudness Gain Adjustment stage (LGAX) offers the possibility to amplify the TX-signal after the speech comparator SCAE and the speech detector SDX. If a lower signal range in front of the SDX is necessary to determine between speech and echo a part of the TX-amplification can be transferred to the LGAX. It is enabled together with the bit GCR.SP. Even if the AGCX is disabled in speakerphone mode the LGAX remains enabled.

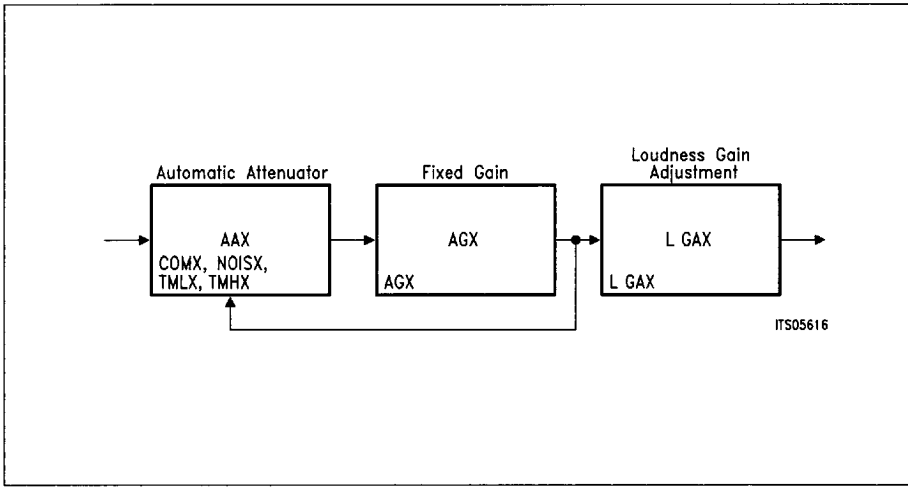


Figure 27
Function of the Transmit AGC

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
LGAX	1	– 12 to 12 dB	Loudness Gain Adjustment
COMX	1	0 to – 73 dB	Compare level rel. to max. PCM-value
AGX	1	0 to 18 dB	Gain range of Automatic control
TMLX	1	1 to 2700 ms/dB	Settling time constant for lower levels
TMHX	1	1 to 340 ms/dB	Settling time constant for higher levels
NOISX	1	0 to – 95 dB	Threshold for AGC-reduction by background noise

2.2.5.6 Automatic Gain Control of the Receive Direction (AGCR)

The Automatic Gain Control of the receive direction AGCR (**figure 28**) is similar to the transmit AGC. One additional parameter (AAR) offers an automatic amplification. The maximum attenuation is selectable with AAR. Depending on the parameters AAR and AGR three different behaviours of the AGCR are possible:

- AGR = 0: the only task of the AGCR is to prevent clipping. If the RX-signal exceeds the compare level, the AGCR starts to attenuate it.
- AGR = AAR: the AGCR works as an automatic amplifier. The RX-signal will be amplified if it is smaller than the compare level.
- |AAR| > AGR: the combination of the previous tasks: If the signal is smaller than the compare level it will be amplified while if it exceeds the level it will be attenuated. The AGCR functions like a dynamic compressor. While the digital RX-signal level varies, the volume coming out of the loudspeaker remains constant.

If the AGCR is disabled in speakerphone mode, the Loudness Gain Adjustment stage (LGAR) offers a programmable amplification in front of the SDR. It is enabled together with the bit GCR.SP. It is highly recommended to program reasonable amplifications in the digital gain stages. Otherwise the ASP will run into saturation above the 3.14 dB PCM-value.

Note that the speech detector for the receive direction is supplied with the signal that comes out of the AGR-block.

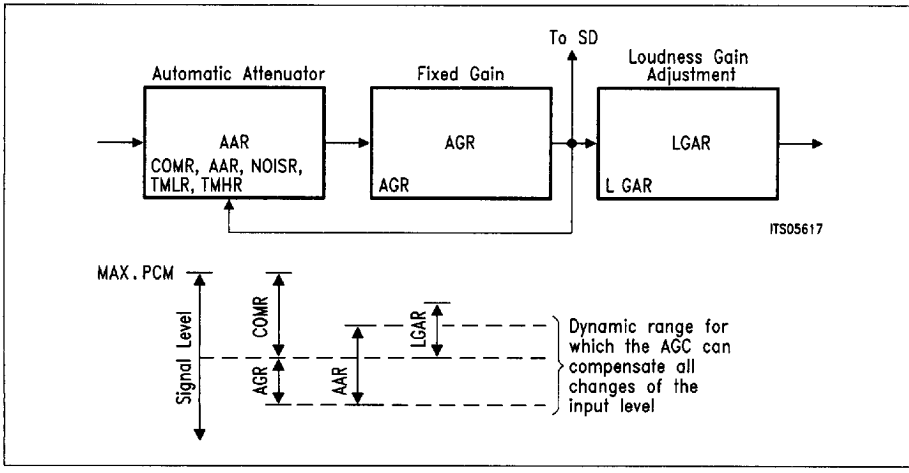


Figure 28
Function of the Receive AGC

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
LGAR	1	– 12 to 12 dB	Loudspeaker Gain Adjustment
COM	1	0 to – 73 dB	Compare level rel. to max. PCM-value
AAR	1	0 to – 47 dB	Attenuation range of Automatic control
AGR	1	0 to 18 dB	Gain range of Automatic control
TMLR	1	1 to 2700 ms/dB	Settling time constant for lower levels
TMHR	1	1 to 340 ms/dB	Settling time constant for higher levels
NOISR	1	0 to – 95 dB	Threshold for AGC-reduction by background noise

2.2.5.7 Loudhearing

The ARCOFI-SP offers the possibility to do a so called "controlled monitoring" when the bit ARCR.CME is set. This mode can only be used together with the speakerphone mode (GCR.SP) With CME = 1 the attenuation stage GHR is fixed to a value of 0 dB but the attenuation takes place in the analog loudspeaker amplifier ALS in a way that the amplification of the ALS is set to – 9.5 dB as soon as the attenuation control unit switches to transmit mode. Therefore in transmit direction the same behaviour as in speakerphone mode occurs but in the receive direction the handset output offers a signal as in normal handset mode while the volume at the loudspeaker output will be reduced to a low level during transmit mode. If the programming for the loudspeaker output (ARCR.LSC) is already chosen for values of less or equal – 9.5 dB, no further attenuation takes place.

2.2.6 Speakerphone Coefficient Set

This example shows a possible configuration for a speakerphone application. All described coefficients can be used as a basic programming set.

CMD Sequence	Coefficient	Code	Value
COP_A	GAE	$0C_H$	4.50 dB
COP_A	GLE	$E5_H$	– 10.02 dB
COP_A	ATT	40_H	24.00 dB
COP_A	ETAE	$0C_H$	48.00 ms
COP_A	ETLE	32_H	200.00 ms
COP_A	TW	09_H	144.00 ms
COP_A	DS	25_H	– 99 ms/dB
COP_A	SW	64_H	0.6 ms/dB
COP_B	GDSAE	20_H	6.02 dB
COP_B	PDSAE	06_H	7.1 ms/dB
COP_B	GDNAE	20_H	6.02 dB
COP_B	PDNAE	06_H	7.1 ms/dB
COP_B	GDSLE	40_H	12.00 dB
COP_B	PDSLE	02_H	21.3 ms/dB
COP_B	GDNLE	40_H	12.00 dB
COP_B	PDNLE	02_H	21.3 ms/dB
COP_C	LIMX, LIMR	22_H	– 48.16 dB, – 48.16 dB
COP_C	OFFX	$0C_H$	4.50 dB
COP_C	OFFR	$0C_H$	4.50 dB
COP_C	LP2LX	20_H	12 dB
COP_C	LP2LR	20_H	12 dB
COP_C	LP1X	$E1_H$	4.00 ms
COP_C	LP1R	$E1_H$	4.00 ms
COP_C	reserved 00_H		
COP_D	PDSX	26_H	102.34 ms
COP_D	PDNX	$F4_H$	32.00 ms
COP_D	LP2SX	20_H	6.55 s
COP_D	LP2NX	44_H	30.06 ms
COP_D	PDSR	26_H	102.34 ms
COP_D	PDNR	$F4_H$	32.00 ms
COP_D	LP2SR	20_H	6.55 s
COP_D	LP2NR	44_H	30.00 ms

Speakerphone Coefficient Set (cont'd)

CMD Sequence	Coefficient	Code	Value
COP_E	LGAX	01_H	9.60 dB
COP_E	COMX	$C3_H$	– 20.43 dB
COP_E	AGX	01_H	12.04 dB
COP_E	TMHX	$0A_H$	14.00 ms/dB
COP_E	TMLX	24_H	383.00 ms/dB
COP_E	NOISX	$4F_H$	– 66.23 dB
COP_E	reserved 00_H		
COP_E	reserved 00_H		
COP_F	LGAR	$F0_H$	6.04 dB
COP_F	COMR	$B2_H$	– 15.05 dB
COP_F	AAR	55_H	– 33.16 dB
COP_F	AGR	00_H	18.06 dB
COP_F	TMHR	$0A_H$	13.95 ms/dB
COP_F	TMLR	$2F_H$	500.84 ms/dB
COP_F	NOISR	$4F_H$	– 66.23 dB
COP_F	reserved 00_H		

2.3 ARCOFI® Digital Interface (ADI)

The ADI-function consists of two interface blocks:

- The Peripheral Control Interface (PCI) or the Serial Control Interface (SCI)
- The IOM-2 interface (TE- or non-TE-timing mode) or the Serial Data Interface (SDI)

Supplementary functions are accessed by strapping the pins MODE and AD according to the following table:

Pin MODE	Pin AD	Mode	Description
0	0	IOM-2 TE	IOM-2 TE-timing mode (AD = 0)
0	1	IOM-2 TE	IOM-2 TE-timing mode (AD = 1)
0	MCLK	Test	
1	0	IOM-2 non-TE	IOM-2 Non-TE-timing mode (AD = 0)
1	1	IOM-2 non-TE	IOM-2 Non-TE-timing mode (AD = 1)
1	MCLK	SDI	Serial Data Interface

A detailed description is in the following chapter.

2.3.1 PCI-Interface

The Peripheral Control Interface (PCI) provides 4 programmable I/O-pins to control the peripheral devices (for more detailed information see section 4, DFICR). These four interface pins are only available in the IOM-2 terminal mode (TE-mode).

Otherwise these pins are used as slot select pins in the IOM-2 non-TE-timing mode or used as a Serial Control Interface (SCI).

SA-SD	Mode
PCI	IOM-2 TE
Slot Select	IOM-2 Non TE
SCI	Serial Mode

2.3.2 IOM®-2 Frame Structure and Timing Modes

This interface consists of one data line per direction (DD: Data Downstream; DU: Data Upstream). Two additional signals define the data clock (DCL) and the frame synchronization (FSC).

In terminal applications, the IOM-2 constitutes a powerful backplane bus offering intercommunication and sophisticated control capabilities for peripheral modules (e.g. ARCOFI).

The channel structure of the IOM-2 is described in **figure 29**.

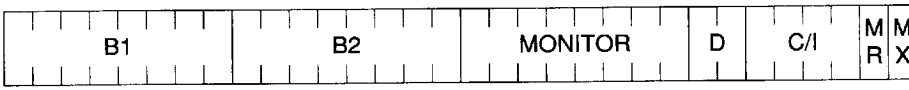


Figure 29
Channel Structure of IOM®-2

- The 64-kbit/s channels, B1 and B2, are conveyed in the first two bytes.
- The third byte (monitor channel) is used for programming and controlling devices attached to the IOM-2 interface.
- The fourth byte (control channel) contains two bits for the 16-kbit/s D-channel, four command/indication bits for controlling activation/deactivation and for additional control functions, two bits MR and MX for supporting the handling of the MONITOR channel.

In case of an IOM-2 interface the frame structure depends on whether TE- or non-TE-mode is selected.

Non-TE-Timing Mode

The frame of this mode is a multiplex of eight IOM-2 channels (**figure 30**), each channel has the structure as shown in **figure 29**.

The ARCOFI is assigned to one of eight channels (0 to 7) by strapping SB to SD according to the following table:

Pin SD	Pin SC	Pin SB	Selected IOM®-2 Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Pin SA is not used in this mode and should be connected to V_{DD} or V_{SSD}.

Thus the data rate per channel is 256 kbit/s, whereas the bit rate is 2.048 kbit/s. The IOM-2 interface signals are:

DD, DU : 2048 kbit/s
DCL : 4096 kHz (double clock rate)
FSC : 8 kHz

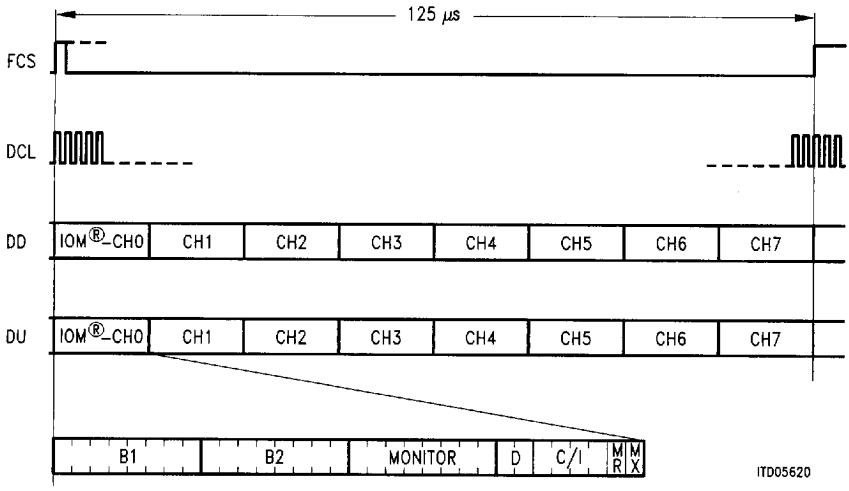


Figure 30
Multiplexed Frame Structure of the IOM®-2 Interface in Non-Terminal Timing Mode

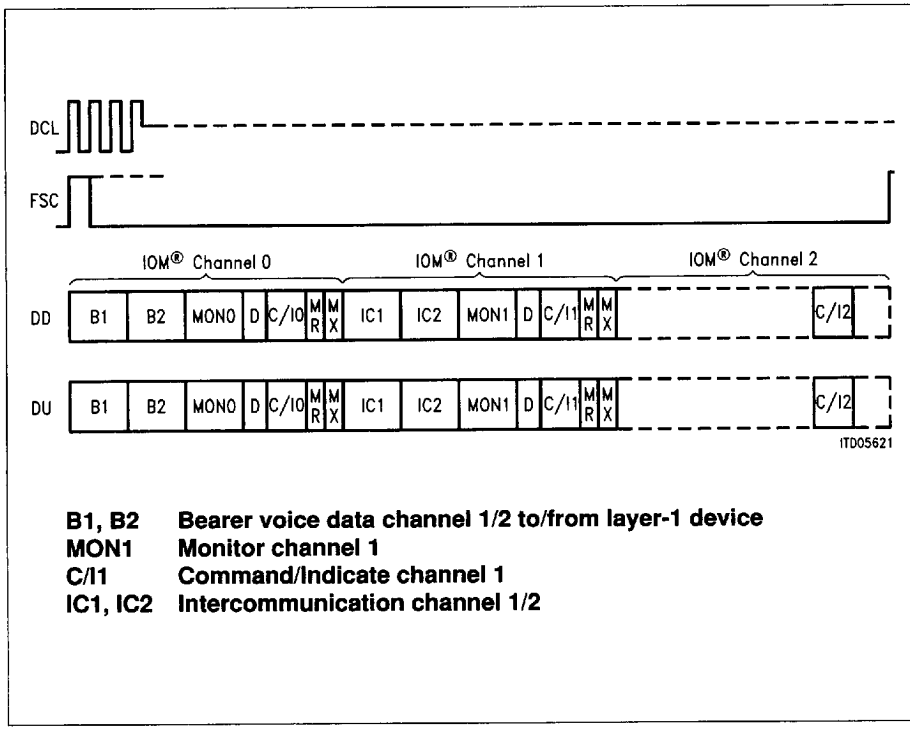
TE-Timing Mode

The IOM-2 frame provides three complete IOM channels (**figure 31**):

- Channel 0 contains 144 kbit/s (2B + D) plus monitor and command/indication channels for the layer-1 device.
- Channel 1 contains two 64-kbit/s intercommunication channels plus monitor and command/indication channels for other IOM-2 devices (e.g. ARCOFI).
- Channel 2 is used for D-channel arbitration.

The IOM-2 signals are:

DD, DU : 768 kbit/s
DCL : 1536 kHz (double clock rate)
FSC : 8 kHz



B1, B2 **Bearer voice data channel 1/2 to/from layer-1 device**
MON1 **Monitor channel 1**
C/I1 **Command/Indicate channel 1**
IC1, IC2 **Intercommunication channel 1/2**

Figure 31
IOM®-2 Interface Structure in Terminal Mode

2.3.3 Serial Control Interface

When the MODE pin is tied high and the AD/MCLK pin is used as system clock input (MCLK), the internal configuration registers and the coefficient RAM of the ARCOFI are programmable via the serial control interface. It consists of 4 lines: SCLK, SDR, SDX (open drain or push-pull) and $\overline{CS}$.

$\overline{CS}$ is used to start a serial access to the ARCOFI-registers and the coefficient RAM. Following a falling edge on $\overline{CS}$, the first eight bits transmitted on SDR specify the command. The subsequent one, two, four or eight bytes (depending on command) read(s) or write(s) the contents of the selected registers or RAM-locations until the $\overline{CS}$ line becomes inactive. If a read command is chosen, the first byte after the command is the identification code of the ARCOFI-SP PSB 2163 (**see also chapter 3.4.2.1**). After one command sequence is completed at least one NOP-command is required (**see figure 32**).

A transfer sequence can be broken by setting $\overline{CS}$ high. All bytes already sent when $\overline{CS}$ changes to high are valid.

The data transfer is synchronized by the SCLK input. SDX changes with the falling edge of SCLK while the contents of SDR is latched on the rising edge of SCLK.

Figure 32 shows the timing of a serial control interface transfer (one byte transfer).

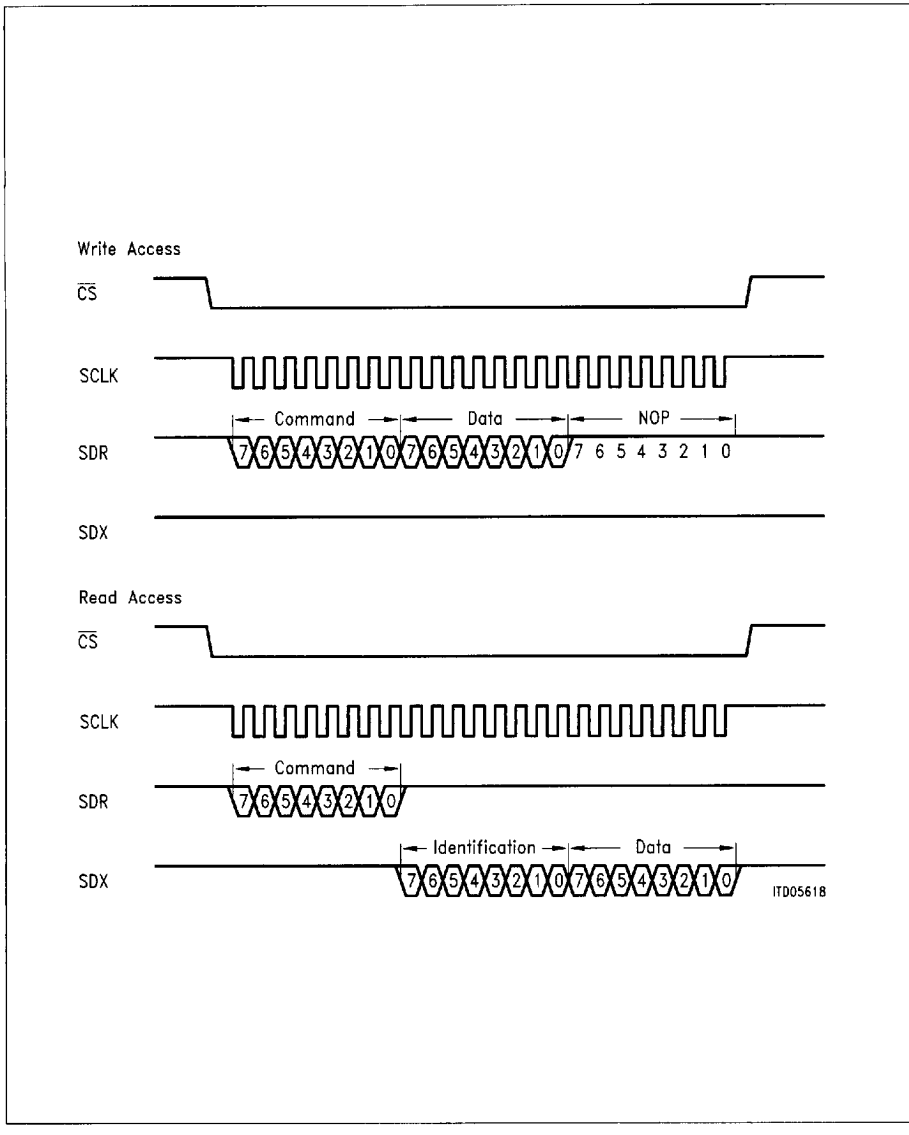


Figure 32
Serial Control Interface Timing

2.3.4 Serial Data Interface

If the serial control interface is selected, the ARCOFI supports an additional serial data interface for B-channel transfer. This control interface consists of five lines: FSC, DCLK, DX, DR and MCLK.

FSC is a 8-kHz frame synchronization signal.

The DCLK is the clock signal to synchronize the data transfer on both data lines DX and DR. The rising edge indicates the start of the bit while the falling edge is used to latch the contents of the received data line DR. If the double clock rate is chosen (twice of the transmission rate) the first rising edge indicates the start of a bit while the second falling edge is used to latch the content of the data line.

The data rate of the interface can vary from 64 kbit/s to 4.096 Mbit/s. A frame may consist of up to 64 time-slots of 8 bits each. The last 6 bits of TSCR (Time Slot Configuration Register) indicate the selected time-slot from 0 to 63. If a 16-bit mode (linear mode) is chosen, the lowest data rate is 128 kbit/s and the time-slot must be set to an even number.

The pin AD/MCLK is a system clock synchronized with FSC (necessary to synchronize internal PLL).

Figure 33 shows the timing of a serial data interface (256 kbit/s with single clock rate).

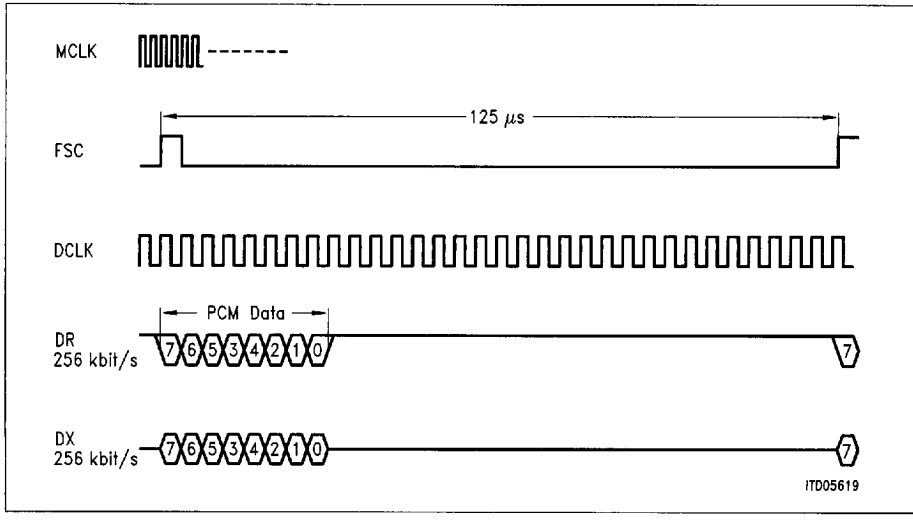


Figure 33
Serial Data Interface Timing

2.4 Test Functions

The ARCOFI provides several test and diagnostic functions which can be grouped as follows:

- All programmable configuration registers and coefficient RAM-locations are readable
- Digital loop via PCM-register (DLP)
- Digital loop via signal processor (DLS)
- Digital loop via noise shaper (DLN)
- Analog loop via analog front end (ALF)
- Analog loop via converter (ALC)
- Analog loop via noise shaper (ALN)
- Analog loop via Z-sidetone (ALZ); sidetone gain stage GZ must be enabled (PFCR.GZ = 1) and sidetone gain must be programmed with 0 dB; depending on the VDM-bit setting (DFICR) an addition to the incoming voice signal is possible
- Analog loop via digital interface (ALI).

3 Operational Description

3.1 Reset

After a RESET (internal power-on reset, hardware reset at pin RS or software reset via XOP_E) the pins SA to SD are programmed as inputs. All other output pins are in high-impedance state (HOP/HON, LSP/LSN, V_{REF}, PZ1, PZ2, DU/DX).

Note: After a Reset (only TE and Non-TE mode) the coefficient RAM-locations have defined reset values.

The defined reset values of the ARCOFI-registers are listed below:

Register	Value after RESET [hex]	Meaning
CMDR	BF	– No operation (NOP)
GCR	00	– Speakerphone disabled (incl. AGCX and AGCR) – Disable voice transmit – IOM-2 channel 0 selected (IOM-2 TE-mode) – Power-down mode – IOM-2 two chip mode (IOM-2 TE-mode) – A-Law
DFICR	F0	– SA to SD programmed as inputs – PCM-mode; receive voice blocked
PFCR	00	– Programmable digital gain disabled – Programmable sidetone gain disabled – Correction filters disabled – 50-Hz receive HP active – 50-Hz transmit HP active
TGCR	00	– Tone generator inactive – Control generator inactive
TGSR	00	– No tone generator connection to any signal path
ATCR	00	– Microphone amplifier is in power-down mode – Reference voltage buffer is in power-down mode – Pins MIP1/MIN1 are directed to the microphone amplifier AMI
ARCR	00	– Earpiece amplifier AHO is in power-down mode – Loudspeaker amplifier ALS is in power-down mode
TFCR	00	– IOM-2 handshake procedure enabled – No internal speakerphone status signals are directed to PZ1/PZ2 – Analog test mode disabled – Digital test mode disabled

Defined reset values of the ARCOFI-registers (cont'd)

Register	Value after RESET [hex]	Meaning
SDICR	00	– Single clock rate (DCLK) is enabled – DX and SDX are configured as open drain outputs – Master clock rate is 512 kHz
TSCR	00	– Time-slot 0 (SDI) is selected
XCR	00	– AHO and ALS are in the differential mode
CRAM	00	– All locations (TE and Non-TE)

3.2 Initialization

During initialization a subset of configuration registers and coefficient RAM-locations has to be programmed to set the configuration parameters according to the application and desired features.

Configuration Registers:

Register	Bit	Effect	Restricted to
GCR	SP	Speakerphone ON/OFF	
	AGCX	TX-automatic gain control (only if GCR.SP = 1)	
	AGCR	RX-automatic gain control (only if GCR.SP = 1)	
	EVX	Enable voice transmit	
	SLOT	IOM-2 slot select	IOM-2 TE
	PU	Power-up/down mode	
	CAM	IOM-2 address mode	IOM-2
	LAW	A-Law/μ-Law	
DFICR	SA-SD	PCI-port configuration	IOM-2 TE
	VDM	Voice data manipulation	
PFCR	GX	TX digital gain	
	GR	RX digital gain	
	GZ	Sidetone gain	
	FX	TX-frequency correction filter	
	FR	RX-frequency correction filter	
	DHPR	Disable high-pass (50 Hz) receive	
	DHPX	Disable high-pass (50 Hz) transmit	
TGCR	TG	Tone generator	
	DT	Dual tone mode	
	ETF	Enable tone filter	
	CG	Control generator	
	BT	Beat tone generator	
	BM	Beat mode	
	SM	Stop mode	

Configuration Registers (cont'd)

Register	Bit	Effect	Restricted to
	SQTR	Square/trapezoid shaped signal	
TGSR	PM	Piezo mode	
	TRL	Tone ringing via loudspeaker	
	TRR	Tone ringing in receive direction	
	DTMF	DTMF-signal in transmit direction	
	TRX	Tone ringing in transmit direction	
ATCR	MIC	Microphone amplifier control	
	EVREF	Enable 2.4 V reference voltage at pin V_{REF}	
	AIMX	Analog input multiplexer	
ARCR	HOC	Handset amplifier control	
	CME	Controlled monitoring	
	LSC	Loudspeaker amplifier control	
TFCR	DHS	Disable IOM-2 handshake procedure	IOM-2
	EPZST	PZ1/PZ2 as speakerphone status output	
	ALTF	Analog Loops and test functions	
	DLTF	Digital Loops and test functions	
SDICR	EPP0	Enable push/pull (DX)	SDI
	EPP1	Enable push/pull (SDX)	SDI
	DCE	Double clock enable	SDI
TSCR	MCLKR	Master clock rate	SDI
XCR	TS	Time slot select	SDI
	DHOP	Disable HOP (tristate)	
	DHON	Disable HON (tristate)	
	DLSP	Disable LSP (tristate)	
	DLSN	Disable LSN (tristate)	

Note: Before accessing the ARCOFI PCI (IOM-2 TE-mode) interface, a GCR-write command (SOP_0 or SOP_F) has to be sent.

Coefficient RAM-locations:

Mnemonic	# of Bytes	Effect
COP_0: Tone generator parameter set 1		
F1	2	Tone generator frequency
G1	1	Tone generator amplitude
GD1	1	Trapezoid generator amplitude
T1	2	Beat tone time
	2	not used

Coefficient RAM-locations (cont'd)

Mnemonic	# of Bytes	Effect
COP_1: Tone generator parameter set 2; tone generator level adjustment		
F2	2	Tone generator frequency
G2	1	Tone generator amplitude
GD2	1	Trapezoid generator amplitude
T2	2	Beat tone time span
GTR	1	Level adjustment for receive path
GTX	1	Level adjustment for transmit path
COP_2: Tone generator parameter set 3; Parameter set for the DTMF-generator (TGSR.DTMF = 1)		
F3	2	Tone generator frequency
G3	1	Tone generator amplitude
GD3	1	Trapezoid generator amplitude
T3	2	Beat tone time span
FD	2	Dual tone frequency
COP_3: Tone filter		
K	1	Attenuation of the stop-band
A1	1	Center frequency
A2	1	Bandwidth
GE	1	Saturation amplification
COP_4: Control generator		
TON	2	Turn-on period of the tone generator
TOFF	2	Turn-off period of the tone generator
COP_5: Receive and transmit gain		
GX	2	Transmit gain
GR	2	Receive gain
	4	Not used
COP_6: Sidetone gain		
GZ	2	Sidetone gain
	2	not used
COP_7/COP_8: Transmit correction filter		
FX	12	Transmit correction filter coefficients

Coefficient RAM-locations (cont'd)

Mnemonic	# of Bytes	Effect
COP_8/COP_9: Receive correction filter		
FR	12	Receive correction filter coefficients
COP_A: Parameter set for transmit and receive speech comparator Parameter set for speakerphone control unit		
GAE	1	Gain of acoustic echo
GLE	1	Gain of line echo
ATT	1	Attenuation programmed in GHR or GHX
ETAE	1	Echo time (acoustic side)
ETLE	1	Echo time (line side)
TW	1	Wait time
DS	1	Decay speed
SW	1	Switching time
COP_B: Parameter set for transmit and receive speech comparator		
GDSAE	1	Reserve when speech is detected (acoustic side)
PDSAE	1	Peak decrement when speech is detected (acoustic side)
GDNAE	1	Reserve when noise is detected (acoustic side)
PDNAE	1	Peak decrement when noise is detected (acoustic side)
GDSLE	1	Reserve when speech is detected (line side)
PDSLE	1	Peak decrement when speech is detected (line side)
GDNLE	1	Reserve when noise is detected (line side)
PDNLE	1	Peak decrement when noise is detected (line side)
COP_C: Parameter set for transmit and receive speech detector		
LIM	1	Starting level of the logarithmic amplifiers
OFFX	1	Level offset up to detected noise (transmit)
OFFR	1	Level offset up to detected noise (receive)
LP2LX	1	Limitation for LP2 (transmit)
LP2LR	1	Limitation for LP2 (receive)
LP1X	1	Time constant LP1 (transmit)
LP1R	1	Time constant LP1 (receive)
	1	not used

Coefficient RAM-locations (cont'd)

Mnemonic	# of Bytes	Effect
COP_D: Parameter set for receive and transmit speech detector		
PDSX	1	Time constant PD for signal (transmit)
PDNX	1	Time constant PD for noise (transmit)
LP2SX	1	Time constant LP2 for signal (transmit)
LP2NX	1	Time constant LP2 for noise (transmit)
PDSR	1	Time constant PD for signal (receive)
PDNR	1	Time constant PD for noise (receive)
LP2SR	1	Time constant LP2 for signal (receive)
LP2NR	1	Time constant LP2 for noise (receive)
COP_E: Parameter set for transmit AGC		
LGAX	1	Loudness gain adjustment
COMX	1	Compare level rel. to max. PCM-value
AGX	1	Gain range of automatic control
TMHX	1	Settling time constant for lower levels
TMLX	1	Settling time constant for higher levels
NOISX	1	Threshold for AGC-reduction by background noise
	1	not used
	1	not used
COP_F: Parameter set for receive AGC		
LGAR	1	Loudness gain adjustment
COMR	1	Compare level rel. to max. PCM-value
AAR	1	Attenuation range of automatic control
AGR	1	Gain range of automatic control
TIMHR	1	Settling time constant for lower levels
TIMLR	1	Settling time constant for higher levels
NOISR	1	Threshold for AGC-reduction by background noise
	1	not used

3.3 ARCOFI® Operating Modes

The most currently used ARCOFI-operating modes are documented in the following table. The 12 ARCOFI-configuration registers have enough build-in flexibility to accommodate an extensive set of user calling procedures.

The following operating mode description table is not exhaustive but should be used as an example of possible functions performed by the ARCOFI.

State	Description
POR	Power-on reset: when power is supplied to the ARCOFI an internal power-on reset is generated. In addition a hardware reset via an RC-network connected to input pin RS will force all ARCOFI internal registers to default values. The ARCOFI-registers reset state is described in section 3.1 and 4.
STAND BY	The system microprocessor can initialize the ARCOFI via the IOM-2 or the SCI-bus with a different set of filter and configuration values. Whilst remaining in power-down (GCR.PU = 0) a new set of filter coefficients and configuration bits can be loaded in the ARCOFI.
HANDSET	The system MPU detects activity from the hookswitch or from the keyboard. The ARCOFI can be placed in HANDSET state where all handset I/O are enabled (AMI & AHO activated).
RINGING	The system MPU detects an incoming call, the ARCOFI can be placed in a RINGING state by activating the tone ringer via TGCR/TGSR and configuring the ARCOFI such that either the LSP/LSN-output or the piezo output (pins PZ1/PZ2) are enabled. An emergency ringing is also implemented. In this mode, only the tone ringer and the loudspeaker amplifier are active (AMI- and AHO-amplifier are disabled by the user). The tone ringer signal is directly switched to the loudspeaker amplifier ALS.
DTMF	All audio inputs can be disabled by forcing the AMI-amplifier (ATCR) to power-down. DTMF tones are generated with the tone generator and are output to the transmit path.
PULSE DIAL	Handset audio path can be enabled by forcing a HANDSET mode. A single tone can be superimposed into the audio receive path so as to provide audible feedback when dialling.
LOUD HEARING (MONITORING)	The handset I/O and the loudspeaker outputs LSP/LSN are active (ATCR & ARCR).

Operating mode description table (cont'd)

State	Description
SPEAKERPHONE	The handset audio I/O's are disabled. The hands-free microphone input and loudspeaker outputs LSP/LSN are activated by configuring ATCR & ARCR. The ARCOFI must be set to the speakerphone mode (GCR.SP = 1).
MUTE	The ARCOFI can be placed in a MUTE state by powering down the AMI. In handset mode the outputs HOP/HON remain enabled while in speakerphone mode the outputs LSP/LSN are enabled. All other analog I/O's being disabled.
FEATURE TONE	A single tone can be superimposed to the incoming PCM-voice signal. Applications requiring system function audible feedback are therefore made possible.

3.4 IOM®-2 Interface Protocol

The following description of the IOM-2 interface comprises all ARCOFI relevant functions in the terminal and non-terminal mode (see IOM-2 interface specification for general information).

Note: Channels IC1 & IC2 are only available in the IOM-2 TE-mode. MON-channel means MON1-channel in the IOM-2 TE-mode.

3.4.1 B- and IC-Channels

The ARCOFI can receive and transmit voice data in the IOM-2 B1- & B2-channels as well as in the IC1- & IC2-intercommunication channels located in IOM-2 channels 0 and 1 respectively. The voice/data channel allocation is programmable via the ARCOFI-channel select bit SLOT in the GCR-register. B1 or B2 or respectively IC1 or IC2 can be programmed by use of the RCM-bit in the CMDR-register.

The IC1- and IC2-intercommunication channels can be used in the terminal for local data communication (e.g. answering machine). This makes post-processing of voice/data information possible (e.g. data encryption).

3.4.2 Monitor Channel

All programming data required by the ARCOFI including coefficients are transmitted exclusively in the MON-time-slot of the IOM-2 channel. The MON-channel allows a point to multi-point access where the layer-2 component acts as the master to program devices like the ARCOFI. Each programmable device is accessed by sending a specific address byte at the start of each SOP- or COP-command stream. Before executing a command, the programmable device compares the received address byte with its own address. The latter consists of 8 bits whose 4th MSB-bit must correspond to the AD-wire (AD/MCLK pin) strapped IOM-2 address.

3.4.2.1 MON-Channel Data Structure

The data to control and program the ARCOFI are transferred in the MON1-channel via the IOM-2 interface by a procedure utilizing read/write registers in the ARCOFI.

The messages transmitted in the monitor channel may have different kinds of data structures. Therefore, the first byte of the message is used to indicate the data structure (first four bits).

Identification Command

In order to be able to identify unambiguously different devices by software, the following identification command is used:

DD 1st byte value	1	0	1	X	0	0	0	0
DD 2nd byte value	0	0	0	0	0	0	0	0

The ARCOFI responds to this DD-identification sequence by sending a DU identification sequence:

DU 1st byte value	1	0	1	X	0	0	0	0
DU 2nd byte value	1	0	DESIGN					

X: logical 0 (active low): AD = 0 (A-chip)
logical 1 (passive high): AD = 1 (B-chip)

DESIGN: six bit code, specific for each device in order to identify differences in operation

e.g.	000000	ARCOFI	PSB 2160
	000010	ARCOFI-SP	PSB 2165
	000100	ARCOFI-SP	PSB 2163

This identification sequence is usually done once, when the terminal is connected for the first time.This function is used so that the software can distinguish between different possible hardware configurations. However this sequence is not compulsory.

Programming Sequence

An ARCOFI-programming sequence is characterized by a "1" being sent in the LSB-nibble of the first incoming identification code.

DD 1st byte value	1	0	1	X	0	0	0	1
DD 2nd byte value	COP_X, SOP_X, XOP_X							

All programmed configurations and coefficients can be read back when issuing an appropriate CMDR read (CMDR.R/W = 1). The ARCOFI responds by sending an IOM-2 specific address byte identifying the chip followed by the requested data.

3.4.2.2 MON-Transfer Protocol

The transfer of a stream of commands in the MON-channel is regulated by a handshake protocol mechanism implemented by two bits MX and MR in the fourth slot of the IOM-2 channel. The procedure is as follows (**figure 34**):

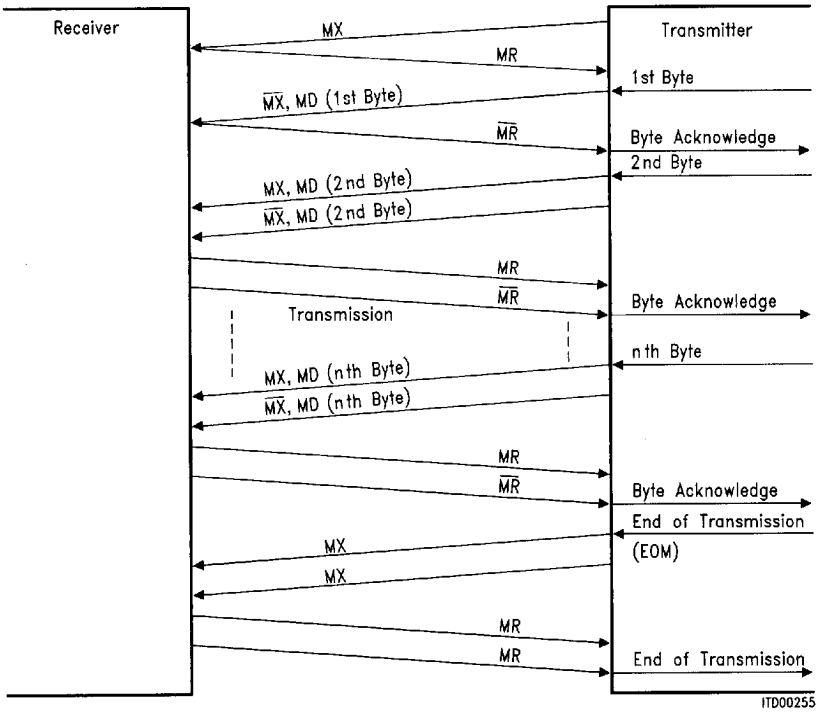


Figure 34
Monitor Channel Handshake Procedure

Monitor transfer protocol rules:

- A pair of MX and MR in the inactive state for two or more consecutive frames indicates an idle state or an end of transmission (EOM).
- A command stream initiated by a transmitter in the MON-slot is accompanied by an activated downstream MX-bit.
- The receiver acknowledges a received byte by toggling the upstream MR-bit from inactive to active in the subsequent IOM-2 frame for at least one frame.
- The transmitter indicates a new byte in the MON-slot by the transition of the MX-bit from the active to the inactive state. The MX-bit returns to the active state after one frame. Two frames with the MX-bit in the inactive state indicate the end of transmission.
- The receiver acknowledges each new byte by a similar one frame transition of the MR-bit to the inactive state. Two frames with the MR-bit set to inactive indicate a receiver request for abort.
- The transmitter can delay a transmission sequence by sending the same byte continuously. In that case the MX-bit remains active in the IOM-2 frame following the first byte occurrence.
- Delaying a transmission sequence is only possible while the receiver MR-bit and the transmitter MX-bit are active.
- Since the receiver is able to receive the MON-slot data at least twice (in two consecutive frames), the receiver waits for the reception of two successive identical bytes.
- To control this handshake procedure a collision detection mechanism is implemented in the transmitter. This is done by making a collision check per bit on the transmitted MON-data.

3.4.2.3 Implementation of the MON-Channel Protocol

The MON-receiver has the following features:

- Transparent interface between IOM-2 interface and any device internal block (sink) with respect to handshake procedure, i.e. any acknowledge, EOM, abort or request for abort is conveyed transparently through the receiver.

Figure 35 shows the state diagram of the MON-receiver. The following signals are used:

MR: MR-bit sent by the receiver
MX: MX-bit received
LL: Last two bytes were identical

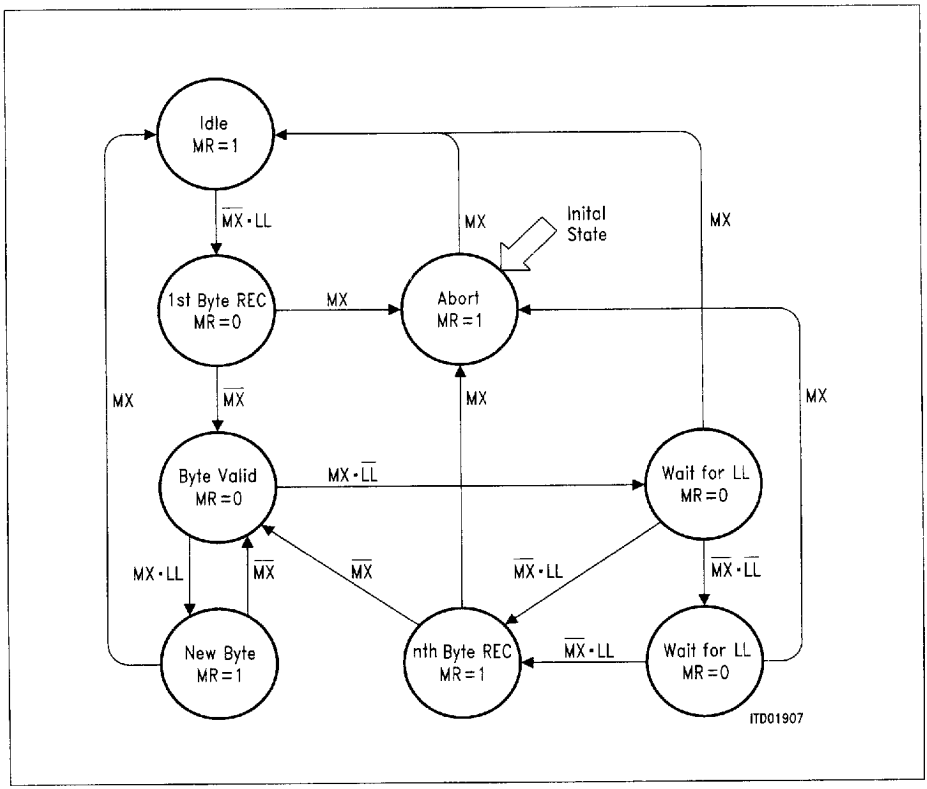


Figure 35
State Diagram of the Monitor Receiver

The MON-transmitter has the following features:

- Transparent interface between IOM-2 interface and any device internal block (source) with respect to handshake procedure, i.e. any acknowledge, abort, request for abort is conveyed transparently through the transmitter.

Figure 36 shows the state diagram of the MON-transmitter. The following signals are used:

MR: MR-bit received
MX: MX-bit transmitted
LL: Last two bytes were identical
RQT: Request transmission
EOM: End of transmission

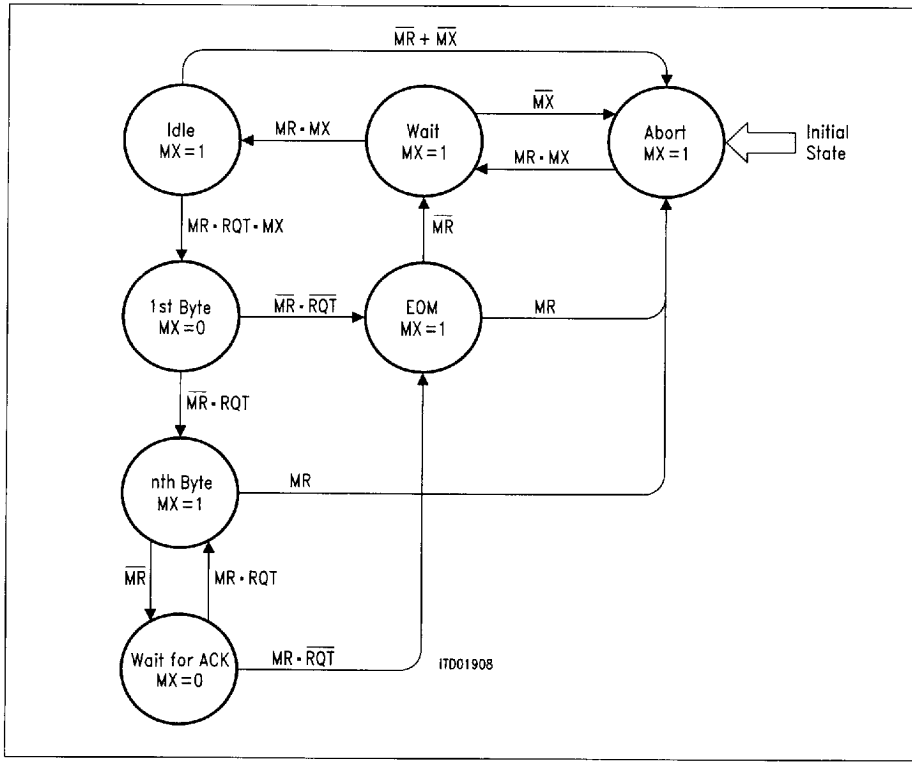


Figure 36
State Diagram of the Monitor Transmitter

3.4.3 Command/Indication Channel 1 (TE-mode)

The C/I-channel bits are represented so that the first bit transmitted/received appears on the left. The data presented to the four peripheral control interface (PCI) pins SA to SD are transparently routed to the C/I IOM-2 channel 1. Pins SA to SD can be configured individually as input or output and the information sent to the pins SA to SD or coming from them will appear respectively in the DD or DU C/I IOM-2 channel 1.

In case a reset has been asserted, the SA- to SD-pins are programmed as input, however the SA- to SD-values are not switched to the DU C/I1-channel unless a write command (except NOP) is issued.

The mapping of the peripheral control interface (PCI) pins SA to SD into the six C/I1-channel bits depends on the hardwired AD-address (see section 3.7) as follows.

AD = 1

	7					2	1	0
DD and DU	–	–	SB	SA	SD	SC	MR	MX

AD = 0 (GCR.CAM = 0; two chip mode)

DD and DU	SD	SC	–	–	–	–	MR	MX

AD = 0 (GCR.CAM = 1; one chip mode)

DD and DU	SD	SC	SB	SA	–	–	MR	MX

C/I1-Channel (Signaling) Bit Allocation Table:

CAM	AD	DD-C/I1						DU-C/I1						PCI-Configuration
		7	6	5	4	3	2	7	6	5	4	3	2	
X	X	X	X	X	X	X	X	H	H	H	H	H	H	after reset
								S	S					
0	0	X	X	X	X	X	X	D	C	H	H	H	H	PCI-pins as inputs
		S	S											
0	0	D	C	X	X	X	X	H	H	H	H	H	H	PCI-pins as outputs
		S							S					
0	0	D	X	X	X	X	X	H	C	H	H	H	H	PCI-pin SC as input PCI-pin SD as output
			S					S						
0	0	X	C	X	X	X	X	D	H	H	H	H	H	PCI-pin SD as input PCI-pin SC as output
										S	S	S	S	
X	1	X	X	X	X	X	X	H	H	B	A	D	C	PCI-pins as inputs
				S	S	S	S							
X	1	X	X	B	A	D	C	H	H	H	H	H	H	PCI-pins as outputs
					S		S			S		S		
X	1	X	X	X	A	X	C	H	H	B	H	D	H	SB and SD as inputs SA and SC as outputs
				S		S					S		S	
X	1	X	X	B	X	D	X	H	H	H	A	H	C	SA and SC as inputs SB and SD as outputs
								S	S	S	S			
1	0	X	X	X	X	X	X	D	C	B	A	H	H	PCI-pins as inputs
		S	S	S	S									
1	0	D	C	B	A	X	X	H	H	H	H	H	H	PCI-pins as outputs
		S		S					S		S			
1	0	D	X	B	X	X	X	H	C	H	A	H	H	SA and SC as inputs SB and SD as outputs
			S		S			S		S				
1	0	X	C	X	A	X	X	D	H	B	H	H	H	SB and SD as inputs SA and SC as outputs

X: don't care
H: passive high

3.5 ARCOFI® Voice/Data Manipulation (VDM)

The ARCOFI offers several possibilities of voice/data manipulation for special applications.

According to the manipulation mode chosen, the byte B1 or B2 (or IC1 or IC2 in the IOM-2 TE-mode) can be output via the handset channel and/or the loudspeaker channel.

The following tables gives an overview of the different voice/data manipulation modes.

- **PCM-mode or normal mode (DFICR.VDM = 000X):**

DFICR.VDM	AD Pin (IOM-2) [1]	CMDR.RCM (IOM-2)	GCR.SLOT (IOM-2)	Receive Channel	Transmit Channel
0000	0	0	0	–	B1
	0	0	1	–	IC1
	0	1	0	–	B2
	0	1	1	–	IC2
	1	0	0	–	B2
	1	0	1	–	IC2
	1	1	0	–	B1
	1	1	1	–	IC1
0001	0	0	0	B1	B1
	0	0	1	IC1	IC1
	0	1	0	B2	B2
	0	1	1	IC2	IC2
	1	0	0	B2	B2
	1	0	1	IC2	IC2
	1	1	0	B1	B1
	1	1	1	IC1	IC1

- **Linear mode (DFICR.VDM = 010X):**

This mode exists only in the SDI mode (in the programmed and the following channel) or in the IOM-2 one chip mode (GCR.CAM = 1). The two voice/data channels B1 and B2 (or IC1 and IC2 in the IOM-2 TE-mode) are connected to one 16-bit linear channel (2s complement).

DFICR.VDM	AD Pin (IOM-2)	CMDR.RCM (IOM-2)	GCR.SLOT (IOM-2)	Receive Channel	Transmit Channel
0100	–	–	0	–	B1 & B2
	–	–	1	–	IC1 & IC2
0101	–	–	0	B1 & B2	B1 & B2
	–	–	1	IC1 & IC2	IC1 & IC2

[1] This table is given for the IOM-2 two chip mode (GCR.CAM = 0).

B1&B2 (IC1&IC2) means B1 (IC1) byte followed by B2 (IC2) byte (totally 16 bits).

- **Three party conferencing (DFICR.VDM = 100X):**

This mode is available only in the SDI-mode (in the programmed and the following channel) or in the IOM-2 one chip mode (GCR.CAM = 1).

DFICR.VDM	AD Pin (IOM-2)	CMDR.RCM (IOM-2)	GCR.SLOT (IOM-2)	Receive Channel	Transmit Channel
1000	–	–	0	B1 + B2	B1, B2
	–	–	1	IC1 + IC2	IC1, IC2

B1 + B2 (IC1 + IC2) means the B1 (IC1) and the B2 (IC2) byte are added together (on 8 bits).
B1, B2 (IC1, IC2) means B1 (IC1) and B2 (IC2) byte have the same information.

- **Voice monitoring mode (DFICR.VDM = 1100):**

This mode is available only in the SDI-mode or in the IOM-2 one chip mode (GCR.CAM = 1). The monitoring chip and the transmission chip must be strapped to a different hardware address (IOM-2: AD/MCLK pin).

The active DU-voice channel of the monitoring chip must be set in the Hi Z-mode (GCR.EVX = 0).

The PCI-port of both chips must be set in the compatible configurations to avoid collision problems in the DU-C/I1 channel.

DFICR.VDM	AD Pin (IOM-2)	CMDR.RCM (IOM-2)	GCR.SLOT (IOM-2)	Receive Channel	Transmit Channel
1100	1/0	0	0	B1D + B1U	B1
	1/0	0	1	IC1D + IC1U	IC1
	1/0	1	0	B2D + B2U	B2
	1/0	1	1	IC2D + IC2U	IC2

Explanations:

–	no signal
B1/B2	voice channels
IC1/IC2	IOM-2 intercommunication channels
B1D/B2D	IOM-2 voice channels (downstream)
B1U/B2U	IOM-2 voice channels (upstream)
IC1D/IC2D	IOM-2 intercommunication channels (downstream)
IC1U/IC2U	IOM-2 intercommunication channels (upstream)

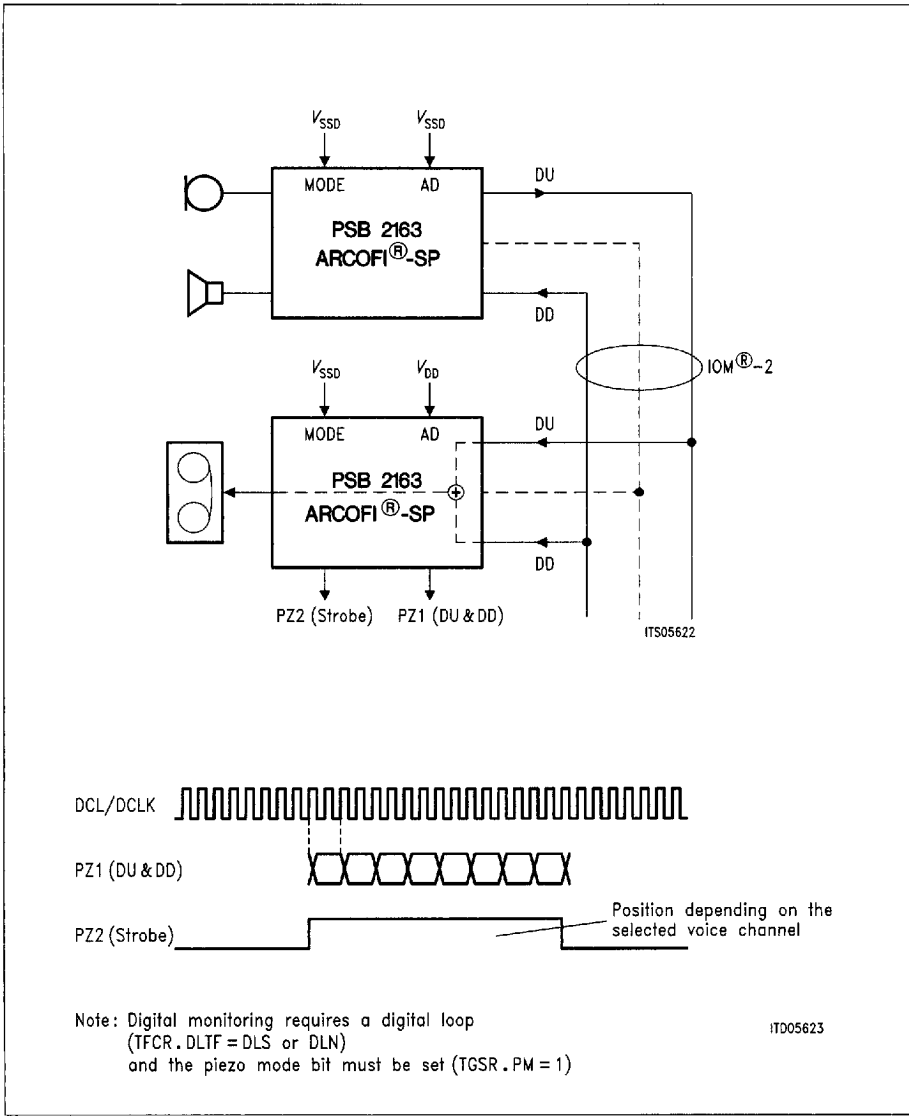


Figure 37
Configuration of the IOM®-2 TE-Monitoring Mode

4 Detailed Register Description

The following section describes the various ARCOFI-registers and coefficient RAM-locations accessible from the terminal equipment microcontroller via the IOM-2 bus or via the serial controller interface (SCI).

A summary of the 12 registers located in the ADI-block is presented below followed by a detailed description of the register content.

Command Register (CMDR)

	7							0
CMDR	R/W	RCM	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

General Configuration Register (GCR)

	7							0
GCR	SP	AGCX	AGCR	EVX	SLOT	PU	CAM	LAW

Data Format and Interface Configuration Register (DFICR)

	7							0
DFICR	SD	SC	SB	SA	VDM			

Programmable Filter Configuration Register (PFCR)

	7							0
PFCR	GX	GR	GZ	FX	0	FR	DHPR	DHPX

Tone Generator Configuration Register (TGCR)

	7							0
TGCR	TG	DT	ETF	CG	BT	BM	SM	SQTR

Tone Generator Switch Register (TGSR)

	7							0
TGSR	PM	TRL	0	TRR	DTMF	TRX	0	0

AFE Transmit Configuration Register (ATCR)

	7			0
ATCR	MIC	EVREF	0	AIMX

AFE Receive Configuration Register (ARCR)

	7		0
ARCR	HOC	CME	LSC

Test Function Configuration Register (TFCR)

	7			0
TFCR	0	EPZST	ALTF	DLTF

SDI-Configuration Register (SDICR); only available in SDI-mode

	7					0
SDICR	0	0	EPP1	EPP0	DCE	MCLKR

Time-Slot Configuration Register (TSCR); only available in SDI-mode

	7		0
TSCR	0	0	TS

Extended Configuration Register (XCR)

	7							0
XCR	PGCR	PGCX	RAAR	OBS	DHOP	DHON	DLSP	DLSN

Test Mode Register (TMR)

	7					0
TMR	TM	0	0	0	0	0

4.1 Command Register (CMDR)

Value after reset: BF_H

	7							0
CMDR	R/W	RCM	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

R/W 0: writing to configuration registers or to coefficient RAM
1: reading from configuration registers or from coefficient RAM

RCM **Reverse Channel Mode** (if R/W = 0)
0: receive and transmit in B1 (or IC1 in TE-mode)
1: receive and transmit in B2 (or IC2 in TE-mode)

For the IOM-2 two chip mode (GCR.CAM = 0), when pin AD is strapped to V_{SS} the above applies. When pin AD is strapped to V_{DD}, RCM operates in the reverse order.

CMDx Address to internal programmable locations

CMD 5	4	3	2	1	0	
0	0	X	X	X	X	code reserved
0	1	X	X	X	X	status operation (SOP)
1	0	X	X	X	X	coefficient operation (COP)
1	1	X	X	X	X	extended operation (XOP)

Coding of status operations (SOP):

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	CMD Sequence Description
0	0	0	0	SOP_0	R/W	2	<GCR>
0	0	0	1	SOP_1	R/W	2	<DFICR
0	0	1	0	SOP_2	R/W	2	<PFCR>
0	0	1	1	SOP_3	R/W	2	<TGCR>
0	1	0	0	SOP_4	R/W	2	<TGSR>
0	1	0	1	SOP_5	R/W	2	<ATCR>
0	1	1	0	SOP_6	R/W	2	<ARCR>
0	1	1	1	SOP_7	R/W	2	<TFCR>
1	0	0	0	SOP_8	R/W	2	<SDICR>
1	0	0	1	SOP_9	R/W	2	<TSCR>
1	0	1	0	SOP_A	R/W	2	<XCR>
1	1	0	1	SOP_D	R	2	<IDENT>[1)]
1	1	1	0	SOP_E	R/W	2	<TMR>
1	1	1	1	SOP_F	R/W	9	<TFCR>..<GCR>

1) See also 4.12.

Coding of coefficient operations (COP):

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	CMD Sequence Description	Comments
0	0	0	0	COP_0	R/W	9	<F1> <F1> <G1> <GD1> <T1> <T1> <..> <..>	Tone generator 1
0	0	0	1	COP_1	R/W	9	<F2> <F2> <G2> <GD2> <T2> <T2> <GTR> <GTX>	Tone generator 2 Additional TG-gain
0	0	1	0	COP_2	R/W	9	<F3> <F3> <G3> <GD3> <T3> <T3> <FD> <FD>	Tone generator 3 Dual tone frequency
0	0	1	1	COP_3	R/W	5	<K> <A1> <A2> <GE>	Tone filter
0	1	0	0	COP_4	R/W	5	<TON> <TON> <TOFF> <TOFF>	Control generator
0	1	0	1	COP_5	R/W	9	<GX> <GX> <GR> <GR> <..> <..> <..> <..>	Transmit gain Receive gain
0	1	1	0	COP_6	R/W	5	<GZ> <GZ> <..> <..>	Sidetone gain
0	1	1	1	COP_7	R/W	9	<FX1>..<FX8>	Correction filter FX
1	0	0	0	COP_8	R/W	9	<FX9>..<FX12> <FR1>..<FR4>	Correction filter FR
1	0	0	1	COP_9	R/W	9	<FR5>..<FR12>	
1	0	1	0	COP_A	R/W	9	<SP1>..<SP8>	Coefficients for
1	0	1	1	COP_B	R/W	9	<SP9>..<SP16>	Speakerphone
1	1	0	0	COP_C	R/W	9	<SP17>..<SP24>	
1	1	0	1	COP_D	R/W	9	<SP25>..<SP32>	
1	1	1	0	COP_E	R/W	9	<AGCX1>..<AGCX8>	AGC-transmit
1	1	1	1	COP_F	R/W	9	<AGCR1>..<AGCR8>	AGC-receive

Coding of extended operations (XOP):

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	Comments
0	0	0	0	XOP_0	W	1	Power-down mode
0	0	0	1	XOP_1	W	1	Power-up mode
1	1	0	1	XOP_D	W	1	DD/DU-voice channel swap (toggle function)
1	1	1	0	XOP_E	W	1	Software reset
1	1	1	1	XOP_F	R/W	1	Normal operation (NOP)

4.2 General Configuration Register (GCR)

Value after reset: 00_H

	7							0
GCR	SP	AGCX	AGCR	EVX	SLOT	PU	CAM	LAW

SP **Speakerphone**
0: speakerphone support disabled
1: speakerphone support enabled

AGCX **Automatic Gain Control Transmit**
0: automatic gain control disabled
1: automatic gain control enabled; only if speakerphone support is enabled (SP = 1)

AGCR **Automatic Gain Control Receive**
0: automatic gain control disabled
1: automatic gain control enabled; only if speakerphone support is enabled (SP = 1)

EVX **Enable Voice Transmit**
0: disable transmit voice data
1: enable transmit voice data (if GCR.PU = 0, idle code is transmitted)

SLOT **IOM-2 Slot Select** (IOM-2 TE-mode only)
0: bearer channels in IOM-channel 0
1: bearer channels in IOM-channel 1

PU **Power-Up**
0: the ARCOFI is placed in standby mode (power-down); all registers and coefficient RAM contents are saved and all interface functions are available
1: the ARCOFI is in a normal operating mode (power-up)

This bit can be directly accessed by the XOP_0/XOP_1 operations.

CAM **Chip Address Mode** (IOM-2 mode only)
0: two ARCOFIs are connected to the IOM-2 bus
1: only one ARCOFI is connected to the IOM-2 bus

LAW **Coding Law**
0: A-Law enabled
1: µ-Law enabled

4.3 Data Format and Interface Configuration Register (DFICR)

Value after reset: $F0_H$

	7				0
DFICR	SD	SC	SB	SA	VDM

SD-SA **Signaling I/O** (PCI-interface; only available in IOM-2 TE-mode)
0: Sx pin programmed as output (x: D, C, B or A)
1: Sx pin programmed as input (x: D, C, B or A)

VDM **Voice Data Manipulation**

Bit 3	2	1	0	Receive Voice Channel	Transmit Voice Channel	Description
0	0	0	0	–	B1	Transmit only
0	0	0	1	B1	B1	Transfer mode
0	1	0	0	–	B1 & B2	16-bit transmit only
0	1	0	1	B1 & B2	B1 & B2	16-bit transfer mode
1	0	0	0	B1 + B2	B1, B2	Conferencing mode
1	1	0	0	B1D + B1U	B1	Monitoring mode

– no signal

Note: In this table above the voice channels indicated are only examples. Other combinations of B1 and B2 (IC1 and IC2 in IOM-2 TE-mode) are possible and a complete description is given in section 3.5.

4.4 Programmable Filter Configuration Register (PFCR)

Value after reset: 00_H

	7							0
PFCR	GX	GR	GZ	FX	0	FR	DHPR	DHPX

GX **Transmit Gain**
0: gain set to 0 dB
1: gain coefficients loaded from coefficient RAM (CRAM)

GR **Receive Gain**
0: gain set to 0 dB
1: gain coefficients loaded from CRAM

GZ **Sidetone Gain**
0: gain set to $-\infty$ dB
1: gain coefficients loaded from CRAM

FX **Transmit Frequency Correction Filter**
0: filter is by-passed
1: filter coefficients loaded from CRAM

FR **Receive Frequency Correction Filter**
0: filter is by-passed
1: filter coefficients loaded from CRAM

DHPR **Disable High-Pass Receive** (50/60 Hz filter)
0: filter enabled
1: filter disabled

DHPX **Disable High-Pass Transmit** (50/60 Hz filter)
0: filter enabled
1: filter disabled

4.5 Tone Generator Configuration Register (TGCR)

Value after reset: 00_H

	7							0
TGCR	TG	DT	ETF	CG	BT	BM	SM	SQTR

TG **Tone Generator**
0: tone generator is disabled (if CG = 0)
1: tone generator is enabled; frequency and gain coefficients loaded from CRAM; CG has priority over TG

DT **Dual Tone Mode** (DTMF)
0: second trapezoid generator is disabled
1: second trapezoid generator is enabled; the output signal is added to the S/T signal generator (only if TGSR.DTMF = 0)

ETF **Enable Tone Filter**
0: tone filter is by-passed
1: tone filter is enabled; filter coefficients loaded from CRAM

CG **Control Generator**
0: control generator is disabled
1: control generator is enabled; time coefficients loaded from CRAM (tone generator is activated independently of TG-bit setting)

BT **Beat Tone Generator**
0: beat tone generator is disabled
1: beat tone generator is enabled; time coefficients loaded from CRAM

BM **Beat Mode**
0: beat mode is disabled; two tone ring activated when BT-generator is enabled
1: beat mode is enabled; three tone ring activated when BT-generator is enabled (only if TGSR.DTMF = 0)

SM **Stop Mode**
0: automatic stop mode is disabled
1: automatic stop mode is enabled; two and three tone ring gets turned off after the sequence is completed

SQTR **Square/Trapezoid Waveform**
0: trapezoid shaped signal is enabled (
only if tone ringing via loudspeaker and piezo mode is disabled: TGSR.TRL = 0 & TGSR.PM = 0)
1: square-wave signal is enabled

4.6 Tone Generator Switch Register (TGSR)

Value after reset: 00_H

	7							0
TGSR	PM	TRL	0	TRR	DTMF	TRX	0	0

PM **Piezo Mode**
0: ringing signal is not output to the piezo ring pins
1: ringing signal (square) is output to the piezo ring pins PZ1/PZ2

TRL **Tone Ringing via Loudspeaker**
0: ringing signal is not output directly to the loudspeaker pins
1: ringing signal (square) is output directly to the loudspeaker pins LSP/LSN

TRR **Tone Ringing Receive**
0: tone generator for receive direction is disabled
1: tone generator for receive direction is enabled

DTMF **DTMF-Generator** (transmit)
0: DTMF-generator for transmit direction is disabled
1: DTMF-generator for transmit direction is enabled

TRX **Tone Ringing Transmit**
0: tone generator for transmit direction is disabled
1: tone generator for transmit direction is enabled

4.7 AFE-Transmit Configuration Register (ATCR)

Value after reset: 00_H

	7			0
ATCR	MIC	EVREF	0	AIMX

MIC **Microphone Control**

Bit 7	6	5	4	Selected Mode
0	0	0	0	AMI is in **power-down** mode
0	0	0	1	0 dB amplification
0	0	1	0	6 dB amplification
0	0	1	1	12 dB amplification
0	1	0	0	18 dB amplification
0	1	0	1	24 dB amplification
0	1	1	0	30 dB amplification
0	1	1	1	36 dB amplification
1	0	0	0	42 dB amplification
1	1	1	1	AMI is in **by-pass** mode

EVREF **Enable V_{REF}** (2.4-V reference voltage)

0: V_{REF}-buffer is enabled in function of bit GCR.PU (global power-up) and ATCR/ARCR-programming

1: V_{REF}-buffer and internal reference voltage generation are enabled independently of the ARCOFI-configuration

AIMX **Analog Input Multiplexer**

Bit 1	0	Selected Input
0	0	AMI is connected to the pins MIP1/MIN1 (differential input)
0	1	AMI is connected to the pins MIP2/MIN2 (differential input)
1	0	AMI is connected to the pin MI3 (single-ended input)
1	1	not used

4.8 AFE-Receive Configuration Register (ARCR)

Value after reset: 00_H

	7			0
ARCR	HOC		CME	LSC

HOC **Handset Output Control**

Bit 7	6	5	Selected Mode
0	0	0	AHO is in **power-down** mode
0	0	1	2.5 dB amplification
0	1	0	– 3.5 dB amplification
0	1	1	– 9.5 dB amplification
1	0	0	– 15.5 dB amplification
1	0	1	– 21.5 dB amplification
1	1	1	AHO is in **by-pass** mode

CME **Control Monitoring Enable** (GCR.SP = 1)
0: controlled monitoring disabled
1: controlled monitoring enabled (if transmit speech is detected, ALS-programming is fixed to – 9.5 dB if LSC > – 9.5 dB)

LSC **Loudspeaker Output Control**

Bit 3	2	1	0	Selected Mode
0	0	0	0	ALS is in **power-down** mode
0	0	0	1	11.5 dB amplification
0	0	1	0	8.5 dB amplification
0	0	1	1	5.5 dB amplification
0	1	0	0	2.5 dB amplification
0	1	0	1	– 0.5 dB amplification
0	1	1	0	– 3.5 dB amplification
0	1	1	1	– 6.5 dB amplification
1	0	0	0	– 9.5 dB amplification
1	0	0	1	– 12.5 dB amplification
1	0	1	0	– 15.5 dB amplification
1	0	1	1	– 18.5 dB amplification
1	1	0	0	– 21.5 dB amplification
1	1	1	1	ALS is in **by-pass** mode

4.9 Test Function Configuration Register (TFCR)

Value after Reset: 00_H

	7			0
TFCR	0	EPZST	ALTF	DLTF

EPZST **Enable PZ1/PZ2** (piezo pins) to output internal Status Information
0: PZ1/PZ2 are used as piezo port pins
1: PZ1/PZ2 are used to indicate internal speakerphone conditions (PZ1: speakerphone idle condition; PZ2: speakerphone transmit active)
Note: PM-bit must be set (TGSR.PM = 1)

ALTF **Analog Loop** and **Test Functions**

Bit 5	4	3	Test Function
0	0	0	NOT: No Test Mode
0	0	1	ALF: Analog Loop via Front End
0	1	0	ALC: Analog Loop via Converter
0	1	1	ALN: Analog Loop via Noise Shaper
1	0	0	ALI: Analog Loop via Interface

DLTF **Digital Loop** and **Test Functions**

Bit 2	1	0	Test Function
0	0	0	NOT: No Test Mode
0	0	1	IDR: Initialize DRAM
0	1	0	DLP: Digital Loop via PCM-Register
0	1	1	DLS: Digital Loop via Signal Processor
1	0	0	DLN: Digital Loop via Noise Shaper

4.10 SDI-Configuration Register (SDICR); SDI-mode only

Value after reset: 00_H

	7					0
SDICR	0	0	EPP1	EPP0	DCE	MCLKR

EPP0 **Enable Push-Pull** at pin DU/DX (SDI-mode only)
0: open drain enabled
1: push-pull enabled

EPP1 **Enable Push-Pull** at pin SDR/SDX (SDI-mode only)
0: open drain enabled
1: push-pull enabled

DCE **Double Clock Enable** for DCLK (SDI-mode only)
0: single clock rate
1: double clock rate

MCLKR **Master Clock Rate** (synchronized system clock)

Bit 2	1	0	MCLK-Clock Rate
0	0	0	512 kHz
0	0	1	1.536 MHz
0	1	0	2.048 MHz
0	1	1	4.096 MHz
1	X	X	16.384 MHz (test mode)

4.11 Time-Slot Configuration Register (TSCR); SDI-mode only

Value after Reset: 00_H

	7							0
TSCR	0	0	TS					

TS **Time-Slot Selection**

Bit 5	4	3	2	1	0	Time-Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
		.				.
		.				.
1	1	1	1	1	1	63

4.12 Extended Configuration Register (XCR)

Value after reset: 00_H

	7							0
XCR	PGCR	PGCX	RAAR	OBS	DHOP	DHON	DLSP	DLSN

PGCR **Position of Gain Control Receive**
0: in front of the speech detector
1: behind the speech detector

PGCX **Position of Gain Control Transmit**
0: behind the speech detector
1: in front of the speech detector

RAAR **Read Automatic Attenuation Receive**
0: disabled
1: enabled

OBS **Observation** of internal modes (only for internal tests)
0: disabled
1: enabled

DHOP **Disable HOP**-Amplifier
0: HOP-amplifier normal mode
1: Disable HOP-amplifier (power-down, output high impedance)

DHON **Disable HON**-Amplifier
0: HON-amplifier normal mode
1: Disable HON-amplifier (power-down, output high impedance)

DLSP **Disable LSP**-Amplifier
0: LSP-amplifier normal mode
1: Disable LSP-amplifier (power-down, output high impedance)

DLSN **Disable LSN**-Amplifier
0: LSN-amplifier normal mode
1: Disable LSN-amplifier (power-down, output high impedance)

Note: XCR.RAAR = 1, SOP_D (read) monitors the magnitude of the gain-cell AGCR instead of IDENT.

4.13 Test Mode Register (TMR)

Value after reset: 00_H

	7					0
TMR	TM	0	0	0	0	0

TM **Test Mode** (only for internal tests)
000: normal mode

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A [1)]	– 25 to 80	°C
Storage temperature	T_{STG}	– 65 to125	°C
Voltage on any pin with respect to ground	V_S	– 0.3 to V_{DD} + 0.3	V
Maximum voltage on any pin	V_{max}	7	V

1) Reduced performance

ESD-integrity (according MIL-Std 883D, method 3015.7): 1000 V
exception: The pins #14, #16, #17 and #18 are not protected against voltage stress > 630 V (versus VSSx, x = A, D, P). The output performance prohibits the use of adequate protective structures.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC-Characteristics

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input leakage current	I_{IL}	– 1.0	1.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level (except pins SCLK, MCLK, DCLK)	V_{IH1}	2.0	V_{DD} + 0.3	V	
L-input level (except pins SCLK, MCLK, DCLK)	V_{IL1}	– 0.3	0.8	V	
H-input level (except pins SCLK, MCLK, DCLK)	V_{IH2}	0.7 V_{DD}	V_{DD}	V	
L-input level (except pins SCLK, MCLK, DCLK)	V_{IL2}	0	0.3 V_{DD}	V	
H-output level (except pins PZ1/PZ2)	V_{OH1}	2.4		V	I_O = 400 µA
H-output level (pins PZ1/PZ2)	V_{OH2}	V_{DD} – 0.45		V	I_O = 2 mA

DC-Characteristics (cont'd)

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-output level (except pin DU)	V_{OL1}		0.45	V	I_O = – 2 mA
L-output level (pins DU, DD[1])	V_{OL2}		0.45	V	I_O = – 7 mA
V_{DD} supply current standby (IOM-2 TE)	I_{DDS1}		0.9	mA	V_{DD} = 5 V; DCL = ON
	I_{DDS2}		0.2	mA	DCL = OFF
V_{DD} supply current operating (IOM-2 TE) [2]	I_{DDO1}		25	mA	V_{DD} = 5 V emergency ringing via ALS (TGSR.TRL = 1)
	I_{DDO2}		25	mA	handset mode (ARCR.HOC = 010_B)
Input capacitance	C_I		10	pF	
Output capacitance	C_O		15	pF	

[1] If voice channel swap (XOP_D) is enabled.

[2] Operating power dissipation is measured with all analog outputs open.
All analog inputs are set to V_{REF}.
The digital input signal (pin DD) is set to an idle code.
For the emergency ringing mode, the tone generator is set to 400-Hz single tone (square).
In this mode the loudspeaker amplifier is set to – 3.5 dB (3.2 Vpp)

Note: Power dissipation values are target values.

AC-Characteristics

Inputs are driven to 2.4 V for a logical "1" and to 0.45 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC-testing input/output waveforms are shown below.

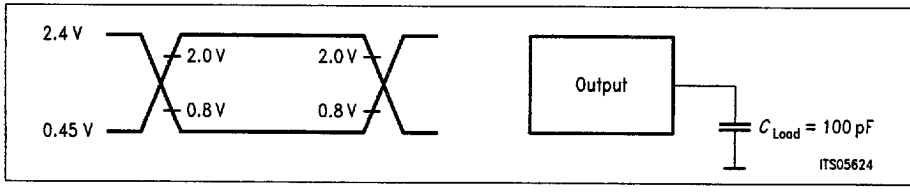


Figure 38
Input/Output Waveforms for AC-Tests

Analog Front End Input Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
AMI-input impedance	Z_{AMI}	15			kΩ	300 – 3400 Hz
AMI-input voltage swing	V_{AMI}			19.3	mVpk	42 dB
AMI-gain	G_{AMI}			42	dB	9.55 mV at 1 kHz

Analog Front End Output Characteristics

AHO-output impedance	Z_{AHO}			2	Ω	300 – 3400 Hz
AHO-output voltage swing [1]	V_{AHO}		3.2		Vpk	Load measured from HOP to HON
AHO-output high voltage [1]	V_{AHOH}		3.2		Vpk	input load – 1 mA @ HOP/HON
AHO-output low voltage [1]	V_{AHOL}		3.2		Vpk	input load + 1 mA @ HOP/HON
ALS-output impedance	Z_{ALS}			2	Ω	300 – 3400 Hz
ALS-output voltage swing [1]	V_{ALS}		3.2		Vpk	Load measured from LSP to LSN
ALS-output high voltage [1]	V_{ALSH}		3.08		Vpk	input load – 60 mA @ LSP/LSN
ALS-output low voltage [1]	V_{ALSL}		3.08		Vpk	input load + 60 mA @ LSP/LSN
V_{REF} output impedance	Z_{VREF}			2	Ω	Load measured from V_{REF} to V_{SSA}
V_{REF} output voltage	V_{VREF}	2.35		2.45	V	input load – 2 mA @ V_{REF}

[1] The maximum output voltage swing corresponds to the maximum incoming PCM-code (± 127).

Transmission Characteristics

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Limit Values		Unit	Test Condition
	min.	max.		
Attenuation Distortion	0		dB	< 200 Hz
@ 0 dBmO	– 0.25		dB	200 – 300 Hz
	– 0.25	0.25	dB	300 – 2400 Hz
	– 0.25	0.45	dB	2400 – 3000 Hz
	– 0.25	0.9	dB	3000 – 3400 Hz
	0		dB	> 3400 Hz
Out-of-band signals				receive:
		– 35	dB	4.6 kHz
		– 45	dB	8.0 kHz
				transmit:
		– 35	dB	4.6 kHz
		– 40	dB	8.0 kHz
Group delay distortion		750	µs	500 – 600 Hz
@ 0 dBmO [1]		380	µs	600 – 1000 Hz
		130	µs	1000 – 2600 Hz
		750	µs	2600 – 2800 Hz
Signal-to-total distortion	35		dB	0 to – 30 dB
(method 2)	29		dB	– 40 dB
	24		dB	– 45 dB
Gain tracking	– 0.3	0.3	dB	3 to – 40 dB
(method 2)	– 0.6	0.6	dB	– 40 to – 50 dB
@ – 10 dBmO	– 1.6	1.6	dB	– 50 to – 55 dB
Idle-channel noise		– 75	dBmO	receive (A-Law; Psoph.)
		– 66	dBmO	transmit (A-Law; Psoph.)
Cross-talk		– 66	dB	Reference: 0 dBmO
Programmable AFE gain	– 0.5	0.5	dB	step accuracy
	– 1.0	1.0	dB	overall accuracy
Overall programming range				Receive:
(with specified transmission	– 21.5	11.5	dB	loudspeaker
characteristics)	– 21.5	2.5	dB	earpiece
				Transmit:
	0	42	dB	differential inputs
	0	24	dB	single ended input

[1] Delay measurements include delays through the A/D and D/A with all features filters FX, GX, FR and GR disabled.

IOM®-2 Bus Switching Characteristics

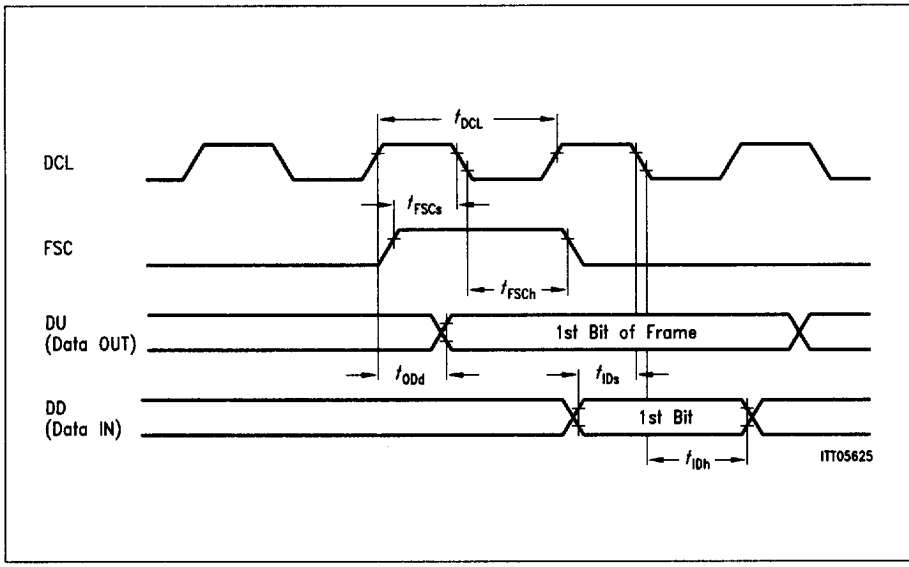


Figure 39
IOM®-2 Bus Timing Diagram

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL-clock period [1]	t_{DCL}		651		ns
DCL-clock period [2]	t_{DCL}		244		ns
DCL-duty cycle		30	50	70	%
FSC-period	t_{FSC}		125		µs
FSC-setup time	t_{FSCs}	70			ns
FSC-hold time	t_{FSCh}	40			ns
DD-data-in setup time	t_{IDs}	50			ns
DD-data-in hold time	t_{IDh}	50			ns
DU-data-out delay	t_{ODd}			150	ns

1) 768 kbit/s (IOM-2 TE-Mode); max. jitter of ± 160 ns once in FSC-period.
2) 2048 kbit/s (IOM-2 Non-TE-Mode)

PCI-Switching Characteristics (IOM®-2 TE-Mode)

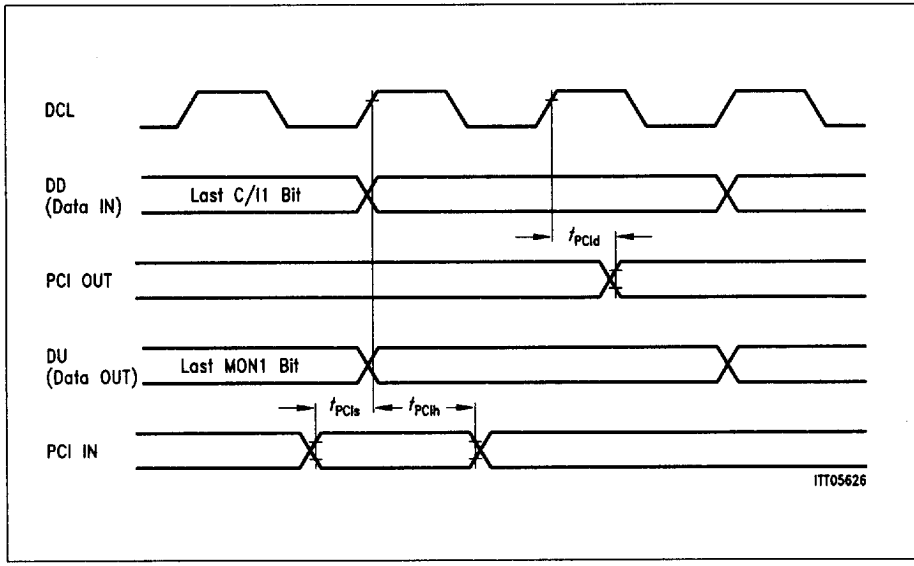


Figure 40
IOM®-2 Bus Timing Diagram (TE-Mode)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCI-data-out delay	t_{PCId}		350	ns
PCI-data-in setup time	t_{PCIs}	50		ns
PCI-data-in hold time	t_{PCIh}	100		ns

SCI-Switching Characteristics

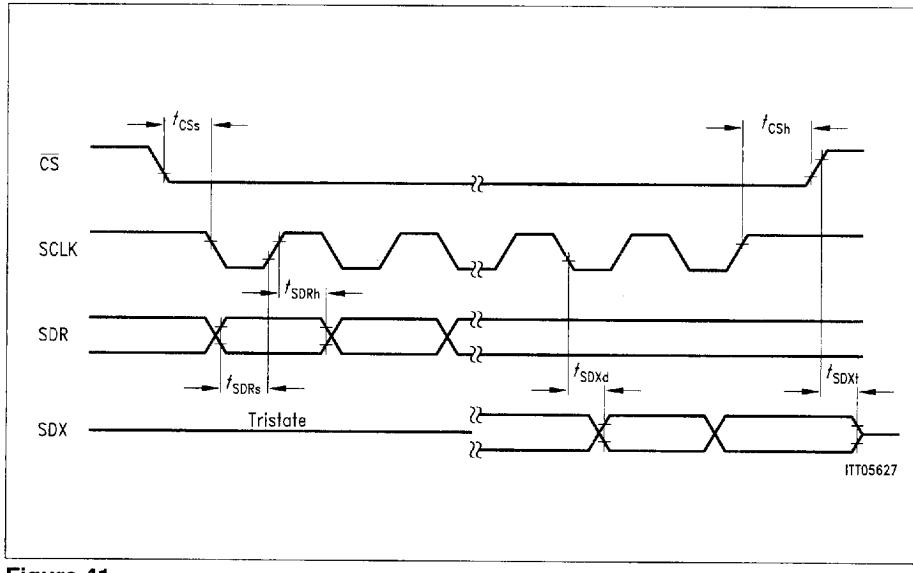


Figure 41
SCI-Switching Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCLK-frequency	f_{SCLK}		2048	kHz
Chip Select setup time	t_{CSs}	0		ns
Chip Select hold time	t_{CSh}	0		ns
SDR-setup time	t_{SDRs}	50		ns
SDR-hold time	t_{SDRh}	50		ns
SDX-data-out delay	t_{SDXd}		150	ns
SDX $\overline{CS}$ high to tristate	t_{SDXt}		30	ns

SDI-Switching Characteristics

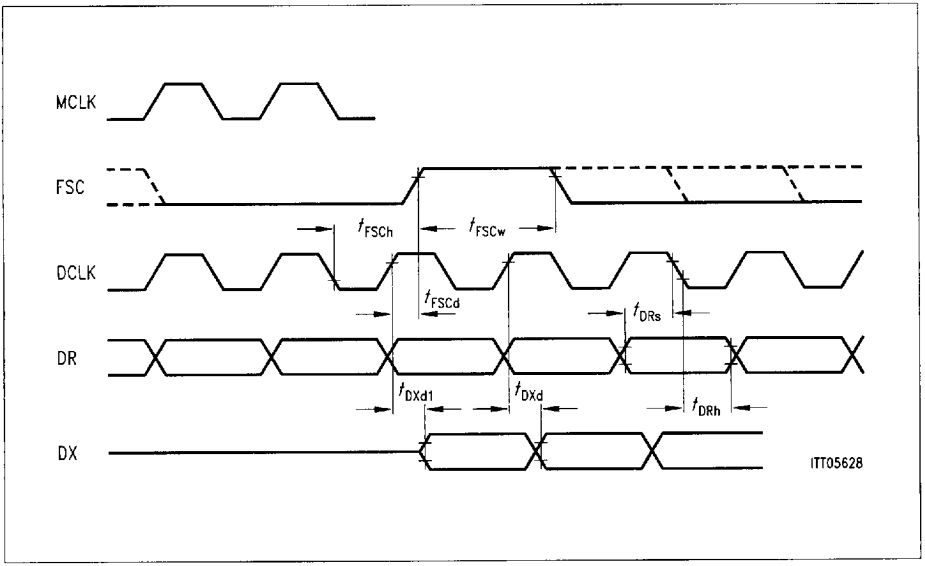
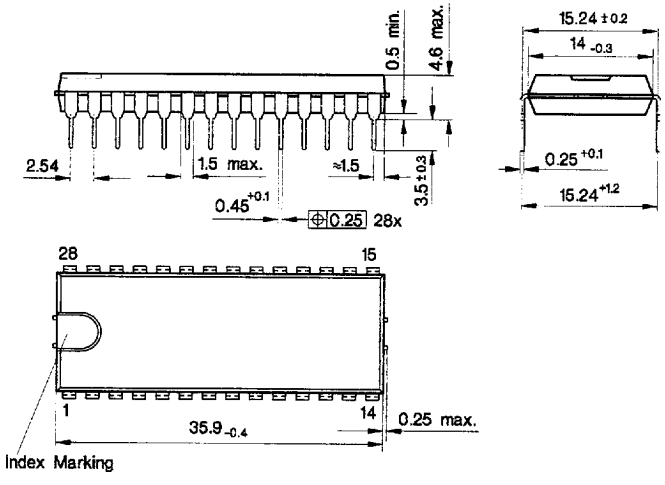


Figure 42
SDI-Switching Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
MCLK-frequency	f_{MCLK}	512	4096	kHz
DCLK-frequency	f_{DCLK}	64	4096	kHz
FSC-pulse width	t_{FSCw}	40		ns
FSC-hold time from DCLK low	t_{FSCh}	30		ns
FSC-delay time	t_{FSCd}		30	ns
DR-setup time	t_{DRs}	50		ns
DR-hold time	t_{DRh}	50		ns
DX-data-out delay (t_{FSCd} < 0 ns)	t_{DXd1}		80	ns
DX-data-out delay ($t_{FSCd} \geq 0$ ns)	t_{DXd1}		80 + t_{FSCd}	ns
DX-data-out delay	t_{DXd}		80	ns

6 Package Outlines

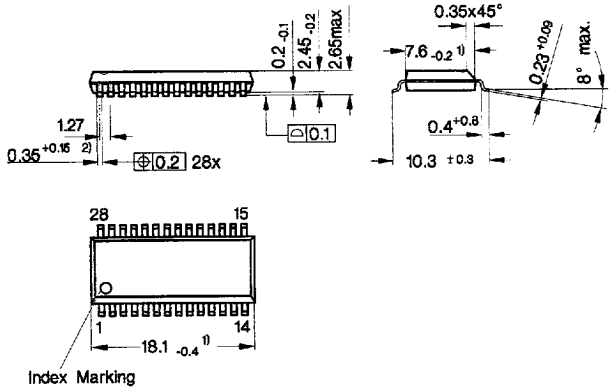
Plastic Package, P-DIP-28
(Dual-in-Line)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

Dimensions in mm

Plastic Package, P-DSO-28 (SMD)
(Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

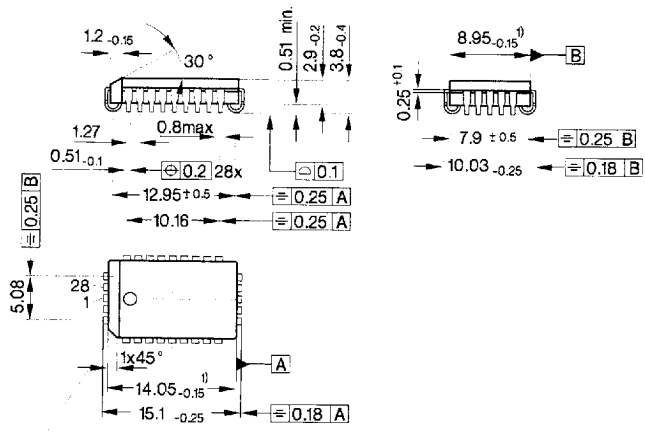
GPS05123

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-LCC-28-1 (R) (SMD)

(Plastic Leaded Chip Carrier)



Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05018

Sorts of Packing

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SMD = Surface Mounted Device

Dimensions in mm